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A NOVEL METHOD OF PRODUCTION OF CdS/CdTe THIN FILM SOLAR CELLS

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A thesis submitted in partial fulfilment of the requirements of the University of Northumbria at Newcastle for the degree of Doctor of Philosophy

Department of Electrical, Electronic Engineering and Physics, Faculty of Engineering, Science and Technology, University of Northumbria at Newcastle in collaboration with Joule Programme

September 1993

To

my late father

Ch. Khushi Muhammad Bhatti

and

brother Mr. Farooq Ahmed Bhatti

ABSTRACT

Thin films of CdTe have been produced using stacked elemental layer (S.E.L.) processing. This method consists of depositing alternate layers of the elements (Cd and Te in this case) followed by an anneal to react them to form CdTe. The layers were deposited using vacuum evaporation and the deposition conditions optimised so that uniform layers with controllable thicknesses produced. The CdTe was synthesised by annealing in air, vacuum and nitrogen environments and the crystal structure, crystallinity, surface morphology, optical, electrical properties of the layers related to the fabrication conditions.

An anneal at 450°C for 15 minutes was found to be optimum for fully synthesising the CdTe without degrading the optical properties of the layers. All the layers synthesised had the sphalerite crystal structure. The layers synthesized in nitrogen and vacuum environments consisted of small randomly. oriented grains (≈ 1000 Å in diameter) whereas the layers synthesized in air consisted of slightly larger grains.

X-ray diffraction data for the latter layers however indicated that $CdTeO_3$ was present as a second phase material and hence the layers synthesised in nitrogen or vacuum were preferred.

It was found that annealing the CdTe layers after dipping them into a solution of $CdCl_2$ in methanol recrystallised the CdTe so that the layers now consisted of large columnar grains. This annealing treatment also converted the as synthesized layers from n-type to p-type with net acceptor concentration ≈ 10^{15} - $10^{16}cm^{-3}$.

Solar cells made using the recrystallised layers had efficiencies ≈ 2% ($V_{o.c.}$ ≈ 680mV, $J_{s.c.}$ ≈ 11mA/cm^2 and F.F. ≈ 0.35)

The solar cells were fully characterised and detailed measurements indicate that the quality of the CdTe and its interface with CdS are good. The efficiency is limited by the series resistance of the device and further work to reduce the contact resistance resistance to the CdTe and the bulk resistances of the CdS and CdTe should improve both $J_{s.c.}$ and the F.F. to improve the device efficiency to > 10%.

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CHAPTER I

INTRODUCTION

Electronic devices which directly convert light into electricity are known as "solar cells" and the phenomenon used in these devices is known as the "photovoltaic effect".

The photovoltaic effect was first observed by Bequerel in 1884 [1] when he observed that electricity was produced when he illuminated platinum electrodes immersed in an acidic solution. Later in 1873 Adams and Day [2] observed a similar effect in a selenium diode, the first solid state photovoltaic device.

Photovoltaic devices based on selenium [3-6] and copper oxide [7-10] were developed in the 1930s and found application as cheap, simple to operate devices for measuring light intensity. These early devices had low efficiencies < 1% and it was only when Chapin et al [11] produced a solar cell with an efficiency of 6% using crystalline silicon that solar cells were seriously considered for generating power; it was realised that such devices were potentially the best way of supplying power for satellites in the rapidly emerging U.S. space programme [12].

These p-n junction devices work on the principle that when a semiconductor is illuminated excess hole-electron pairs are produced and when these excess carriers diffuse to the junction region the electric field there separates them and pushes them through an external detection

circuit generating electrical power. A major requirement for efficient solar cell action is that the minority carrier diffusion length (a measure of the distance the excess carriers diffuse before recombination) is much greater than the absorption length (a measure of how thick the material should be to absorb most of the incident light)

In 1954 Lofferski [13] theoretically determined how the efficiency of p-n junction solar cell depended on the material used to make the solar cell and showed that there was an optimum value of the energy gap equal to 1.5 eV. Crystalline silicon with E_g = 1.1eV was not hence the best material in theory for solar energy conversion and interest was stimulated in developing other semiconductor materials such as gallium arsenide (GaAs) [14] and cadmium telluride [15,16] which had energy bandgaps close to the optimum value of Eg.

Another device of early interest was the CdS/Cu_2S thin film solar cell [17-21]. Although the energy bandgap of Cu_2S = 1.2 eV was somewhat lower than the optimum value, 1.5 eV, and the device was a "heterojunction" (a junction of dissimilar materials) rather than homojunction (a p-n junction made out of one material) it was found that promising efficiencies could be achieved, moreover with much cheaper fabrication techniques than those used with silicon. It was realised that silicon was not very good material for absorbing light because of its indirect energy bandgap; to absorb the light incident the silicon layers had to be thick and

of high crystalline quality to permit the minority carriers generated to diffuse to the junction region without substantial loss through recombination. Both these factors meant the cost of silicon solar cells would be high. Copper sulphide (as well as GaAs and CdTe) have direct energy bandgaps and hence absorb the light within a relatively short distance reducing the need for a thick absorber layer and the need for a long minority carrier diffusion length. Thus material and production costs could be minimised.

Although substantial improvements were made in improving the efficiency of Cu_2S/CdS solar cells these devices were found to degrade with time and after substantial research efforts the devices have not found wide application because the stability problem has not been overcome [22]. Despite its non-ideal energy bandgap, its nonideal absorbing properties and its high cost the crystalline silicon solar cell was found to be stable and with improvements in efficiency to find the applications not only in space but also terrestrially. Improvements in device design, in particular the use of "texturing and light trapping" have resulted in solar cell devices with efficiencies, up to 24 % and module efficiencies > 20% [23]. Commercial modules currently available have efficiencies = 15% with a cost of $3.5/peak watt. (A module with an area of $1/3m^2$ generates 50 peak watts i.e generates 50 watts for an irradiance of $1kW/m^2$ and costs about £600). To reduce the cost of production of silicon solar cells and modules innovative developments have

included the use of polycrystalline silicon [24,25] rather than crystalline silicon and the development of amorphous silicon devices [26]. Commercial modules using polycrystalline silicon have efficiencies of 15% with a cost 1.5-3$/peak Watt. Although reported efficiencies for solar cells produced using amorphous silicon devices can be upto ≈10% the efficiency of such devices degrades when the cells are illuminated due to the so called "Stabler-Wronski effect" [27-30]. The stabilisation of these devices using multijunction structures has been reported [30] but the more complex structures used add to the cost of manufacture and reduce the yield of the production processes for large scale manufacture.

Silicon solar cells have now many commercial applications including their use to generate power for water pumping systems, to power refrigerators used to store vaccines to supply power for navigational aids and to supply power in remote locations which cannot easily connected to national grid supplies [31,32]. Another important application is the use of "photovoltaics" to supply power for the T.V sets used in classrooms in remote areas where teachers are not available. A very successful T.V classroom system has been established on the Ivory Coast where 20,000 children are being educated using remote T.V. classrooms [33].

Various American, Japanese and European companies are also using photovoltaics in consumer products such as solar powered calculators, watchs, lights, clocks and battery charges [31].

Concurrent with the development of silicon technology has been the development of solar cells made using III-IV compounds such as gallium arsenide. It is found that solar cells made from silicon when used on satellites degrade in efficiency due to " radiation damage " and in semiconductors such as GaAs and InP the cell degradation due to radiation damage is less severe [34-37].

Solar cells made using these materials, particularly, GaAs have higher efficiencies than those made of Si because of their superior physical properties [38].

Also such solar cells are found to improve in efficiency when they are heated unlike silicon solar cells which are found to degrade in efficiency. Thus GaAs solar cells can be used in " concentrator systems " where light from the sun is collected by a lens and focussed onto them [39-40]. The highest efficiency device ever produced uses a GaAs p-n junction with a GaSb P-N junction beneath it in a so called " tandem arrangement "; this device has an efficiency ≈ 38% in concentrated sunlight [38].

The major problem with the III-IV compounds and GaAs in particular is that crystal imperfections severely reduce device performance and the production of high quality materials needed for good solar cell efficiencies means that manufacturing costs are high. Although this is offset by using concentrator systems to concentrate the sunlight onto a small area the concentrator cells must track the sun and the sun must not be blocked in any way for the system to work efficiently [42,43].

Such concentrator systems are used in very hot regions

of the world, where these are high levels of unimpeded sunlight. (The cost of system estimated to be about 2.5$/peak Watt.)

For more temperate climates " flat-plate technology " is considered to be more economic for generating power from "diffuse" sun light [39]. There are currently many demonstration projects showing that solar cells and modules can produce power on a larger scale than the current commercial applications. For example the largest photovoltaic "power station" in the world is at San Luis Opispo in California, U.S.A [44] (producing 6MW of power) and the largest in Europe at Central Solaire Mont-Soleil, Switzerland (producing 500kW of power).

The technology is ecologically sound, reliable, and is in energy production terms good but not yet economic compared to the other forms of energy production.

To lower the cost of solar cell and module production, a desirable aim for all applications of photovoltaics, cheaper methods of manufacture must be used and this has stimulated substantial research into the use of thin film devices made using compound semiconductors.

Although the CdS/Cu_2S device (mentioned earlier) was found to be unstable devices made using other materials have proved not to have this problem. Foremost amongst these materials are copper indium diselenide ($CuInSe_2$) and cadmium telluride (CdTe) [45,46]. Both these materials are currently being studied and developed in Europe as a part of the "Joule research programme" and the work presented in this thesis is a contribution to

the "EUROCAD" part of the programme. The aim of the programme is to develop different methods of manufacture, particularly those with the potential to be scaled-up for module production and to further develop an understanding of the CdS/CdTe solar cell.

The methods used to deposit the CdTe include electrodeposition (B.P Solar International), screen printing (University of Ghent), close spaced sublimation (Battelle Institute), sputtering and ion assisting doping (University of Parma), M.O.C.V.D. (University of Durham) and atomic layer epitaxy (Microchemistry Ltd, Finland). In this work a novel method, stacked elemental layer (S.E.L) processing has been used to produce CdTe. This technique was originally developed in our laboratory to produce $CuInSe_2$ [47]. The technique involves depositing alternate layers of the elements in the stoichiometric ratio needed to form the compound followed by an anneal to react them to form the compound. The exothermic reaction between the elements should produce very high internal temperature within the layers resulting in robust layers of the material. The technique is flexible in that a range of methods can be used to deposit the layers and the production of the large area of material, with minimal material wastage is possible. In this work thermal evaporation was used to deposit the layers of Cd and Te because this was the simplest technique available.

The objectives of the work were, first to determine whether CdTe could be formed using this technique, second

to relate the properties of the CdTe to the preparation conditions used, and thirdly to determine whether such CdTe was suitable for producing efficient solar cells.

This thesis thus :-

1. presents the background theory relevant to understanding the principles of operation of solar cell devices, in particular, the dependence of solar cell performance on the properties of the materials used.
2. reviews the history of the development of cadmium telluride solar cells.
3. outlines the experimental methods used to produce the layers used and to characterise the layers and devices produced
4. presents the result and discusses their significance and
5 presents conclusions and recommendations for future work

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CHAPTER II

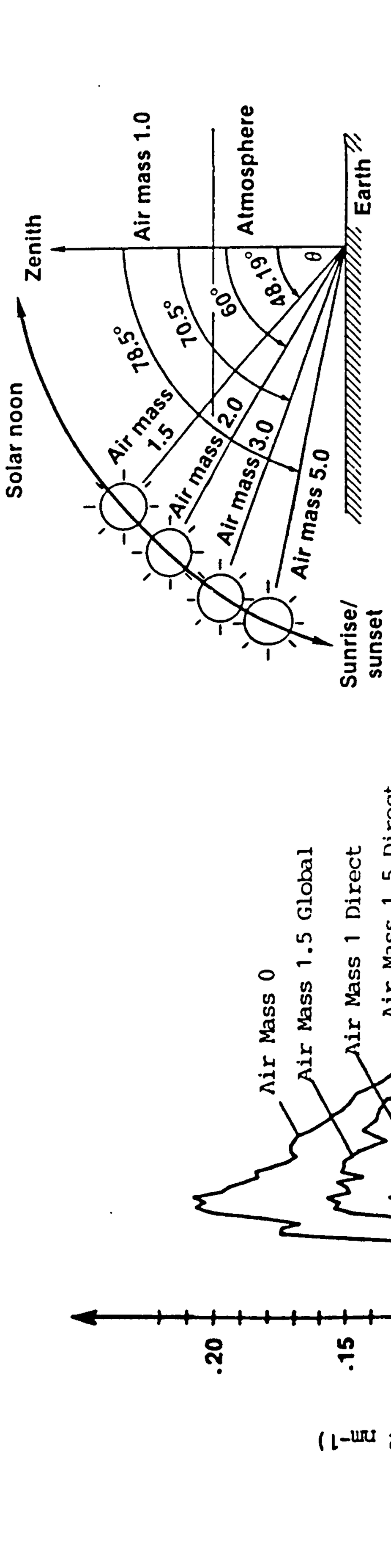
BACKGROUND THEORY

2.1 Solar Radiation:

The spectral distribution of light incident from the sun just outside the Earths atmosphere (A.M.O. spectrum) is given in fig. 2.1. The spectrum may be approximated to that emitted by a 6050 K blackbody and most of the energy radiated (98%) lies with in the wave length range, 0.25 to 3μm. The energy incident normally on an area of 1 m^2 at the average distance of the Earth from the sun is known as the " solar constant ", and it has the currently accepted value, 1.353kW m^{-2}.

When the sunlight passes through the Earths atmosphere some of the radiation is reflected, some absorbed and some diffusely scattered. The diffuse component of the radiation is found to be strongly peaked in the blue region of the spectrum and it contributes 8-10% of the radiation falling on the Earths surface on a clear day. In Northern Europe where the skies are often cloudy as much as 60% of the sunlight arriving at the Earths surface is diffuse.

The longer the path length of the sunlight through the Earths atmosphere the more the sun light is attenuated and the solar spectrum from the sun modified. The minimum path length will occur when the sun is directly overhead and the path length increases the lower the sun is in the sky.



Air Mass	Total Irradiance mW/cm2
0.0	130
1.5 Global	95
1.0 Direct	85
1.5 Direct	74
2.0 Direct	65

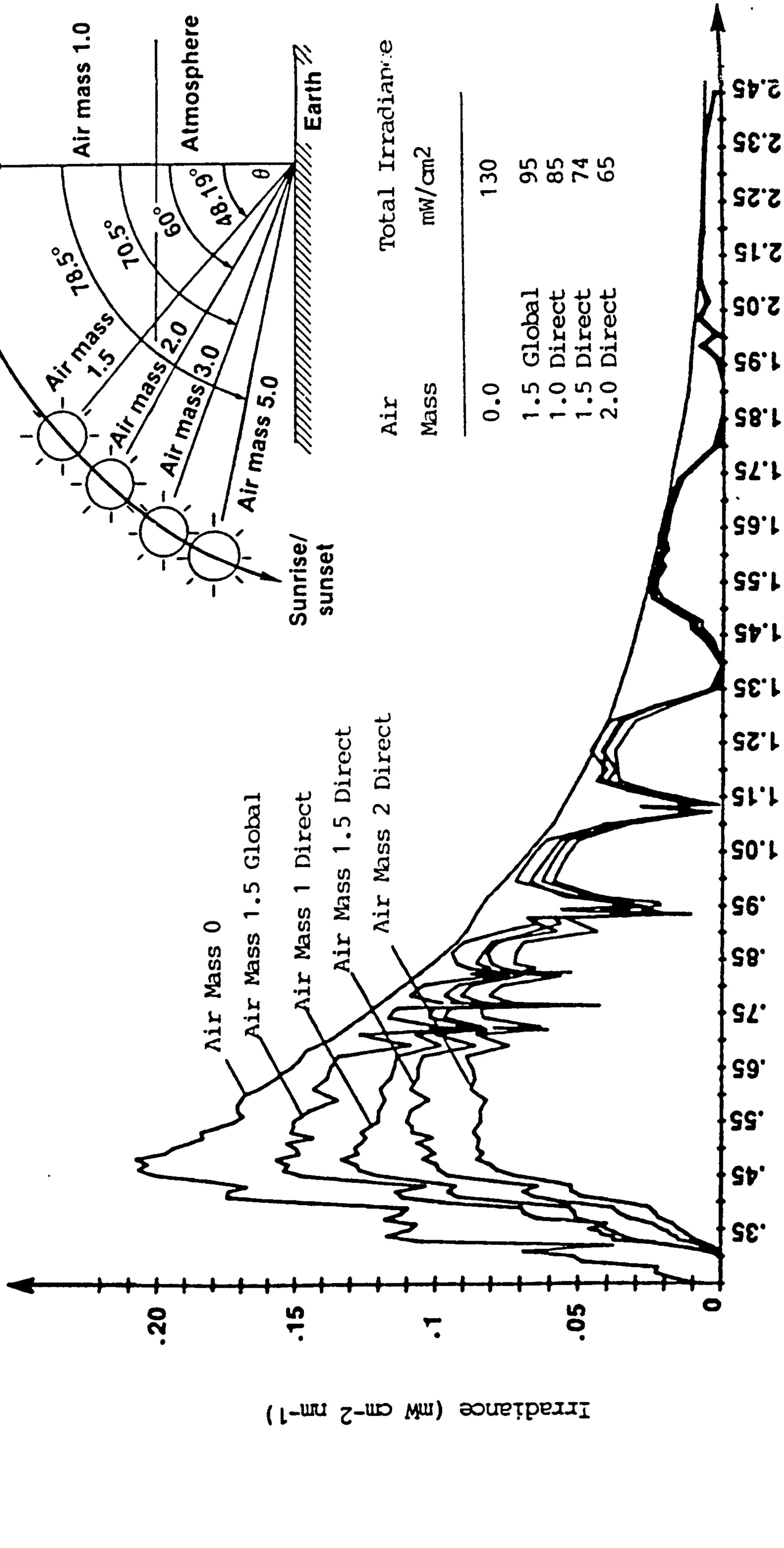


Figure 2.1 Solar Spectrum Irradiance Curves as a Function of the Wavelength of Light

The path length through the atmosphere is characterised by the term "air mass". The air mass is defined by :

$$\text{Air mass} = \sec\theta \; (= 1/\cos\theta) \qquad 2.1$$

where θ is the angle made between the sun and the zenith.

A.M.O refers to the spectrum from the sun just outside the Earths atmosphere, A.M.1 to the spectrum received on Earths surface when the sun is directly overhead i.e. $\theta=0$, A.M.1.5 to the spectrum received on the Earths surfaces when the sun is at an angle of 45° to the Zenith e.t.c.

The air mass spectra given in fig. 2.1 are "global" i.e. "average" air mass spectra which contain both direct and diffuse components of sun light incident on the Earth.

The power incident per unit area is taken to be $925Wm^{-2}$ for the A.M.1 spectrum $844Wm^{-2}$ for the A.M.1.5 spectrum and $691Wm^{-2}$ for the A.M.2 spectrum.

For space applications the A.M.O spectrum is obviously the most relevant whereas for terrestial applications the A.M.1.5. spectrum is usually considered to be the best average value to use.

Fig.2.2 indicates the world-wide distribution of solar energy in terms of duration of sunshine in hundreds of hours per year. It is evident that most regions of the world levels of solar insolation are high and that the possibility for generating energy on a large scale exists

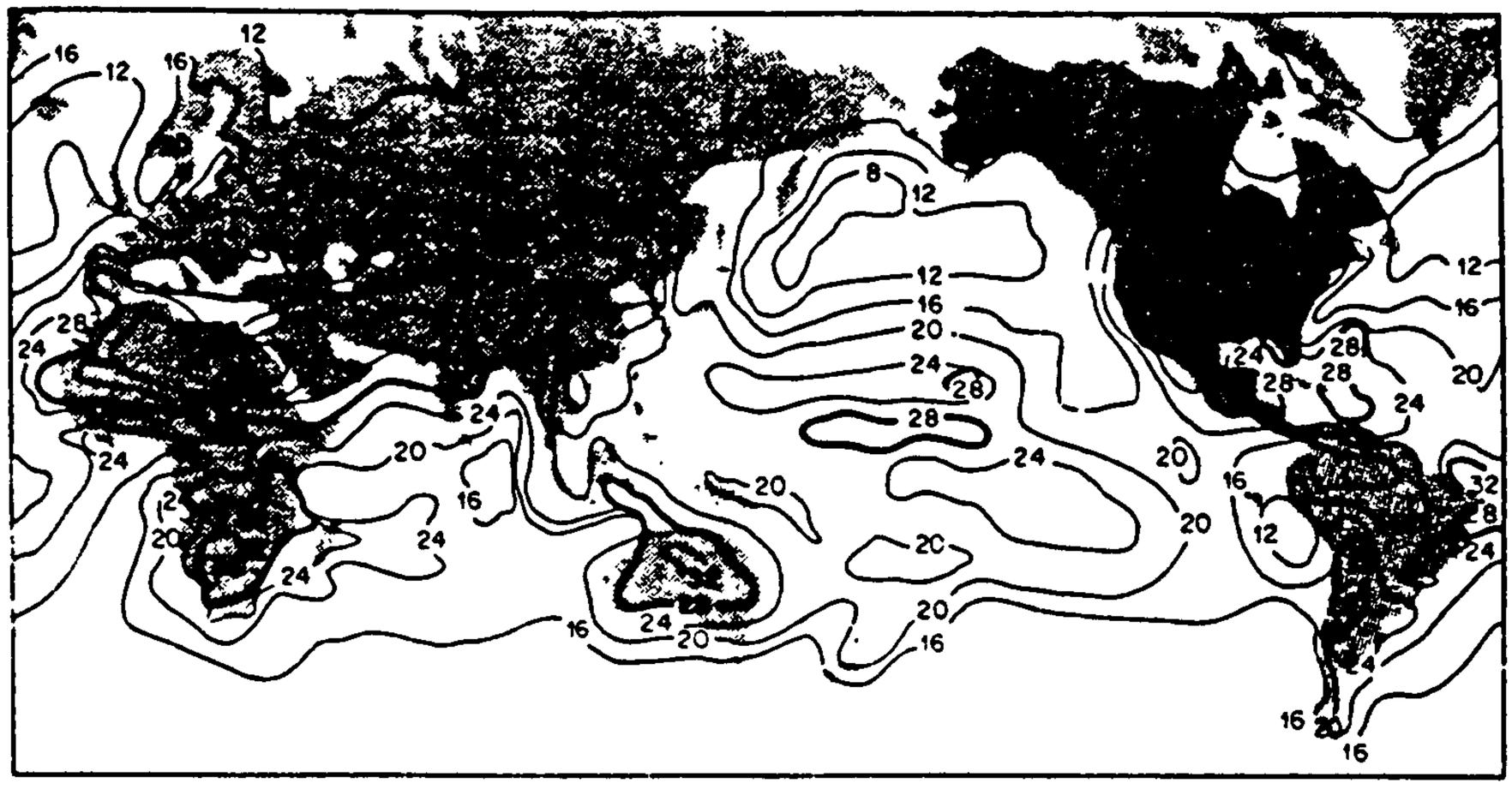


Figure 2.2 Solar Energy Distribution Over World Wide in Terms of Duration of Sunshine.

2.2 Theory of Operation of Solar Cells:

A solar cell is a p-n junction device consisting of a n-type "window layer" and a p-type "absorber layer". If the p-n junction is a homojunction i.e. a p-n junction is formed using one material then the window layer must be made very thin to allow light to reach the junction region. If the device is a "heterojunction" i.e. a p-n junction made from different semiconductors then it is possible to make the window layer transparent to the available light by using a semiconductor with a wide energy bandgap. Electrical contacts must also be made to the n-type and p-type regions. To permit light to reach the window layer and hence the junction region a grid contact as shown in fig.2.3 is commonly used. The grid geometry is designed to ensure efficient collection of carriers, and to ensure the resistance of the material forming the grid is small enough to not perturb device performance while allowing as much light as possible to reach the junction [1,2]. The back contact is usually deposited over the entire back surface of the p-type absorber and deposited sufficiently thick to ensure series resistance losses in this layer are minimal. The choice of the materials used for contacts, their method of deposition and subsequent heat treatment are governed by the need to form "ohmic contacts" to the n-type and p-type regions i.e. to form contacts with resistances sufficiently low as to not perturb device performance.

When the n-type and p-type regions of a p-n junction are in contact electrons diffuse from the n-type side to the

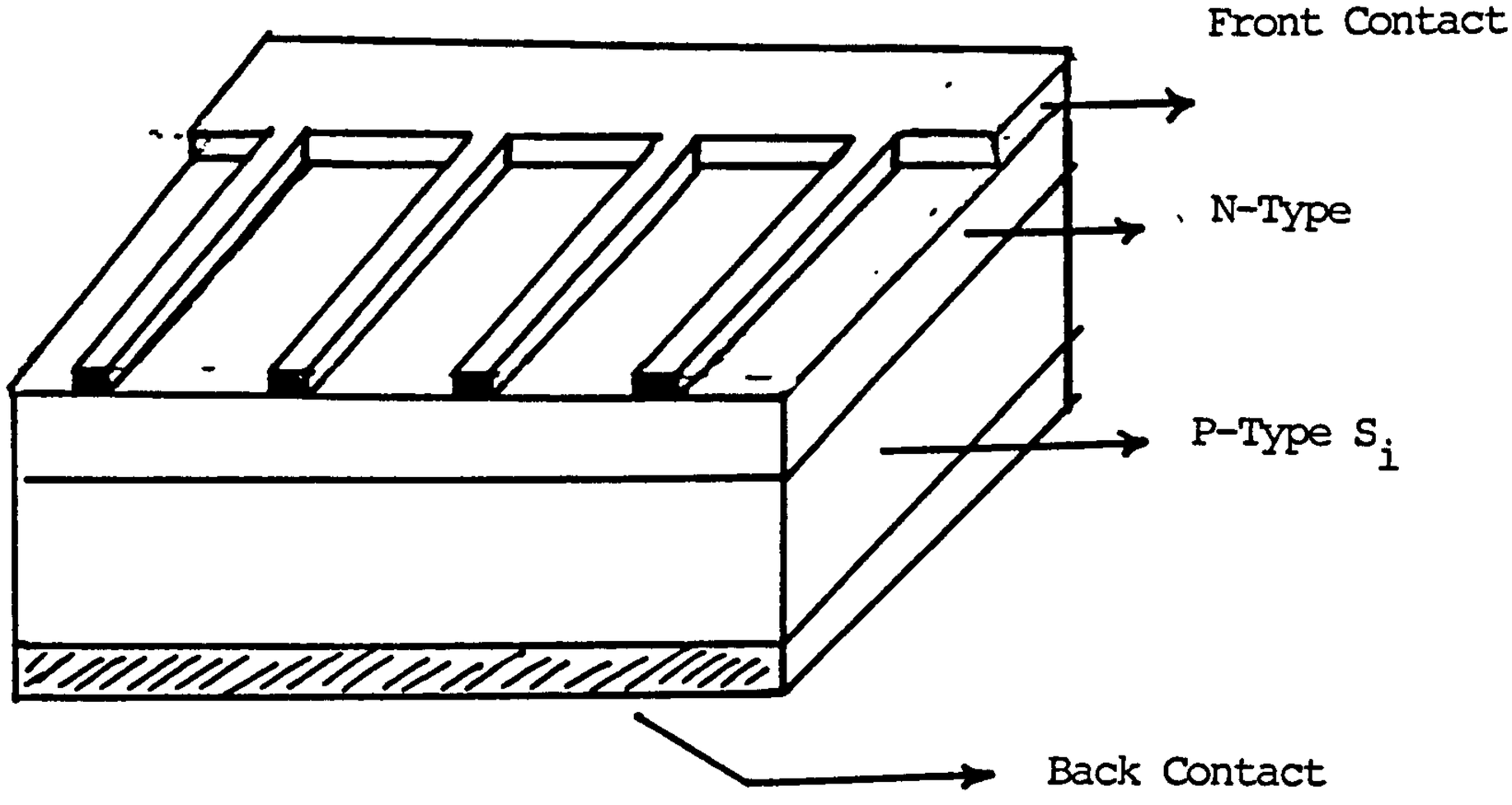


Figure 2.3 Diagram of a Silicon p-n Solar Cell

p-type side and holes diffuse from the p-type side to the n-type side because of concentration gradients existing for each of these carriers within the device.
The loss of electrons from the n-type side of the device results in a net positive charge on the n-type side the loss of holes from the p-type side results in a net negative charge. An electric field is hence produced at the interface which causes the drift of the electrons from the p-side to n-side of the device and the drift of holes from the n-type side to the p-type side so that the net electron flow and net hole flow through the device are zero when no bias is applied to the device. Because there is an electric field at the interface and E =-dV/dx there is a potential difference between the n-type and p-type side of the device.
The built-in potential difference is known as the "built-in voltage" or "diffusion voltage" of the junction.The region where the potential varies, (i.e. where there is an electric field acting), is known as the "depletion region". The variation of the charge density, potential and electric field across a homojunction device are shown in fig. 2.4.
If a semiconductor is illuminated with photons with energy greater than the energy bandgap of the semiconductor then the electrons are excited from the valence band to conduction band leaving a corresponding number of holes in the valence band.
If these excess carriers are generated in the depletion region the electrons move towards the n-type side and the

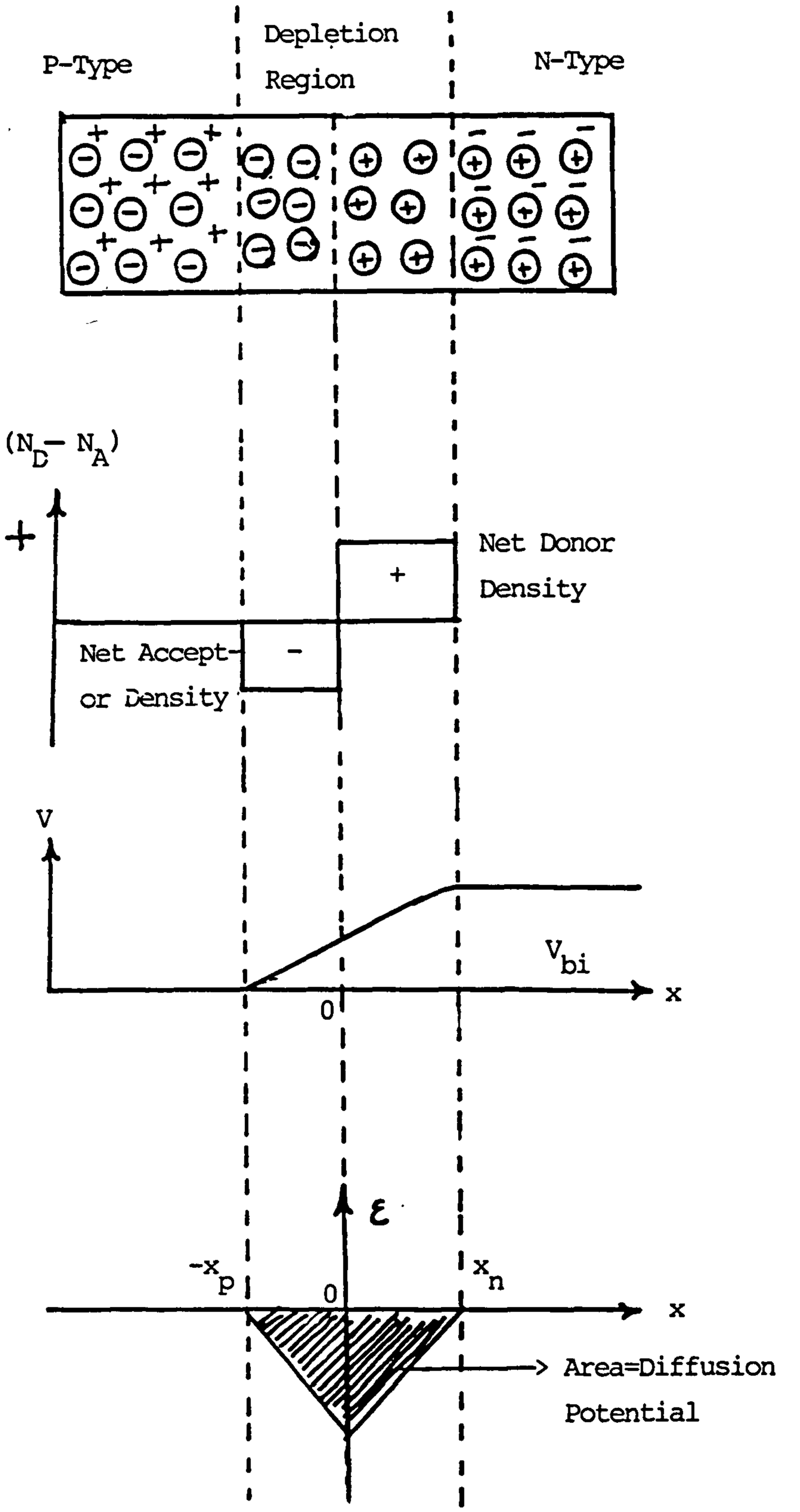


Figure 2.4 Diagram of p-n Junction in Thermal Equilibrium

(a) Space-charge Distances

(b) Variation of Potential With Distance

(c) Electric Field Distribution

holes to move towards the p-type side. Charge carriers generated near to the depletion region that can diffuse to the depletion region before recombination has occurred (i.e. within approximately a distance equal to the minority carrier diffusion length in the material) will also be acted upon by the electric field within the depletion region when they diffuse to this region. The excess electrons and holes are thus separated and pushed through an external detection circuit i.e a photocurrent is generated.

If the, W, is the depletion region width, L_e, the minority carrier diffusion length in the p-type material, L_h is the minority carrier diffusion length in n-type material and A_o the cross sectional area of the device then the charge carriers are generated within a volume ($w + L_e + L_h$)A_o.

If generation is assumed to be uniform throughout this volume and g_{opt} is the optical generation role i.e. the number of electron-hole pairs generated/sec then the photo current, I_L, is given by :-

$$I_L = qA_o g_{opt}(L_n+L_p+w) \qquad 2.2$$

The optical generation rate is closely linked to the "optical absorption coefficient", α of the semiconductor. For an efficient solar cell, α must be sufficiently large for the photons incident with different wavelengths that as many carriers as possible are generated within the volume $(L_n+L_p+w)A_o$. Semiconductors with direct energy

bandgaps such as CdTe and GaAs have a steep "absorption edge" (as shown in fig.2.5) and high values of α for $hv>E_g$ and hence the photons incident with $\lambda < \lambda_G$ (where $\lambda_G = hc/E_gq$) are strongly absorbed within the material. A measure of the thickness of semiconductor needed to absorb most of the incident photons is the " absorption length", $1/\alpha$, which for CdTe is about $1\mu m$. Thus to make an efficient CdTe solar cell $(L_n+L_p+w)>1\mu m$.

For silicon which has a indirect energy bandgap the absorption edge is not steep and many photons with $\lambda<\lambda_g$ for silicon may be absorbed deep within the silicon e.g. for photons with $\lambda = 1.03\mu m$, $\alpha\approx10^2cm^{-1}$ and hence $1/\alpha= 100\mu m$. The depletion region width in a silicon p-n junction increases with a decrease in doping of the p-type and n-type materials[3,4]. However too low a doping level in either side of the device will cause an increase in series resistance,R_s, which can in turn reduce device efficiency [5]. This limits , w, to about 1 μm. Thus the only way to ensure $(L_n+L_p+w)>1/\alpha$ is to produce materials with high values of L_n and L_p ie. to make the device using very pure crystals containing as few crystal defects as possible [3].

If the current-voltage (I-V) characteristic of the solar cell is measured under illumination then the most simple model of the behaviour assumes the "diode equation" is valid and that the photocurrent, I_L, may be simply added to the current flowing [6] i.e.

$$I = I_o[\exp(qV/AkT) - 1] - I_L \qquad 2.3$$

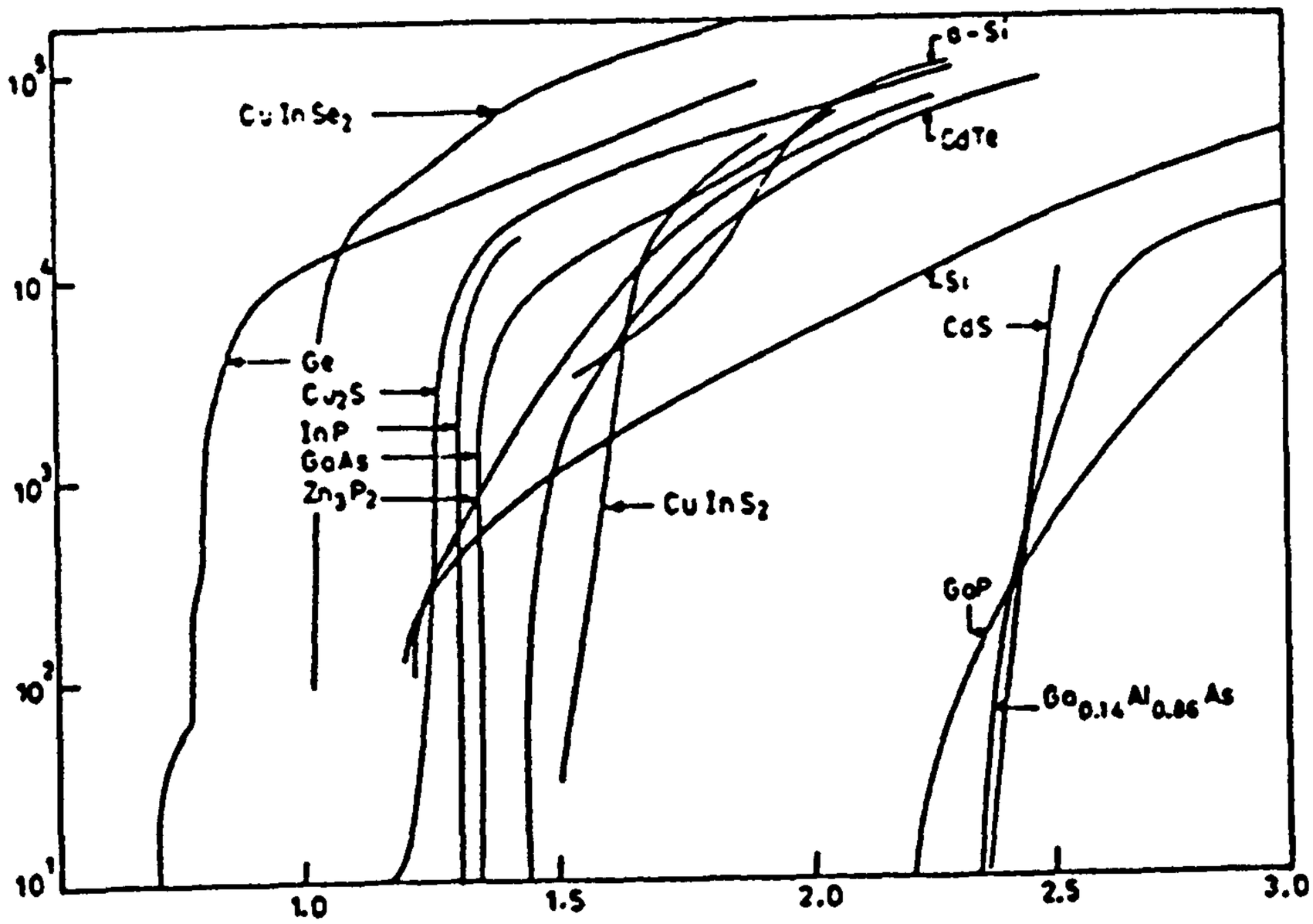


Figure 2.5 The Variation of Absorption Coefficient With Wavelength for Typical Solar Cell Materials

where I_o is the diode saturation current and A the "ideality factor" which has a value in the range 1-2 depending on whether diffusion or recombination dominates the current transport behaviour [6]. Such ideal behaviour is given in fig.2.6 [7].

The photocurrent generated when V = 0 is known as the "short-circuit current", $I_{s.c}$, because it corresponds to the photocurrent generated when a load resistor, R,, connected across the solar cell has R=0 i.e. the solar cell output terminals are short circuited.

For an ideal solar cell, $I_{s.c}$, is the is equal to I_L :-

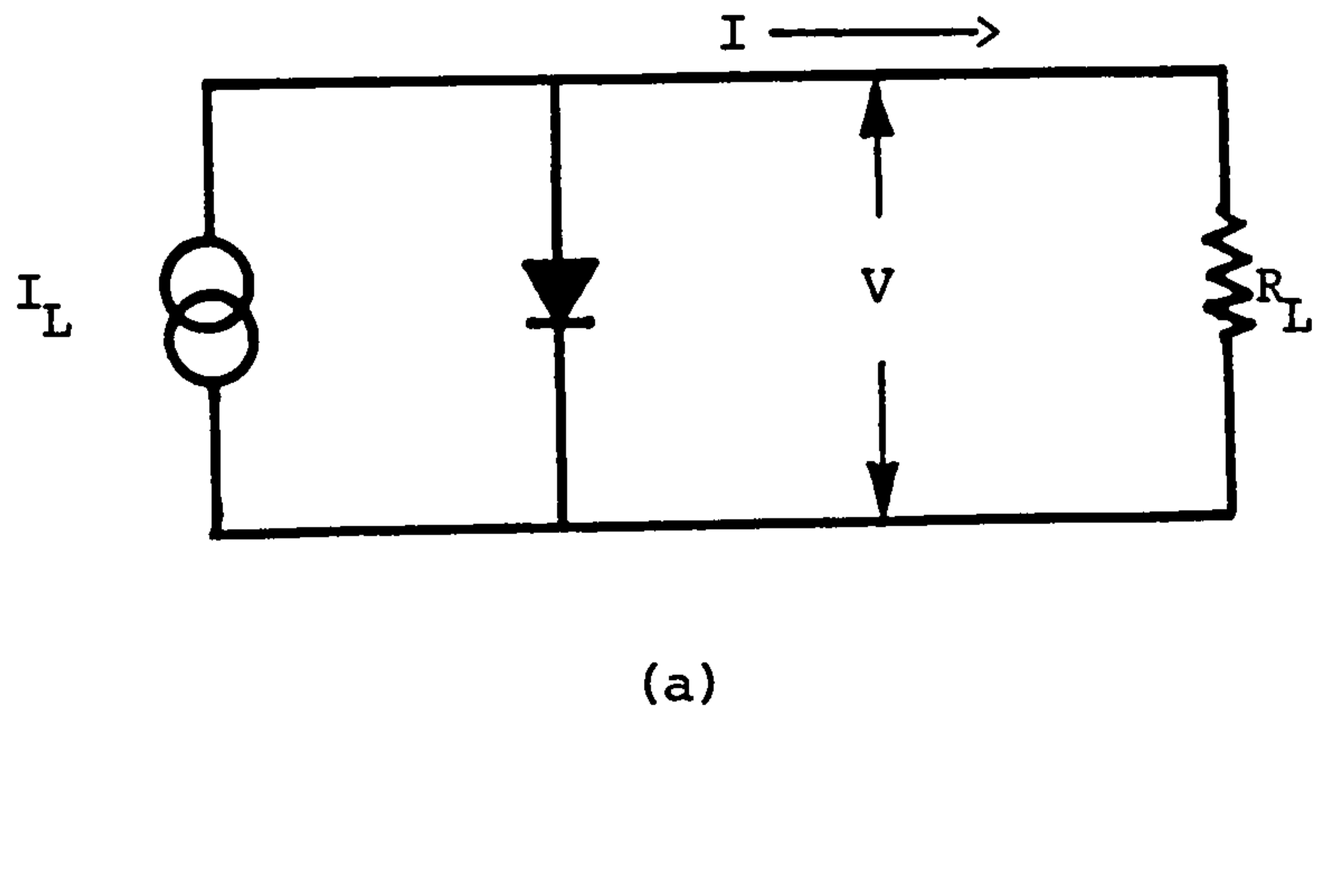
$$I_{s.c.} = I_L = qA_o g_{opt}(L_n+L_p+w) \qquad 2.4$$

if uniform generation of charge carrier is assumed. The magnitude of $I_{s.c}$ is assumed to be directly proportional to the incident light intensity. The forward bias voltage applied which reduces the photocurrent to zero is known as the "open circuit voltage", $V_{o.c.}$, of the device because it corresponds to the voltage produced when a load resistor, R, connected across the output terminals has R=∞ i.e. the output terminals are open-circuited.

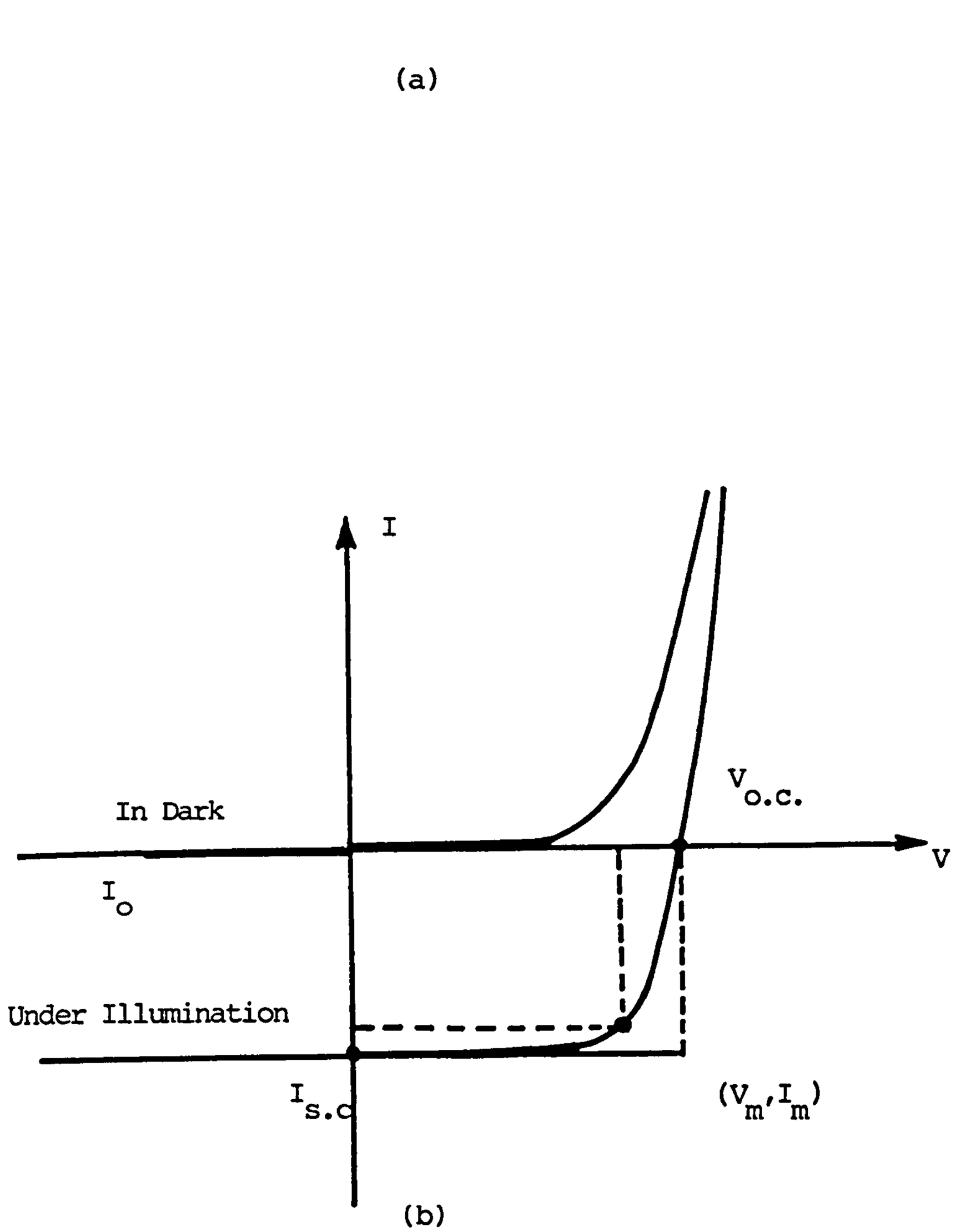
For an ideal solar cell, $V_{o.c.}$, is given by :-

$$V_{o.c.} = AkT/q[\ \ln(I_{s.c}/I_o) + 1] \qquad 2.5$$

For a given, $I_{s.c}$, produced, I_o, should be as small as possible to produce a large value of $V_{o.c}$ and A as close



(a)



(b)

Figure 2.6(a) Equivalent Circuit Diagram for an Ideal Solar Cell.

(b) Current-Voltage Characteristic of an Ideal Solar Cell in the Dark and Under Illumination

to unity as possible. Although it might at first appear that A should be as large as possible to maximise $V_{o.c.}$ a large value of A is associated with a high value of I_o which more severely reduces $V_{o.c.}$

It is evident that power will not be produced if the device is either operated under short-circuit conditions or open circuit conditions because the power, P=IV, will be zero.

For an ideal solar cell:-

$$P = IV = I_oV[\exp(\exp(qV/AkT) - 1] - I_LV \qquad 2.6$$

and the maximum power generated will occur when dP/dV=0. Using such an approach it can be shown [8] that maximum power is generated for a voltage, V_m, and current, I_m given by :-

$$V_m = V_{o.c}\text{-}kT/q \ \ln[1+qV_m/AkT] \qquad 2.7$$

and $$I_m = I_L[1-AkT/qV_m]$$

The maximum power generated, P_m, will be given by:

$$P_m = I_mV_m \qquad 2.8$$

At this maximum power point the rectangle drawn within the I-V characteristic (I_m by V_m) will have the largest area possible i.e. the rectangle will "fill" the I-V characteristic as fully as as possible. A parameter known as the "fill-factor" (F.F.) is defined as :-

F.F. = $I_mV_m/I_{s.c}V_{o.c.}$ and it represents the filling of the I-V characteristic.

For an ideal solar cell [9] :-

$$F.F.=V_m/V_{o.c.}\{1-[\exp(qV_m/AkT)-1]/[\exp(qV_{o.c.}/AkT)-1]\} \quad 2.9$$

The fill-factor improves with an increase in the value of $V_{o.c.}$ and is larger for A=1 than for when A>1.

The "solar conversion efficiency", η, is the most important device parameter and it is defined as the ratio of the maximum power generated by the solar cell (p_{max}) to the power of the light incident on the solar cell (p). It follows that :

$$n = (I_{max}V_{max})/p = (I_{s.c.}V_{o.c.}F.F.)/p \quad 2.10$$

To maximize the efficiency, η , $V_{o.c.}$ I_{sc} and the F.F must all be maximised for a given incident power p, is given by

$$P = A_t\int F(\lambda)(hc/\lambda)\lambda \quad 2.11$$

where A_t is area of the device, $F(\lambda)$ the number of photons/cm^2/sec/unit bandwidth incident on the device at a wavelength, λ and hc/λ is the energy of each photon.

To maximise, η, losses in the solar cell must be minimised. The equation given by [10,11] indicates where losses may occur :-

$$n = \left(\int_{o}^{\lambda_g} P(\lambda)d\lambda\right)/\left(\int_{o}^{\infty} P(\lambda)d\lambda\right) * E_G\left(\int_{o}^{\lambda_g} N(\lambda)d\lambda / \int_{o}^{\lambda} P(\lambda)d\lambda\right) * (A_s/A_t) * (1-R) * (n_d) * (n_{coll}) * (qV_{o.c}/E_G) * F.F. \qquad 2.12$$

Term 1: This takes into account the fact that photons with energies less than E_g cannot contribute to the creation of electrons and holes because they are not absorbed.

Term 2: This represents the loss of energy due to carriers being generated with energies greater than E_G. The excess energy is lost as heat.

Term 3: This represents reflection losses from the front contact. A_S is the area of the cell not covered by the grid.

Term 4: This represents the loss of the light by reflection from the semiconductor surface. It may be minimised by using an antireflection coating.

Term 5: This term represents the incomplete absorption of light due to the solar thickness being inadequate.

Term 6: This term takes into account the fact that not all electron-hole pairs generated will contribute to the photocurrent. They will be lost by either bulk or surface recombination.

Term 7: For an ideal solar cell, $V_{o.c.}$, is equal to the diffusion voltage, V_D, which may be as high in value as E_G. $V_{o.c.}$ is usually limited by recombination to a value lower than V_D. [$V_{o.c}$ is usually at least 50% lower than V_D].

Term 8: The fill factor is not only related to $V_{o.c.}$ and A, as discussed previously, but strongly reduced by

the series resistance and shunt resistance of the device.

2.3 The Effect of Series and Shunt Resistance on Solar Cell Performance:

An equivalent circuit of a solar cell taking into account the series resistance,R_S , and the shunt resistance, R_{SH} , of the device is given in fig.2.7(a)

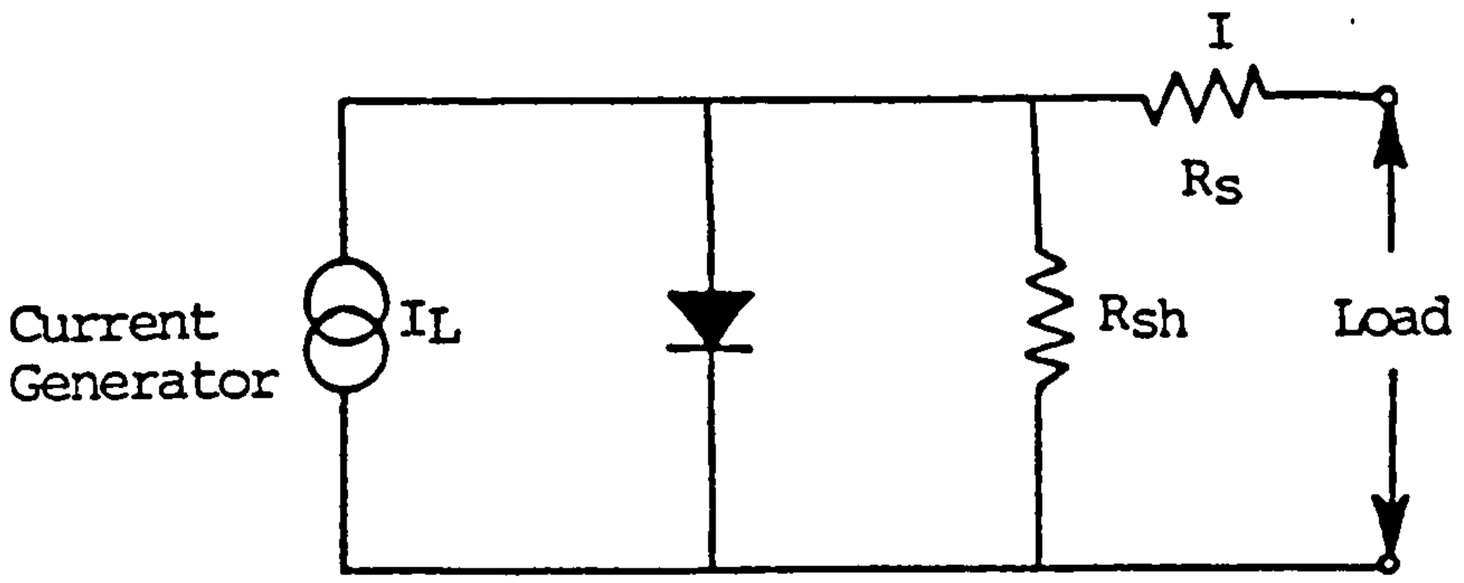
The series resistance arises from the bulk resistances of the n-type and p-type materials forming the device and from the resistances of the contacts to both the n-type and p-type materials [12].

The shunt resistance results from the presence of low resistance conduction paths at the interface. With polycrystalline devices the grain boundaries may be more conductive than the bulk material, because of segregated impurities, or because they are regions where there is more rapid diffusion of atoms from the back contact material. Grain boundaries may thus provide "short circuit" paths through the material leading to a low value for R_L.

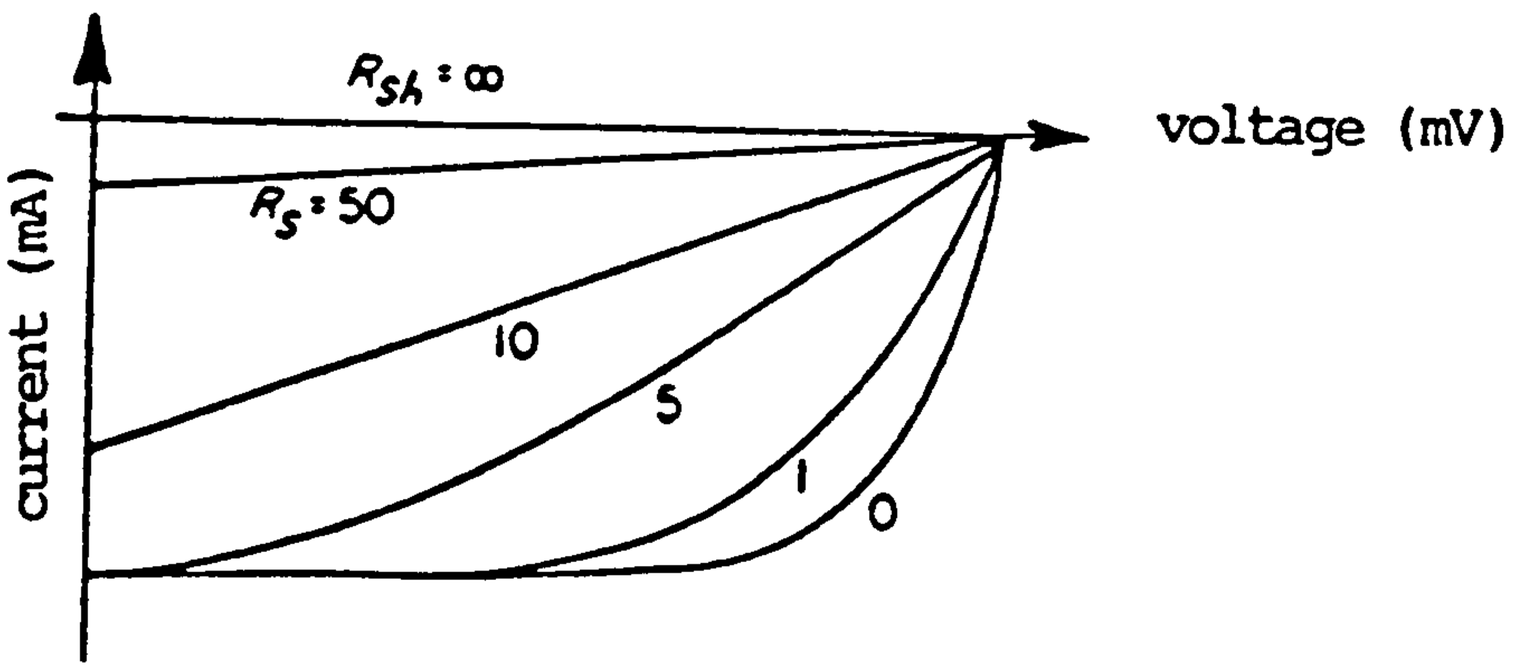
For an ideal solar cell the I-V characteristic is modified to [9,13,14]:-

$$I = I_o[\exp(q(V-IR_S)/AkT) - 1] + ((V-IR_S)/R_{SH}) - I_p \quad 2.13$$

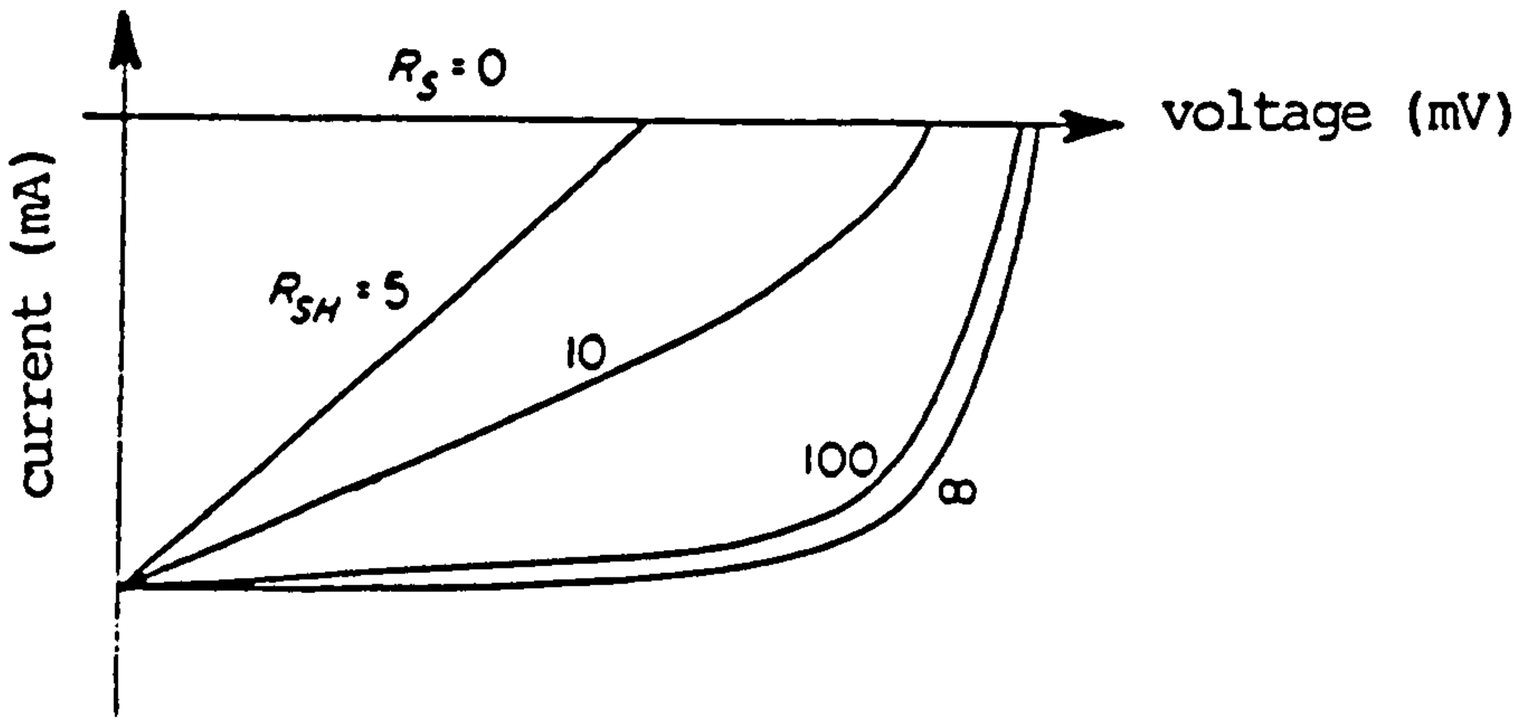
The effect of R_S and R_{SH} on the I-V characteristic has been determined by [5] and fig.2.7(b) shows the result obtained.



(a)



b(i)



b(ii)

Figure 2.7 (a) Equivalent Circuit for Solar Cell Including a Current Generator With Output Proportional to Light Intensity, a Series Resistance R_s and a Shunt Resistance R_{sh}

(b) The Effect of Shunt and Series Resistance on the I-V Characteristic of a Solar Cell

A small increase in R_S is found to reduce the maximum power available from the device whereas a shunt resistance as low as 100Ω does not appreciably alter the output power. The relative available power for R_S equal to 0, 1, 2, 5, or 10Ω is 100%, 77%, 27% and 14% respectively [4].

The series resistance should thus be ideally < 1Ω. The series resistance may be reduced when the device is illuminated because photoconductive effects in the n-type and p-type regions reduce their resistances. One ""rule of thumb" expression used is that $R_S<0.8/x\Omega$ for a solar cell with an area of $1cm^2$, where x is the solar concentration used [4].

2.4 Optical Properties of Thin Films:

The main methods used to determine the optical properties of thin films are given by Chopra [9] and Heavens [15,16]. The most commonly used technique involves the measurements of transmittance and reflectance as functions of the wavelength of incident light. When the incident beam is normal to the film and the film thickness is large enough for multiple reflections to be ignored, the transmittance through the film with refractive index (n_1-ik_1) and thickness (t) is given by the relation [17] :-

$$T = \{16n_0n_1(n_1^2+k_1^2)^2/[(n_1+n_2)^2][(n_0+n_1)^2+k_1^2] \exp(-4\pi vkt)\} \qquad 2.14$$

where v is the frequency of the incident light and n_0 and n_2 are the refractive indices of the ambient and the substrate respectively. The imaginary part of the complex refractive index, k, is known as the "extinction coefficient" and its value can be determined from the slope of ln(T) versus T [17]. If the surrounding medium is air, n_0=1 and the above equation reduces to :-

$$T = 16n_2(n_1^2+k_1^2)^2/[(n_1+1)^2+k_2^2][(n_1+n_2)^2+k_2^2] \exp(-4\pi k_1 t/\lambda) \qquad 2.15$$

Reflection is a much more complicated phenomenon than transmission because of there can be a reflection contribution from the backside of the transparent substrate. If the effect of the backside reflection of the film is ignored then the reflectance of the film can be related to the refractive indices with the following relation [17]:-

$$R = [(n_1-n_0)^2k_1^2]/[(n_1+n_0)^2+k_1^2] \qquad 2.16$$

If the surrounding medium is air then the above expression reduces to

$$R = [(n_1-1)^2+k_1^2]/[(n_1+1)^2+k_1^2] \qquad 2.17$$

It should be noted that reflectance measured can be affected by the surface roughness especially in the high energy region [18].

From the the law of conservation of energy :-

$$T + R + A_f = 1 \qquad 2.18$$

where A_f is the "absorption" of the material. The absorption coefficient , (α), is related to the absorbency of the film using the first order approximation [19] :-

$$t\alpha = A_f \qquad 2.19$$

and to the extinction coefficient, k_1, by

$$\alpha = 4\pi k_1/\lambda. \qquad 2.20$$

For highly absorbing films where no interference fringes are observed in the absorption edge and the percentage transmittance and reflectance are known, the absorption coefficient can be calculated using the following expression [9,20,21] :-

$$T = (1-R)^2\exp(-\alpha t) \qquad 2.21$$

This formula may be used when the refractive index of the substrate material is less than that of the thin film [9]. The substrate material used in this work was Corning 7059 glass with a refractive index equal to 1.53 at 589.3 nm and this is much lower than the refractive index of CdTe; R.I = 2.6 [9,22].

This formula is expected to be valid for CdTe thin films

deposited onto glass and is in fact found to be valid for most II-IV compounds deposited onto the glass [21].

The absorption coefficient is closely related to the energy band structure of the material. For semiconductors with direct energy bandgap, α, is given by [5] :-

$$\alpha = (C/hv)(hv-E_g)^{1/2} \qquad 2.22$$

where A is a constant.

Many workers [23] have used this relationship to determine the energy bandgap of the semiconductor; it is usually found by plotting $(\alpha hv)^2$ versus hv and then E_g is the intercept of straight line portion of the graph on the hv axis.

For materials with an indirect energy bandgap [4,19], α, is given by :-

$$\alpha = (A/hv)(hv-E_g)^{3/2} \qquad 2.23$$

This variation of α with hv is not as rapid as that observed with direct energy bandgap materials because phonons must be involved in the absorption process (to convert momentum) and this makes the absorption process less likely for incident photons of a given energy.

" Free carrier absorption " [4,24-27] and crystal imperfections and impurity atoms [24,27] may perturb the expected variation of α with hv.

The influence of free carrier absorption increases with an increase in carrier concentration [19]. Crystal

imperfections and impurities may introduce discrete energy levels into the energy bandgap which may shift the energy bandgap towards lower energies [4].

Interference fringes are very often observed in the transmittance versus wavelength data obtained in thin films and Manficier et al [28] present methods for determining the refractive index (as a function of wavelength, λ) and the film thickness from such data.

The refractive index, n, of the thin film is given by :

$$n = \{N+(N^2-n_0^2n_1^2)^{1/2}\}^{1/2} \qquad 2.24$$

where n_0 and n_1 are the refractive indices of air ang glass respectively. For air, n_0=1 and for corning 7059 glass, n_1=1.53 for λ=589nm.

N is a constant, and its value is determined using :-

$$N = [(n_0^2+n_1^2)/2]+2n_0n_1(T_{max.}-T_{min.})/(T_{max.}*T_{min.}) \qquad 2.25$$

where $T_{max.}$ and $T_{min.}$ are the transmittances at the maximum and minimum of the interference fringe.

Thus evaluating, N, from the experimental data and substituting into eq. 2.25 permits n to be calculated at a given wavelength.

The film thickness, t is given by :

$$t = (M\lambda_1\lambda_2)/[2(n(\lambda_1)\lambda_2-n(\lambda_2)\lambda_1)] \qquad 2.26$$

where M is the number of oscillations between the two

values of λ, (M=1 between two consecutive maxima or minima) and $(n)\lambda_1$ and $(n)\lambda_2$ are the refractive indices corresponding to the values of the wavelengths λ_1 and λ_2 respectively.

2.5 Spectral Response:

The "spectral response" of a solar cell is experimentally obtained by measuring the photocurrent generated when the solar cell is illuminated with light of different wavelengths. Because the light source used emits different wavelengths of light with different intensities and the spectrometer used may transit different amounts the spectral response is usually presented by plotting the "current responsitivity", R, or the "quantum efficiency", η versus wavelength because both of these quantities take into account these factors.

The current responsitivity is defined to be the ratio of the photocurrent generated, I_p, to the power of the incident radiation, P_λ, at a given wavelength i.e.

$$R=I_p/P_\lambda \quad \text{(Amp/Watt)} \qquad 2.27$$

The "quantum efficiency", η, is defined to be the number of electron-hole pairs generated per incident photon at a given wavelength.

The number of electron-hole pairs generated/sec is I_p/q and the number of incident photons/sec is P_λ/hv and hence :-

$$\eta = I_p hv/qP_\lambda \qquad 2.28$$

The reponsitivity and quantum efficiency are obviously closely linked and :-

$$R = \eta q/hv \qquad 2.29$$

For light of wavelength, λ, and power, P_λ, the photocurrent generated will be the sum of the photocurrent generated in the n-type regions and p-type regions of the device excluding the depletion region (I_n and I_p respectively) and the photocurrents generated in the depletion region in the n-type side of the device and the depletion region in the p-type side of the device (I_{nd} and I_{pd} respectively) [4,5] i.e. :-

$$I_p = I_n+I_p+I_{nd}+I_{pd} \qquad 2.30$$

The individual photocurrents may be calculated by integrating over the photon energy range of interest ($hv>E_g$) for the device region under consideration.

For a CdS/CdTe solar cell the "heterojunction window effect" is expected to be observed i.e. there should be no response to photons with energies less than the energy bandgap of CdTe because these are not absorbed in either the CdS or CdTe and there should be no response for photons with energies greater than with energy bandgap of the CdS because electron-hole pairs generated at the CdS surface are too far from the junction to contribute to a photocurrent. [The recombination of the excess carriers

will occur mainly at the CdS surface where recombination is enhanced].

For photons with energies less than the energy bandgap of CdS is transmissive and the light will be absorbed either the depletion region of the p-type CdTe, or within the bulk CdTe. Carriers generated in the depletion region and carriers generated within a diffusion length of the edge of the depletion region will contribute to the photocurrent.

The long wavelength fall-off in the spectral response has been used by several workers to determine the minority carrier diffusion length in CdTe [19,29-31]. These workers use the expression given by [32] for the photocurrent:-

$$I_{s.c.} = q\varphi(\lambda)T(\lambda)[1-\exp(-\alpha w)+\alpha L/(1+\alpha L)\exp(-\alpha w)] \quad 2.31$$

where $\varphi(\lambda)$ is the photon flux, $T(\lambda)$ is the transmittance through the CdS window layer, α is the absorption coefficient in the p-type absorber layer, w is the depletion layer width and L is the minority carrier diffusion length in the p-type layer.

When $\alpha(\lambda)w<<1$ i.e. carrier generation in the bulk CdTe dominates then this expression can be simplified to :-

$$[I_{s.c.}/q\varphi(\lambda)T(\lambda)]^{-1} = (1/L)[L+1/\alpha] \quad 2.32$$

If $\varphi(\lambda)$ and $T(\lambda)$ are constants then a plot of $1/I_{s.c.}$ versus $1/\alpha$ will be a straight line with an intercept as

the x-axis equal to L [32].

If the solar cell is reverse biased then the depletion width will increase but the diffusion length will be unaffected. If the photocurrent is not strongly bias dependent then the bulk generation of the photocurrent dominates over the generation in the depletion region [33] i.e. the material has a high value of minority carrier diffusion length.

If the photocurrent is strongly affected generation in the depletion layer dominates and the minority carrier diffusion length is probably small.

A small minority carrier diffusion length is also expected to result in a decrease in the photocurrent at wavelengths near the bandedge of the CdTe [34].

The spectral response measurements are hence a useful diagnostic tool to determine factors which influence the overall solar conversion efficiency of the device.

2.6 Heterojunction Solar Cell:

Heterojunction solar cells usually consist of a n-type material with a wide energy bandgap, the "window layer" and a p-type material with a narrower energy bandgap, "the absorber layer". This structure allows photons with energies less than the energy bandgap of the window layer to reach the absorber layer where they will be absorbed if their energies are greater than the energy bandgap of the absorber layer. The absorption of the light is hence also where carriers will be generated with most effect i.e. near to the junction region. Although it is possible

to fabricate devices using a p-type window layer and n-type absorber layer the structure using p-type absorber layer is preferred because the mobility and the minority carrier lifetime and hence minority carrier diffusion length of electrons, (the minority carriers in p-type material) are usually greater than those of holes (minority carrier in p-type material).

Advantages of using heterojunction devices rather than homojunction devices include enhanced spectral response at short wavelengths [5,26,35] which increases the photocurrent generated, a large diffusion voltage, which increases V_0 [9], and a reduction in lateral series resistance because the thickness of the window layer can be much greater than that possible in a homojunction device [36].

The use of heterostructures also permits the use of a wide range of materials which can not used to make homojunction devices e.g. many II-IV compounds e.g. CdS can only be made n-type due to self-compensatation effects. The major problems with heterojunctions arise because the n-type and p-type layers are different materials and there are hence discontinuities in their physical properties at the interface.

Usually the heterojunction partners are chosen to have the same crystal structure or related crystal structures. Even with the same crystal structure the semiconductors used will have different lattice parameters leading to a "lattice mismatch" at the interface [37].

The lattice mismatch between the two semiconductors with

lattice parameters, $\lambda 1$ and $\lambda 2$ is defined by [37]:-

$$\text{Lattice mismatch} = 2(\lambda 2 - \lambda 1)/(\lambda 1 + \lambda 2) \qquad 2.33$$

if $\lambda 1 < \lambda 2$ Values of the lattice mismatches for many heterojunction partners are given by [37];

For the CdTe/CdS heterojunction it is determined to be 4% for sphalerite CdTe/CdS device and 10% for wurtzite CdTe/CdS devices [37].

The lattice mismatch is important because it leads to strain at the interface and Van der Merve has shown that this strain may be relaxed by the formation of misfit dislocations at the interface [38] . These accommodate the stress by providing extra half planes of atoms in the material with the smaller lattice parameter.

The spacing, p, of the misfit dislocations along any direction is given by [38] :-

$$p = ab/(a-b) \qquad 2.34$$

where a is the repeat distance in the given direction of the smaller lattice constant material and b is the corresponding repeat distance in the other material. The incomplete bonds are known as " dangling bonds " and they may give rise to "interface states" at the junction of the two semiconductors.

Such interface states may act as recombination centres and the charge density associated with them may alter the electrical nature of the interface i.e. alter V_o , w etc

[39].

The materials forming the heterojunction may also have different thermal expansion coefficients. If a layer of one material is deposited on the other material at an elevated temperature and there is such a "thermal mismatch" then allowing the sample to cool to room temperature may result in the layers cracking or pealing from the substrate. Even when the layers do not peal or crack the stress may also produce interface states. Although all the physical properties of the material forming the heterojunction may be different the two discontinuities discussed have proved to be the most important. The "thermal mismatch", in particular, must obviously be minimised.

Another consideration when choosing the materials to form a heterojunction is whether cross diffusion of the elements from one side of the device to the other will be detrimental to device performance because some elements may be very active as a recombination centres when they cross diffuse into the heterojunction partner material [40].

For some heterojunction pairs the cross diffusion of the elements may be beneficial e.g. there is some evidence that the interdiffusion of the CdS and CdTe to form $CdS_{1-x}Te_x$ at the interface may reduce the density of interface states perhaps by reducing strain at the interface [41-43].

2.7 Ideal Energy Band Profile of Heterojunctions:

A method for modelling heterojunction behaviour was developed by Anderson [44]. Each semiconductor is assumed to be characterised by its energy bandgap, E_g, its electron affinity, X, and its work function, φ, as shown in fig.(2.8(a)). The electron affinity is the energy needed to take an electron from the conduction band-edge to the " vacuum level " (i.e. the energy level of free space or vacuum, outside the material) and the work function is energy required to take an electron from the Fermi level to the vacuum level.

When the two semiconductors are bought into intimate contact then electrons are transferred from the material with the higher energy Fermi level (lower work function) to the material with the lower energy Fermi level (higher work function) until the Fermi level is equal throughout the device as shown in fig.(2.8(b)). The "diffusion voltage", V_D, is thus equal to $E_{F2}-E_{F1}$ and to $\varphi_1-\varphi_2$.

It follows that :-

$$V_D = (X1 + E_{g1} - \delta_1) - (X2+\delta_2) \qquad 2.35$$
$$= E_{g1} + (X1-X2) - (\delta_1+\delta_2)$$

where the energy difference (in eV) between the Fermi level and the conduction bandedge for the n-type material, δ_1, and the energy difference between the Fermi level and the valence bandedge for the p-type material, δ_2, are given by :-

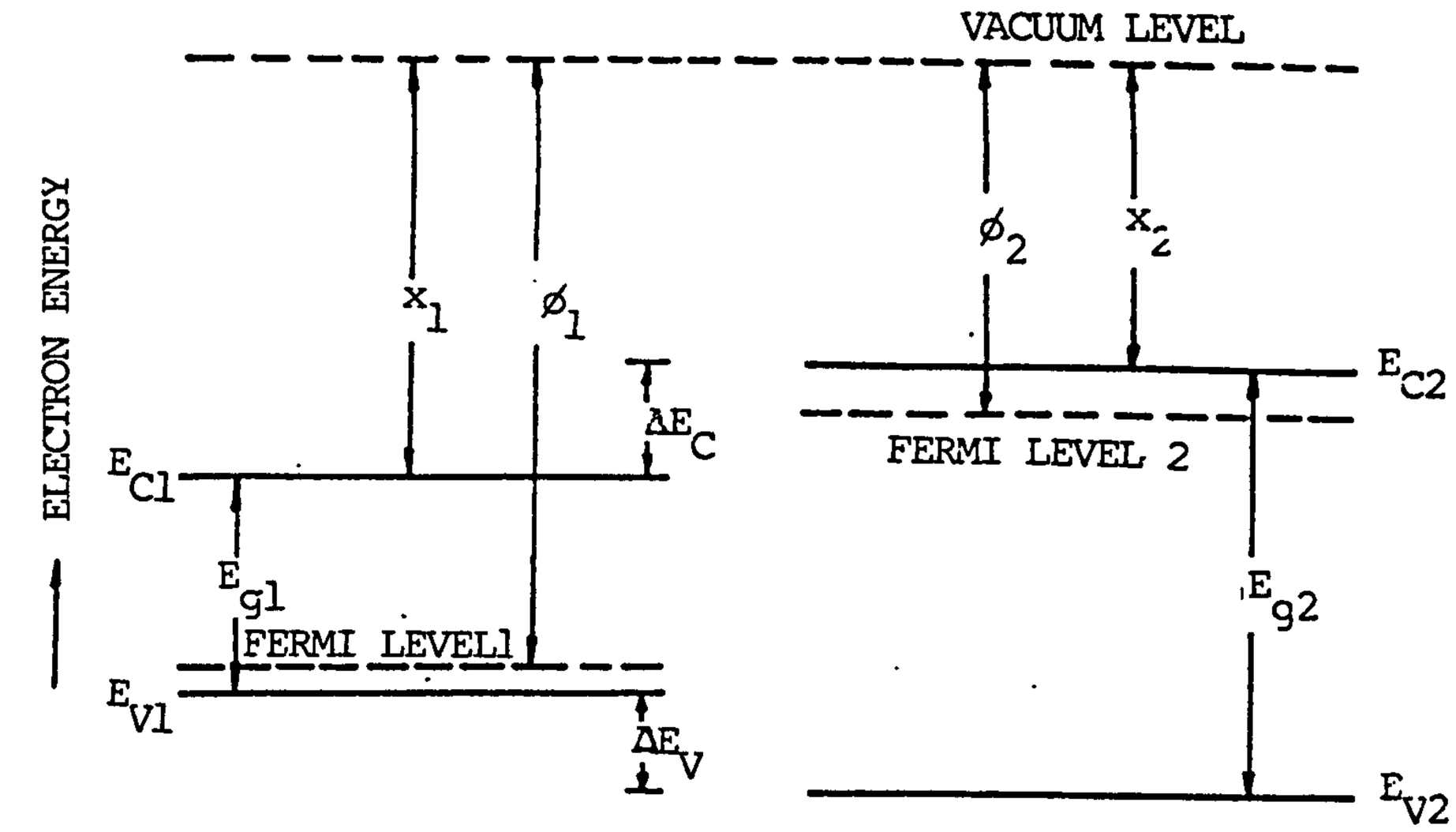


Figure 2.8 (a) Energy Band Diagrams Semiconductors Before the Formation of a Junction

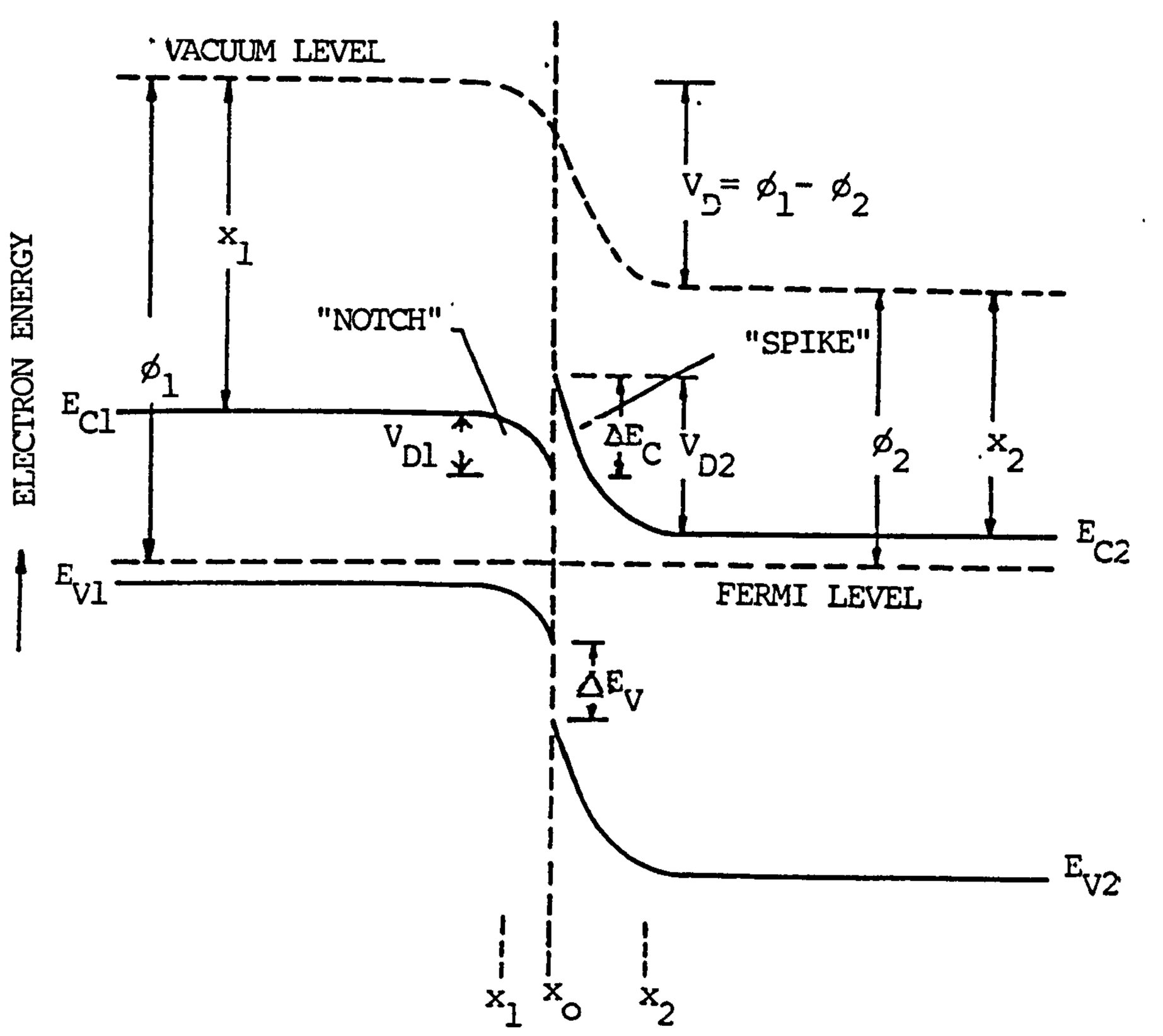


Figure 2.8 (b) Energy Band Diagram of an Anderson Energy Band Profile After Formation of the Junction

$$\delta_1 = (-kT/q)(\ln(N_A/N_V)) \qquad 2.36$$

and $$\delta_2 = (-kT/q)(\ln(N_D/N_C)) \qquad 2.37$$

For non-degenerate semiconductors the maximum value of V_D is hence expected to be given by :-

$$V_{Dmax} = E_{g1}+(X_1-X_2) \qquad 2.38$$

which will correspond to when both the n-type and p-type materials are heavilly doped.

As with homojunctions the transition regions are assumed to be completely depleted over the distances x_1 and x_2 and by charge conservation :-

$$x_1/x_2 = N_D/N_A \qquad 2.39$$

It is apparent that there is a discontinuity in the conduction bandedge, $\blacktriangle E_c$, which arises from the differences in the electron affinities of the materials :-

$$\blacktriangle E_c = X_1-X_2 \qquad 2.40$$

and a discontinuity in the valence bandedge, $\blacktriangle E_v$, which from both the differences in electron affinities and energy bandgap of the two materials :-

$$\blacktriangle E_v = E_{g2}-E_{g1}-\blacktriangle E_c \qquad 2.41$$

For some heterojunction partners these discontinuities may give rise to a "spike" and "notch" in the energy band profile subject to the relative magnitudes of X, E_g and φ [37]. For the heterojunction energy band profile shown in fig.2.9 these do not occur, a consequence of the fact $\varphi 1 > \varphi 2$ and $X_1+E_{g1} > X_2 > X_1$ in this case [37].

By solving Poissons equation on each side of the junction Anderson was also able to derive expressions for the transition region widths on each side of the device, X_1 and X_2, and hence the total transition region width, w:-

$$X_1 = [(2/q)(N_D\epsilon_1\epsilon_2V_D)/N_A(\epsilon_1N_A+\epsilon_2N_D)]^{1/2} \qquad 2.42$$

$$X_2 = [(2/q)(N_A\epsilon_1\epsilon_2V_D)/(N_D(\epsilon_1N_D+\epsilon_2N_D)]^{1/2} \qquad 2.43$$

and $$w = [2\epsilon_1\epsilon_2V_D(N_A+N_D)^2/q(\epsilon_1N_A+\epsilon_2N_2)N_DN_A]^{1/2} \qquad 2.44$$

It should be noted that if $N_D>>N_A$ then the expression for w reduces to :-

$$w = (2\epsilon_1V_D/qN_A)^{1/2} \qquad 2.45$$

which is the same result as that obtained for a n^+-p homojunction [45].

The Anderson model simply ignores the effects of interface states. If a charge density is associated with the interface states then the ideal energy band profile will be changed [37] and values for V_d, w e.t.c.

modified.

2.8 Current Transport Models:

Very good reviews of the possible current trransport mechanisms in anisotypes hetrojunctions are given by Donnely and Milnes [46], Anderson [44], Sharma and Purojhit [47], Milnes and Feucht [48] and others [37]. The major current transport processes are hence discussed only briefly in this section.

2.8.1 The Anderson Model:

Anderson [44] was the first worker to derive the I-V characteristic of a heterojunction device. Because the discontinuities in the conduction band edge and valence band edge lead to potential barriers of very different heights he assumed that the current flow would be dominated by the carriers which encountered the smaller potential barrier. If his model is applied to a heterojunction with the energy band profile of the type shown in fig.2.9 then the forward I-V characteristic will be of the form [37] :-

$$J = J_{00}\exp[-q(\Delta E_c+V_D)/kT][\exp(qV/kT)-1] \quad 2.46$$

where $J_{00} = qXN_D(D_n/\tau_n)^{1/2}$

D_n and τ_n are the diffusion constant and minority carrier lifetime of electrons in the n-type material and X is the "transmission coefficient" for electrons to cross the

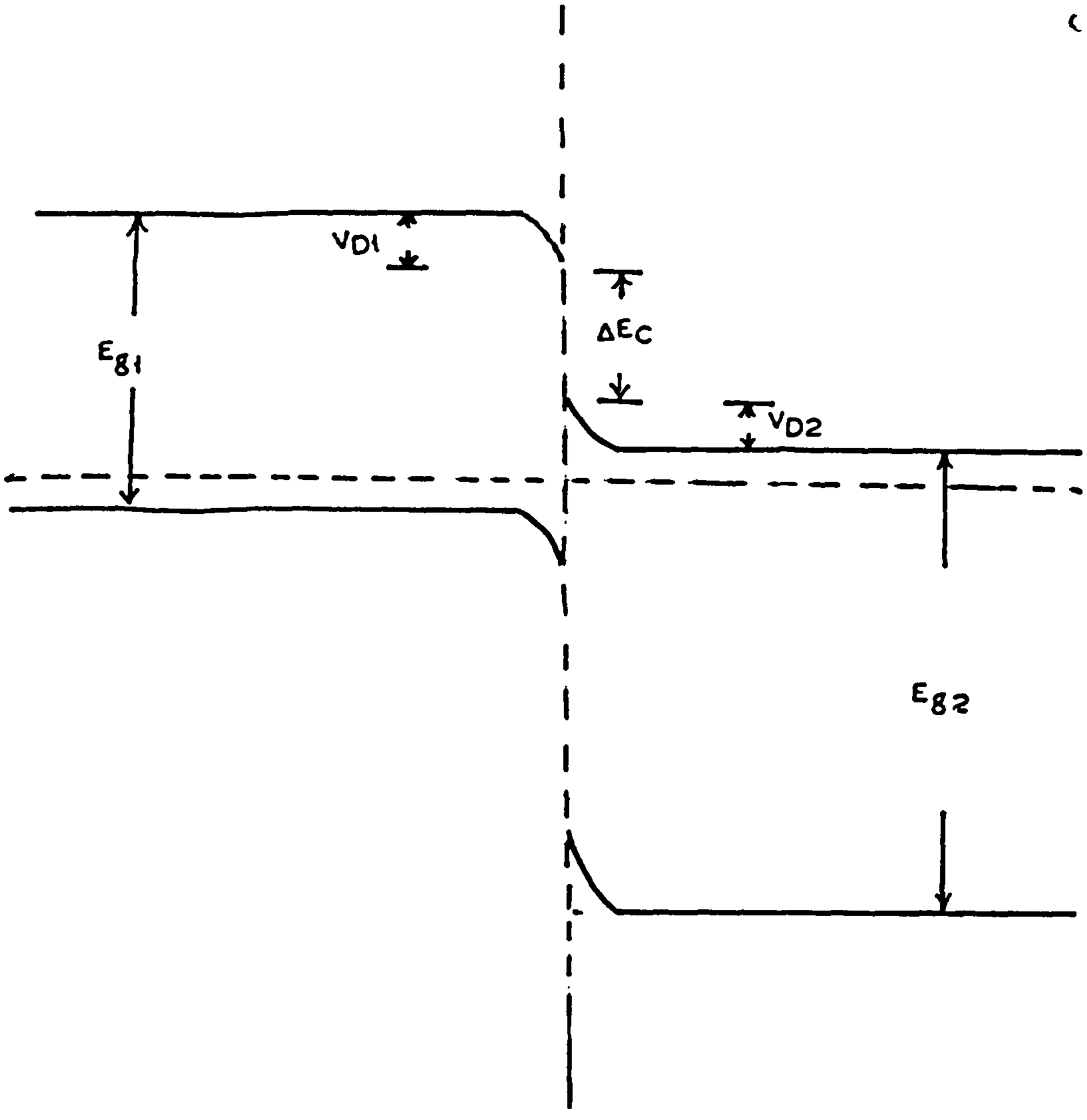


Figure 2.9 Energy Band Profile of Anderson Model Without Formation of the Spike at the Interface

interface. The transmission coefficient, X, was included by Anderson because the derived current density using X=1 was much higher than that empirically observed and he tried to account for the discrepancy by assuming there was a high probability of reflection of carriers at the interface leading to a small value of X. The model also predicted the reverse bias current should increase exponentially with reverse bias voltage and again the X needed to be included if the theoretical current was to be reduced to approach that observed experimentally.

Studies of the current transport in many heterojunction pairs indicate that they do not in general confirm to this current transport model [49].

2.8.2 The Emmission Model of Pearlman and Feucht:

Pearlman and Feucht [46] were able to avoid the need for an improbably small value of transmission coefficient, X, by including the effect of a spike in the conduction band edge as shown in fig.2.10 they assumed that current flow was limited by a homojunction type of operation where a minority carrier build up at the edge of the depletion region limits the current flow, followed by a metal-semiconductor type of operation where the current is limited by the potential barrier in the conduction bandedge.

The forward bias current of behaviour is expected to be given by :-

$$J = J_0[\exp(qV/kT)-1] \qquad 2.47$$

but J_0 differs for the two mechanisms

For low biases, less than some threshold voltage V_T, where the homojunction type behaviour dominates :-

$$J_0 = qN_D(D_n/\tau_n)^{1/2} \qquad 2.48$$

and for $V > V_T$ where the metal-semiconductor behaviour dominates :-

$$J_0 = (1/2)qX_mN_D(2kT/\pi m_n^*)^{1/2}\exp[-q/kT(V_F+V) \qquad 2.49$$

where m_n^* is the electron effective mass in the n-type material, V_F is the "barrier height" and X_m the transmission coefficient. It should be noted that X_m does not need to be as low as in the case of the Anderson model because the predicted value of the J_0 is much lower in this case, for X_m=1 than that obtained using the Anderson model.

This model also predicts that the reverse bias current should increase exponentially with reverse bias voltage [47].

2.8.3 <u>The Tunnelling Model of Rediker, Stopek and Ward</u>:

Rediker et al [50] considered the possibility that quantum mechanical tunnelling through the spike in the conduction band of a p-n hetrojunction could be the current limiting transport mechanism (as shown in fig.2.11). Assuming a parabolic shaped potential barrier

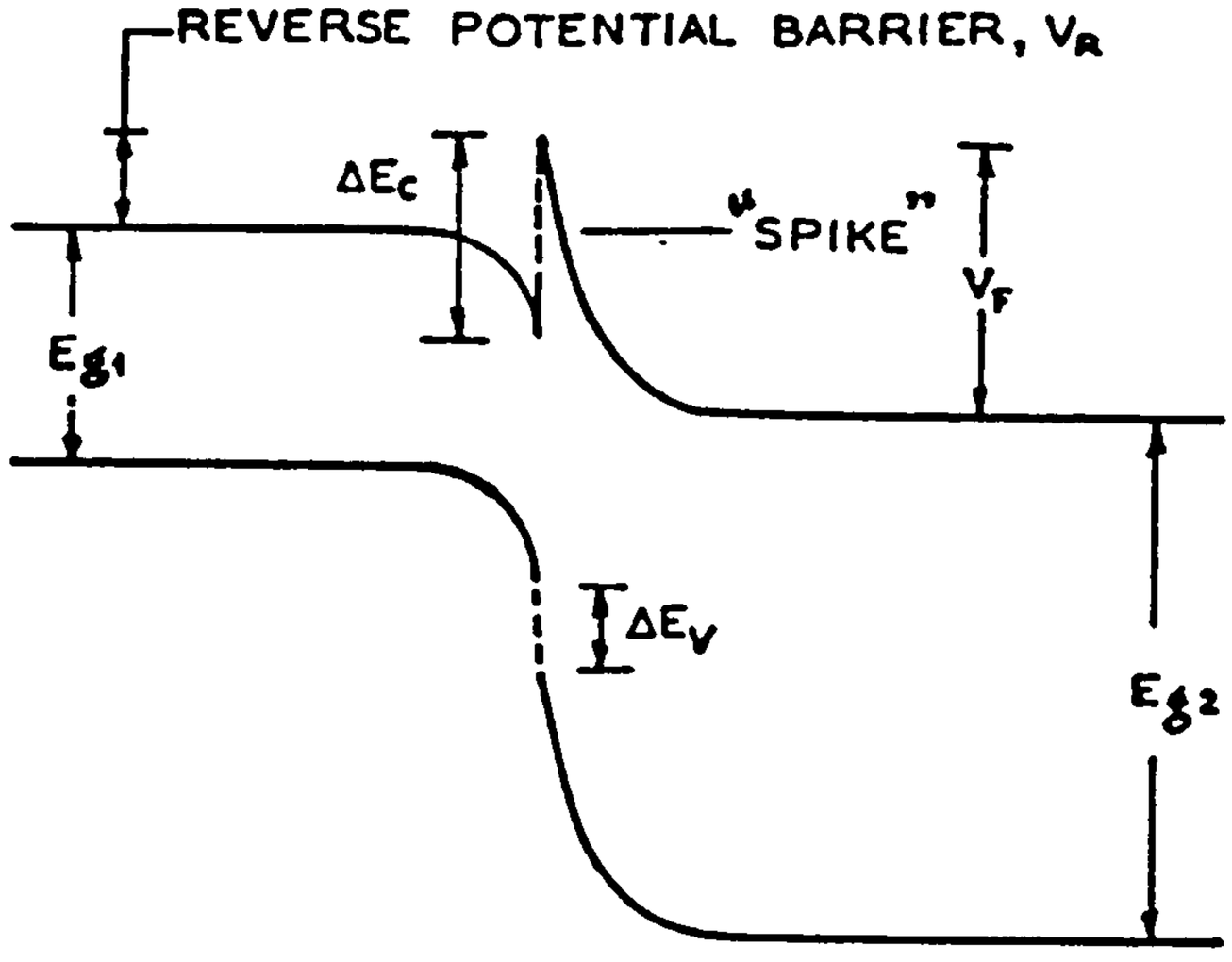


Figure 2.10 Transport Model of Perlman and Feucht

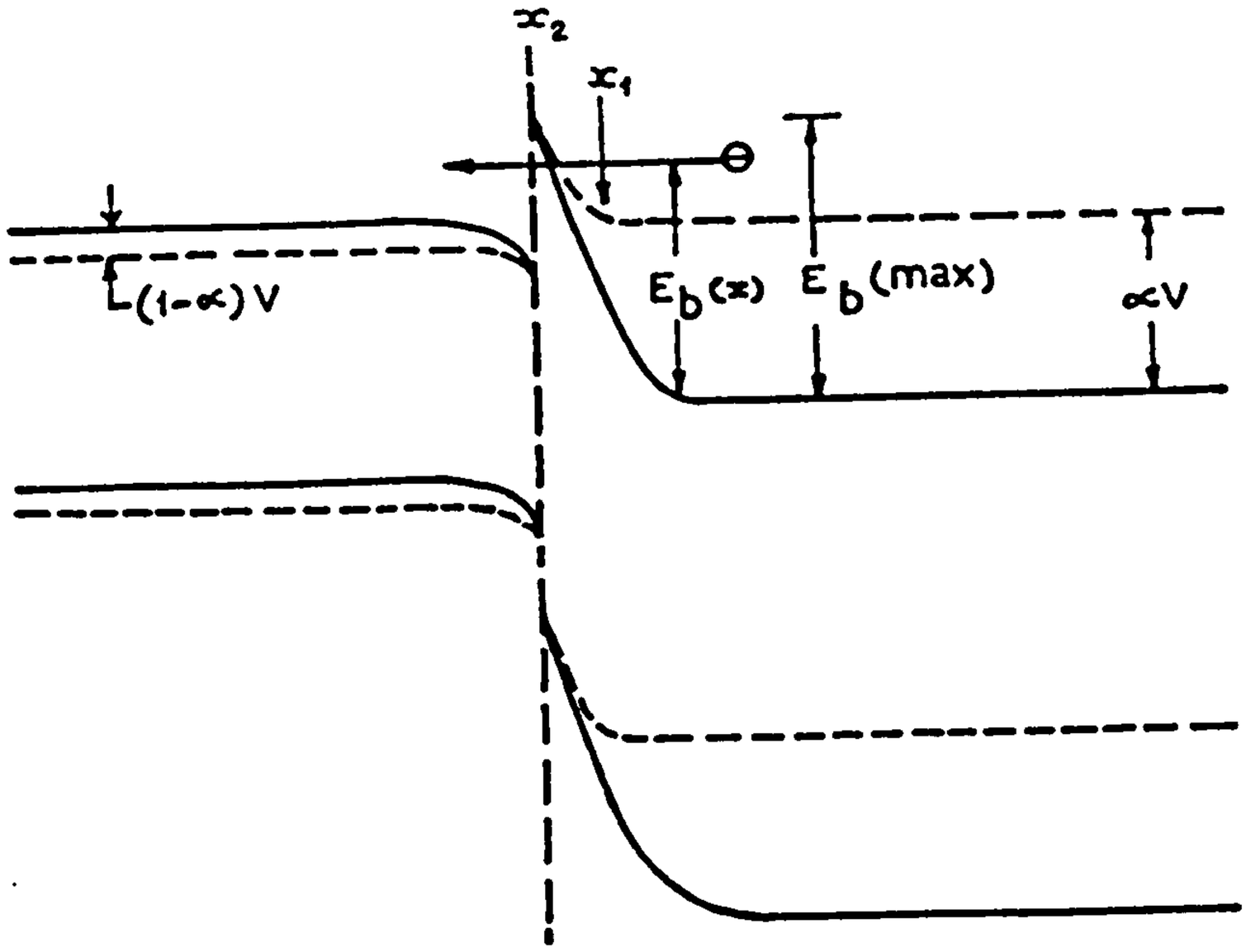


Figure 2.11 Model of Tunnelling Proposed by Rediker, Stopek and Ward

they calculated the tunnelling probability and hence the current flow for forward bias. The forward current was found to be of the form :-

$$J = J_0(T)\exp(V/V_0) \qquad 2.50$$

where V_0 is a constant and $J_0(T)$ varies only weakly with temperature.

Although Rediker et al [50] did not determine the precise temperature dependence of J_0, Newman [51] pointed out that for many heterojunctions, J_0, is found to be proportional to $\exp(T/T_0)$.

Thus the above expression may be rewritten as :-

$$J = J_{00}\exp(T/T_0)\exp(V/V_0) \qquad 2.51$$

where J_{00},T_0 and V_0 are constants.

This expression predicts that V and T are separable variables and that the slopes of the plots of lnJ versus V should be independent of temperature as is observed in many heterojunction devices either for all values of forward bias or for forward biases greater than some critical value, V_T.

2.8.4 Tunnelling-Recombination Model of Riben and Feucht

Another tunnelling mechanism was considered by Riben and Feucht [52]. They considered that electrons could tunnel from the wide bandgap n-type material and holes could tunnel from the narrow bandgap p-type material to

interband states where they could recombine. This process is shown in fig.2.12.

If the tunnelling originates from the bottom of the conduction band or top of the valence band then they predicted a forward current given by :-

$$J = \beta \exp[-\alpha(V_D - V)] \qquad 2.52$$

where β is a weak function of voltage and temperature and α is given by :-

$$\alpha = (8\pi/3h)(m_n^* \epsilon_n / N_D)^{1/2} \qquad 2.53$$

if tunnelling is mainly from the n-type material and

$$\alpha = (8\pi/3h)(m_p^* \epsilon_p / N_A)^{1/2} \qquad 2.54$$

if the tunnelling is mainly from the p-type material. Because the agreement between the theoretical value of α and the value observed experimentally for α are poor, Riben and Feucht [52] also considered the possibility of multistep tunnelling which is also shown in fig.2.12 A particular problem with the latter mechanism is that detailed quantitative calculations are difficult to perform without knowing in detail the distribution of the states within the energy bandgap.

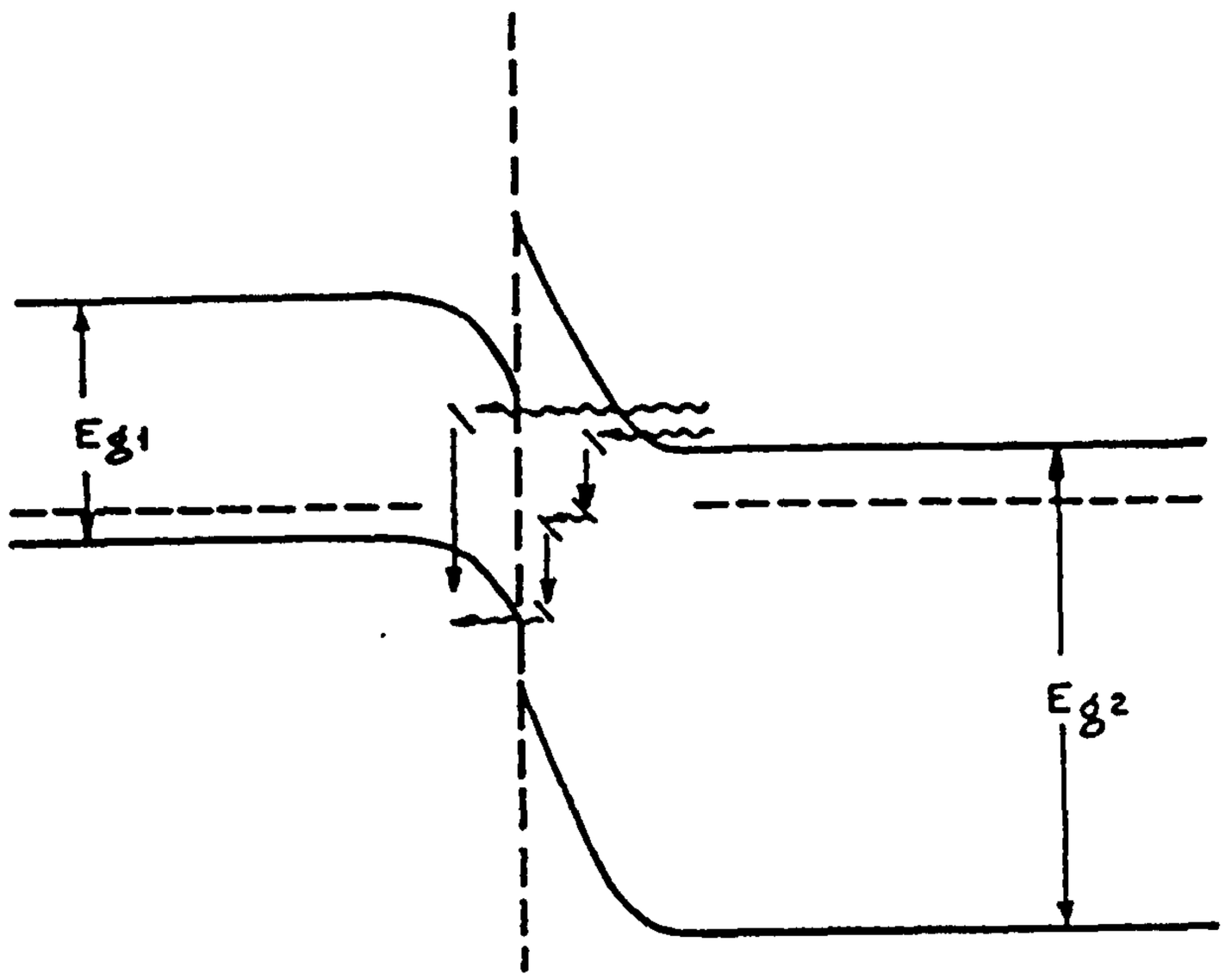


Figure 2.12 Tunnelling-Recombination Model of Riben and Feucht

2.8.5 Tunnelling Recombination Model of Donnelly and Milnes:

Donnelly and Milnes [51] have also considered a tunnelling-Recombination mechanism but they considered that it was recombination at the interface which limited the current flow. They derived the following expression for the current flow :-

$$J = qSN_B\exp(-q\blacktriangle E_0/kT)\exp(qV/AkT) \qquad 2.55$$

where S is the interface recombination velocity, N_B the doping in the base and $\blacktriangle E_0$ the thermal activation energy for the process.

The surface recombination velocity, S, is given by

$$S = V_{th}\sigma N_I \qquad 2.56$$

where V_{th} is thermal velocity of the electrons, σ capture cross-section of the interface states and N_I the density of empty interface states. N_I may be calculated using , $N_I=\blacktriangle a/a^3$ where $\blacktriangle a$ is the difference in lattice constants between the two materials and a is the average lattice constant in the plane of the junction.)

The equation for the J may be rewritten in the form:

$$J = J_{00}\exp(-q\blacktriangle E/kT)\exp(qV/AkT) \qquad 2.57$$

$$= J_{00}\exp(q\blacktriangle E/AkT) \quad \text{where}$$

$$\blacktriangle E = \blacktriangle E_0 - V/A$$

The model may hence be confirmed by determining , $\blacktriangle E_0$ from plots of ln J_0 versus 1/T for various applied biases and then plotting $\blacktriangle E$ versus V.

The slope should then be -1/A (which can be compared to the A obtained from lnJ versus V plots) and the intercept on the $\blacktriangle E$ axis should be $\blacktriangle E_0$. It is also possible to directly compare the theoretical value for J_{00} with that obtained experimentally.

This model has been used by various workers to interpret the behaviour of their devices and it would appear to be the model which best fits the forward characteristics of the CdS/CdTe devices [49].

2.9 Synthesis of Transport Models:

Anderson [44] has classified the forward current flow in anisotype hetrojunctions into two groups : "thermal currents" and "non-thermal currents".

The thermal currents are those in which carriers must surmount a potential barrier prior to crossing the junction and it is the surmounting of the barrier which limits the current flow. The forward characteristics are hence given by :-

$$J = J_{00}\exp(-\varphi/kT)\exp(qV/AkT) \qquad 2.58$$

where φ is the barrier height / activation energy for the process and J_{00} is a constant which depends on the current flow mechanism.

It should be noted that the Anderson diffusion model, the

emission model of Pearlman and Feucht [47], the interface recombination model of Dolega [54] and the tunnelling-recombination model of Donnely and Milnes [53] predict a forward current which fits this general equation.

The non-thermal currents do not obey the above relationship i.e. J_0 is not proportional to $\exp(-\varphi/kT)$. J_0 is either weakly temperature dependent or $J_0 \alpha \exp(T/T_0)$ and hence tunnelling through a spike or tunnelling to the interface states dominates the current flow. The tunnelling models of Rediker et [55] and Riben and Feucht [52] hence predict forward currents which are "non-thermal" in nature.

It is of course possible that the current mechanism may change from thermal to non-thermal or vice-versa for different bias or temperature regimes.

2.10 Capacitance-Voltage Characteristic:

Anderson was the first worker to derive an expression for the junction capacitance, by ignoring the presence of interface states and by simply extending the method used for the derivation of homojunction capacitance. His expression for the junction capacitance per unit area can be written as :-

$$C = [q\epsilon_n\epsilon_p N_D N_A/2(\epsilon_n N_D+\epsilon N_A)][(V_D-V)^{-1/2}] \qquad 2.59$$

$N_D$and N_A are the donor and acceptor concentrations, ϵ_n and ϵ_p the dielectric constants in the n-type and p-type material respectively, V_d is the built-in voltage and V

the applied voltage.

A plot of C^{-2} versus reverse bias voltage, V should be a straight line with an intercept on the voltage axis equal to V_D. Various workers have found that plots of C^{-2}versus V are straight lines for their heterojunction devices and they have used the above formula to determine V_D [19,56]. For heterojunctions formed between semiconductors with small lattice mismatchs < 1% the agreement between the V_D measured and the V_D calculated from the ideal band profile is satisfactory implying that interface states may be ignored in these devices.

The C-V measurements made for the anisotype hetrojunctions fabricated by Donnelly and Milnes [57], with lattice mismatch of greater than 4%, however indicated that interface states could not be ignored in these devices and they have derived a theoretical expression for the junction capacitance taking interface states into account. Assuming that interface states are localised in infinitesimally thin sheets at the metallurgical interface and including dipole effects they derived the following expression :-

$$C = B_1[1+f(V)dQ_{IS}/dV+d\varphi_m/dV]*[V_D-V-\varphi_m-B_2Q_{IS}^2)^{-1/2} \qquad 2.60$$

where $f(V) = 2B_2Q_{IS}+2(B_2\epsilon_nN_D/\epsilon_pN_A)^{1/2}(V_D-V-\varphi_m-B_2Q_{IS}^2)$

and $B_1 = [q\epsilon_n\epsilon_pN_AN_D/2(\epsilon_nN_D+\epsilon_pN_A)]^{1/2}$

and $B_2 = [2Q(\epsilon nN_D+\epsilon pN_A)]^{-1}$

Q_{IS} is the net charge on the interface states and $\varphi_m$is

the net charge on the electric dipole. The presence of an electric dipole at the heterojunction interface due to interface states being distributed on the either side of the junction was first postulated by Van Ruyven [58].

If the net charge on the interface states is independent of applied voltage and an electric dipole is not present then the equation may be written as :-

$$C = [q\epsilon_n\epsilon_p N_D N_A/2(\epsilon_N N_D+\epsilon_p N_A)]^{1/2}(V_D-V-B_2Q_{IS}{}^2)^{-1/2} \qquad 2.61$$

This equation shows that a plot of C^{-2}versus V should be a straight line but now the intercept on voltage axis is $(V_D-B_2Q_{IS}{}^2)$ instead of V_D. This model hence plausibly accounts for why the V_D determined from C-V measurement may differ from that theoretically determined using the Anderson model when C^{-2} versus V plots are observed to be straight lines. It should be noted that irrespective of whether the interface states are positively or negatively charged, $Q_{IS}{}^2$ is positive and hence the effect of the charged interface states is to reduce the measured diffusion voltage. For some devices [49] the diffusion voltage determined from C-V measurements is greater than that expected Anderson model and the only way to account for this is the assume that φ_m is negative and larger than $B_2Q_{IS}{}^2$ so as to increase V_D[49].

The capacitance of heterojunctions and in fact homojunctions, is often observed to decrease as the measurement frequency is increased. For homojunction the decrease has been shown to be due to the inability of

deep impurity centres to follow the frequency as it is increased [9]. For heterojunctions the capacitance variation with frequency is expected to be dominated by the inability of interface states to follow the frequency as it is increased and hence such measurements give information regarding the density of interface states present in the device [59].

2.11 Polycrystalline Thin Films:

Thin films of semiconductors deposited using low cost methods onto low cost substrates are found to be polycrystalline i.e. to consist of small crystallites separated by the grain boundaries.The grain boundaries are regions of increased disorder containing both structural defects and segregated impurities in large densities [60]. They are usually considered to be the regions where recombination is enhanced and there may hence be considerable loss of photo generated carriers in their vicinity. Charge trapping at grain boundaries may also form potential barriers which impede carrier transport [60].

The model most often used to take into account the role of grain boundaries in electrical conduction is the Petritz barrier model [61] which considers that the conductivity of the grains is much greater than that of intergrain regions.

It is assumed that such high resistivity grain boundaries are due to the formation of the depletion regions associated with the electrical barrier, φ_B,

between the grains. The current flow is assumed to be limited by thermionic emission of carriers over the barrier and the "thermally activated" carrier mobility given by :-

$$\mu = \mu_o \exp(-\varphi_m/kT) \qquad 2.62$$

where φ_m is the barrier height, and μ_o is given by :-

$$\mu_o = Yq V_{th}/4kT \qquad 2.63$$

where Y is the average diameter of the grains and V_{th} is the thermal velocity of the carriers.

Snejdor and Jerhot [62-64] have extended this model and considered that current transport can occur across the intergrain barrier by either thermionic emission, tunnelling or by ohmic conduction. They assumed that the grain boundaries could be treat as heterojunctions and related the physical parameters affecting the conductivity to elements in an equivalent electrical resistance network. According to this model when thermionic emission is dominant the conductivity is given by :-

$$\sigma = \sigma_o \exp(-q\varphi_m/kT) \qquad 2.64$$

where $\sigma_o = q^2 n_g V_{th}/4N_G kT$

V_{th} is the thermal velocity of carriers within the grains and N_G is the number of grains encountered along the current path.

The grain boundary barrier height, φ_m, (or thermal

activation energy) is given by :-

$$\varphi_m = kT/q \ln(n_g/n_b) \qquad 2.65$$

where n_g and n_b are the electron densities in the grain and in the grain boundary regions respectively.

The height of the potential barrier and the width of the depletion layer at the grain boundaries hence depend of the carrier densities in the grain and the intergrain regions.

The distribution of charge traps, impurities and defects and hence donor or acceptor concentrations near the grain boundaries will depend critically on the deposition parameters used [8].

It is found that many semiconductors can be deposited such that they consist of "columnar grains" (see fig.2.13) rather than randomly orientated grains if the deposition conditions are suitably optimised. Such a grain structure has the advantage that minority carriers may travel through the material without crossing the grain boundaries because the charge density at the grain boundary may be such that the grain boundaries repel the minority carriers so confining them within the grains [5,9]. Although the effective area through which carrier move is reduced and "surface scattering" will reduce the mobility of the carriers within the grain [55,66] compared to that in single crystal material the mobility reduction and minority carrier diffusion length reduction will not as severe as in the polycrystalline material

consisting of randomly, orientated grains.

For solar cell applications the polycrystalline material used hence always consists of columnar grains.

As shown in fig.2.14 there is also a correlation between the solar cell efficiency achieved and the grain size of the absorber material used [67].

The aim in producing efficient solar cells is hence to optimise the fabrication condition of the absorber layer to produce columnar grains which are as large as possible.

2.12 Requirements of the Absorber layer:

(a) Photon absorbing material should have direct bandgaps within the range 1.0 to 1.7 eV. A small energybandgap will ensure a high photo-current but will produce a low diffusion voltage and consequently a low open circuit voltage whereas a large energy bandgaps results in a high open circuit voltage but a low short-circuit current. Because the cell efficiency is proportional to the power output, there is an optimum value of energy bandgap which has been shown to be be 1.5eV [68].

(b) Absorber materials should have a large absorption coefficient, which results from an interband transition [19]. Because the necessary absorption thickness should be > $1/\alpha$, large absorption co-efficients permit the absorber layer to be thin (i.e. photons are absorbed

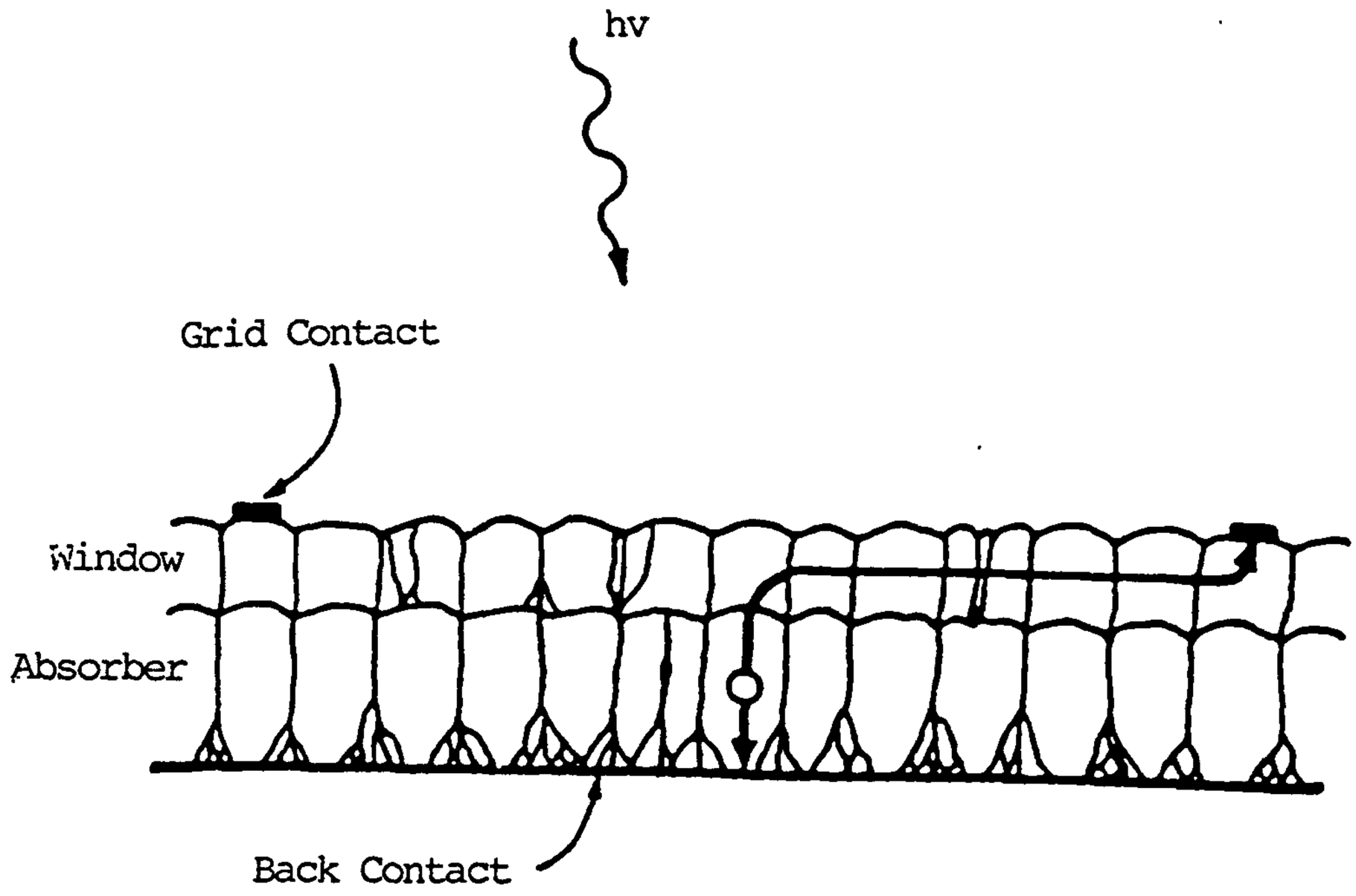


Fig.2.13 A Cross-sectional View of a Polycrystalline Thin Film Hetrojunction Showing the Grains of the Window and Absorber Layers

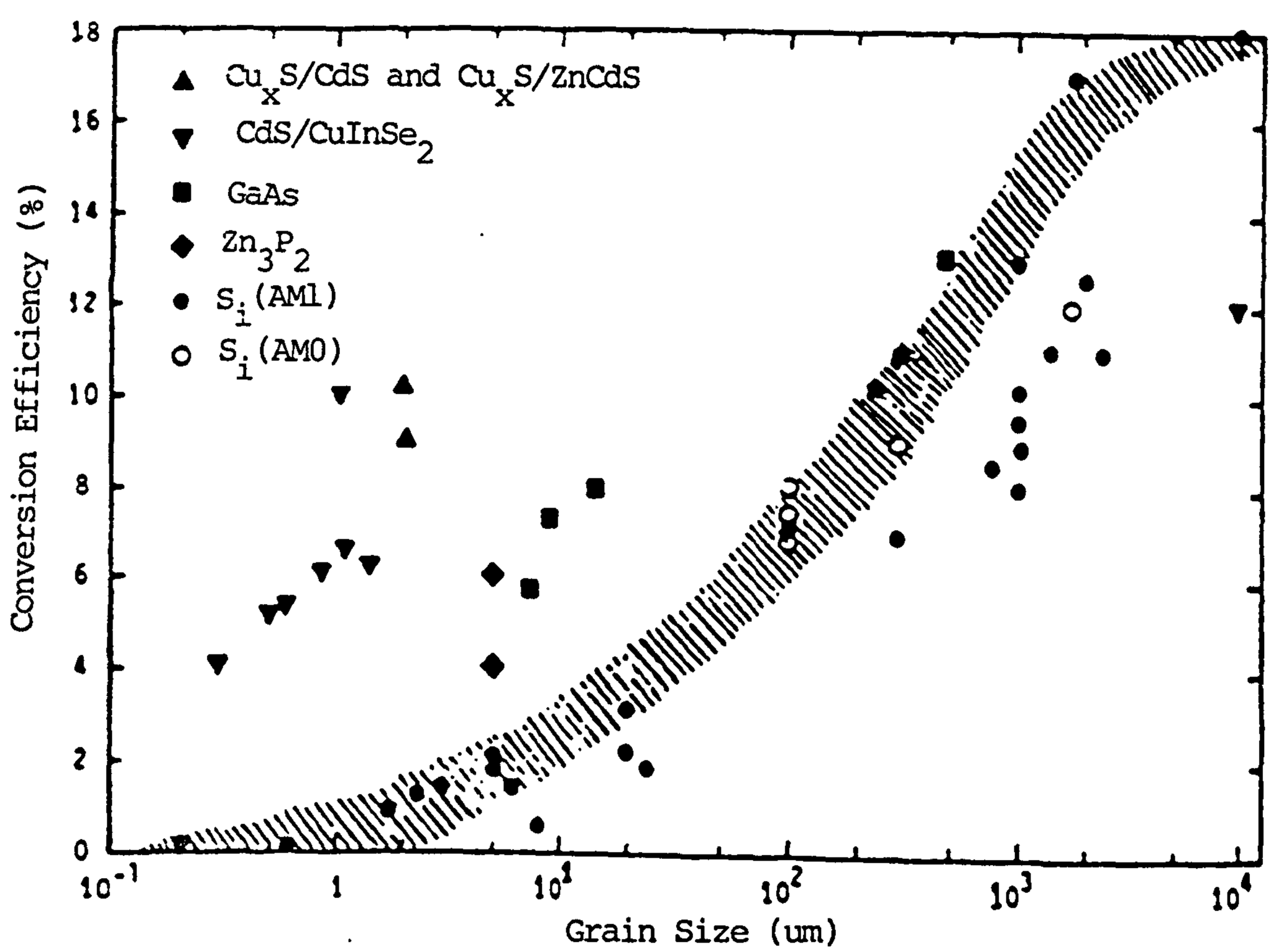


Fig.2.14 The Relation of Solar Conversion Efficiency to Grain Size for Polycrystalline Thin Films

nearer the junction interface). As a result, less material is required for solar cell fabrication, which has a positive implication on device cost. The requirement that α should be as large as possible means that direct bandgap materials e.g. CdTe are preferred rather than indirect bandgap materials e.g. Si.

(c) The photogenerated carriers in the absorber semiconductor must be able to move across that region to the junction region of the solar cell. The carriers which recombine before arriving at the junction are lost and cannot take part in the generation of J_L. Diffusion is the mechanism with which the minority carriers move to the depletion region and therefore, the minority carrier diffusion length is the most important material parameter. In general the diffusion length should be greater than $1/\alpha$ to ensure the excess minority carriers reach the junction without excessive losses due to recombination. The diffusion length can be expressed in terms of the basic material parameters :- $L_{n,m}=[(kT)\mu_{n,p}\tau_{n,p}]$ i.e. for the diffusion length to be as large as possible, the mobility, $\mu_{n,p}$ and the life time $\tau_{n,p}$ of the minority carriers should be as large as possible.

Grain boundaries are surfaces when the recombination of the minority carriers is enhanced and to avoid such recombination polycrystalline material with large columnar grains is desired. It should be noted that the minority carrier diffusion length of electrons is always greater than that of holes and so in general p-type

absorber layers are used rather than n-type.

(d) In photovoltaic devices, surfaces with high recombination velocities are in competition with the junction (depletion) region for collection of photogenerated carriers. This high recombination is due to the presence of surface states, that result from dangling bonds, native oxides, metallic precipitates, organic precipitates, chemical residues and crystal defects. For an illuminated solar cell, the number of photogenerated carriers is highest at the surface and decreases exponentially into the material. Thus the surface recombination velocity is a critical parameter especially in direct bandgap semiconductors close to the surface. Different etchant treatments can be used to minimise these losses. It is desirable to passivate photovoltaic material surfaces in order to keep the surface recombination velocity low.

(e) A high absorber layer resistivity results in a high device series resistance and, as a consequence, a drop in power. Thus it must be possible to dope the material to a high enough value to minimise such losses in power. In silicon solar cells series resistances of 0, 1, 2, 5,or 10Ω reduce the available power to 1, 0.77, 0.57, 0.27, or 0.14 respectively [4]. For CdTe thin film solar cells with thickness of 1.5μm a CdTe resistivity < 6000 Ω-cm is desired to reduce the series resistance to < 1 Ω-cm (for a small area cell).

(f) External contacts to the absorber layer must be ohmic, i.e. of sufficiently low resistance to the

semiconductor that they do not significantly perturb the device performance. In particular for a typical solar cell, contact resistances < $0.1\Omega/cm^2$ are desired [4].

2.13 Window Layer Requirements

(a) The energy bandgap of the window layer should be sufficiently high to allow most of the incident radiation to be transmitted to the absorber layer. Materials with bandgaps 4.0 eV > E_g > 2.2 eV are commonly used.

(b) A low value of window layer resistivity is essential to reduce the device series resistance which would if too large would decrease the power output of the cell. Large bandgap materials are usually highly resistive and in practice only a few material can be made with low resistivities. CdS, ITO and ZnO are three materials which have proved to be successful.

(c) In order to construct an Anderson energy band model of the heterojunction [44] it is necessary to know the electron affinities of the materials to be used in forming the heterojunction. This knowledge allows a choice of materials that will not have obvious spike in the conduction band or valence band that will limit the collection of photogenerated current.

A reduction in $V_{o.c}$ will occur if the electron affinity of the window layer is greater than the absorber layer and a reduction of $I_{s.c}$ will occur if the electron affinity of the absorber layer is greater than that of window layer. There should be a minimum mismatch so that "spikes" and "notches" are not present in the energy band

profile [37].

(d) A perfect window layer/absorber layer interface will contain no recombination centres. In practice there is always a degree of lattice mismatch which results in interface strain and dislocations. A high lattice mismatch will reduce the efficiency of the device because the increase of misfit dislocation density will increase carrier recombination at the interface because they act as recombination centres.

(e) The window layer should be composed of large crystallities with good crystallinity. This will ensure the formation of a good p-n junction with the absorber layer and reduce the density of short circuit paths through the junction. Good window layer crystallinity may augment the efficiency of the device due to the generation of the excess carriers near to the junction.

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CHAPTER III

LITERATURE REVIEW

3.1 Historical Development of CdS/CdTe Solar Cells

Cadmium Telluride was first synthesized in 1879 when it was produced by the French scientist Margottet during his investigation of the reactivity of tellurium with metals. Fibre [1] also reported in 1888 the formation of well crystallized cadmium telluride and Tebbals ,1889 [2] reported that cadmium telluride was synthesized successfully during his investigation of the formation of tellurides.

The material found some use in pigments [3] but it was not until 1947 when it was grown by Frerichs [4,5] in single crystal form using the vapour phase reaction of cadmium and tellurium in the presence of hydrogen that its potential as a semiconductor was more extensively investigated. Cadmium telluride photoconductive devices were made in 1948 [6,7] and it was found that heat treatments strongly influenced the performance of such devices. Detailed investigations of the electronic properties of single crystal CdTe were made in the 1950,s [8-10] and later detailed doping studies were made by Kroeger and de Nobel [11] and by Boltaks, Konorov and Matveev [12]. In 1957 Loferski [13] theoretically determined the optimum energy bandgap for a semiconductor to be used in a p-n junction solar cell to be 1.5 eV and CdTe was immediately recognised to be one of the few semiconductors with an energy bandgap close to this

value.

In 1959 [14] de'Nobel and Kroeger discussed the importance of CdTe, in particular that different to the other II-IV compounds CdTe was amphoteric i.e. it could be made both n-type and p-type and hence it was possible to produce semiconductor devices such as diodes or transistors using this material. CdTe also had potential to be used for X-ray and nuclear particle detection, and for a range of electro-optical devices including solar cells.

The first effort for producing a high efficiency thin film solar cell was reported by Cusano [15,16] in 1963. A low resistivity n-type, iodine doped, cadmium telluride film was prepared by the vapour phase reaction of Cd and Te on a heated substrate and a p-type Cu_2Te thin film, with an energy bandgap 1.04 eV, was grown chemically on top of the CdTe layer. These cells were prepared on an industrial basis; they had an area of 40 cm^2, an open circuit voltage 0.58 V, a short circuit current, 14 mA/cm^2 and an efficiency of 5 % [17]. It was however discovered that such devices suffered from poor stability due to the diffusion of copper from the Cu_2Te into the n-type CdTe [18]. It was also found that oxygen and moisture strongly affected the properties of Cu_2Te which in turn also deteriorated the cell performance (Cusano, [19] ; Justi et al, [20]; Lebrun, [21]; Guilian et al; [22].

The problems associated with the poor stability of Cu_2Te/CdTe device lead Stanley [23] to consider a

radically different device structure - the n-CdS/p-CdTe heterojunction solar cell. Cadmium sulphide was considered to be a promising junction partner for p-type CdTe because the higher electron affinity ensured "spikes" and "notches" at the heterojunction interface would be avoided (X_{CdS} = 4.5 eV and X_{CdTe} = 4.28 eV [24]), CdS had an energy bandgap 0.9 eV higher than CdTe permitting a large proportion of photons from the solar spectrum to reach the heterojunction interface and further low resistivity CdS was found to be relatively easy to produce.

Reservations regarding the performance of such a device were the lower minority lifetime in p-type CdTe compared to the n-type CdTe and the substantial lattice mismatch of CdS and CdTe (9.7%) which could give rise to high densities of misfit dislocations at the interface which could enhance interfacial recombination. It was however pointed out by [25] that the higher electron mobility in n-type CdTe was sufficient to make the minority carrier diffusion length in n and p-type material comparable. The problem of how badly the lattice mismatch would effect device performance could only be determined by empirical studies.

The first thin film solar cell based on this structure, CdTe/CdS, was fabricated by Adirovich who reported an efficiency of 1 % [26]. This very first cell had the "superstrate configuration" in which an undoped CdTe thin film was evaporated onto a CdS/Sno_2/glass substrate. It is interesting that the highest efficiency solar cells

currently produced also use this structure.

A significant advance was made in 1972 when Bonnet et al [27] at the Battle Institute in Frankfurt produced devices with efficiencies in the range 5-6 % by using close spaced sublimation (C.S.S) to deposit the CdTe onto CdS/SnO_2/glass substrates [27]. Although the cell area for these 5-6 % efficient devices was small, the devices were found to be stable and the respectable efficiencies achieved indicated that the interface states due to lattice mismatch were probably not going to limit device efficiency.

Further studies using single crystal CdTe [28] and using the CdTe produced using thin film techniques e.g screen printing [29,30] and sputtering [31,32] confirmed that efficiencies > 5 % and as high as 12 % could be achieved.

A summary of some of the key achievements in terms of cell efficiency made in the 1970,s to confirm the viability of the CdS/CdTe cell are given in table 3.1.

Following these promising achievements, work in the 1980,s and 1990,s has mainly concentrated on electrodeposition, screen printing, C.S.S. and spray pyrolysis with the objectives of producing low cost devices with higher values of efficiency. Detailed measurements on the properties of the CdTe and CdTe/CdS cells produced using these methods as well as more advanced (yet non-eoconomoic) methods of growth e.g. M.B.E., M.O.C.V.D. and A.L.E. have resulted in a more

TABLE 3.1

Serial No.	Method of Deposition	Investigators	Ref.	Voc (V)	Isc (mA/cm^2)	F.F.	η (%)	Junction Type	Brief Comments
1	Vacuum Deposition	Cusano (1963)	16	0.5	Iligh	0.45-0.60	6.0	Cu_2Te/CdTe (Heterojunction)	Cu_2Te was deposited by chemical method. N-type CdTe was prepared by the reaction of Cd, CdI, and Te (Indium doped CdTe).
2	Single Crystal (Bridgman method).	Cusano (1963)		0.7	Low	.0.70	7.0	Cu_2Te/CdTe (Heterojunction)	CdTe was prepared by Bridgman method. Cu_2Te was chemically deposited.
3	Vacuum Evaporation (CdS) Bridgman Method (CdTe)	Yamaguchi et al (1975, 1976)	24	0.67	18.4	0.60	10.5-12.0	In:CdS/p-CdTe (Buried Homojunction)	Phosphorous doped CdTe was prepared by Bridgeman method. CdS was vacuum evaporated. Ni contact to CdTe, In-Ga contact toCdS.
4	V.P.E. (Vapour Phase Epitaxy)			0.67	20.1	0.59	10.5	In:CdS/ p-CdTe (Buried Homojunction)	CdTe was prepared by V.P.E.
5	Screen Printing (0.36 cm^2 area)	Nakayama et al (1976)	25	0.67	14.2	0.58	8.2	Glass/ In_2O/ CdS/CdTe/ Cu_2Te ($n^{++}n^+n$/ p p^+)	Buried Homojunction. The position of the junction was determined by EBIC measurement.
6	Screen Printing (10.0 cm^2 area)	Nakayama et al (1976)		0.73	11.4	0.51	6.3	Glass/ In_2O/CdS/ CdTe/ Cu doped carbon paste (Buried)	At higher temperatures, Cu diffuses into CdS and deteriorates the cell stability and efficiency, but carbon dopes p-type and makes better contact.
7	Vacuum Evaporation	Adiovich et al (1969,1971)	32				1.0	Glass/ ITO/CdS/ CdTe/ contact	True heterojunction. Theoretical efficiency of this device ≈15% and further, no spike exists at the interface.
8	C.S.V.T. (Vacuum evaporation)	A.L. Fahrenbruch et al (1974, 1975)	33				4.0		
9	Vacuum Evaporation CdS on single crystal CdTs	Mitchell et al (1977)	34	0.63	16.1	0.66	8.0	n-p	True Heterojunction
10	C.V.D. (Chemical Vapour Deposition)	Bonnet and Robenhorst (1974, 1975)	23	0.5	15.0	0.45	5.0-6.0	n-p CdS/CdTe	Cell is even stable at higher temperatures.
11	Sputtering of ITO onto single crystal CdTe.		34	0.82	14.5	0.55	8.0	ITO/ CdTe (n^+n p)	Buried Homojunction due to diffusion of In into CdTe during evaporation.

detailed understanding of the electronic properties of CdTe and of the CdS/CdTe heterojunction.

3.2 Screen Printing :

This technique has been used since 1975 by Matsushita Inc. to produce CdS/CdTe solar cells. Currently efficiencies more than 12 % have been achieved for small cell area cells and efficiencies ≈ 10% for large area modules (30*40) cm^2 [36]. In this process a paste is obtained by mixing CdS powder with 9 % wt of $CdCl_2$ (flux) and an appropriate amount of propylene glycol as a binder and then the mixture screen printed onto borosilicate glass. The sample is dried at 120 °C for 1hr and then sintered in a N_2atmosphere at 690 °C for 90 mins [37]. In this way layers about 30 μm thick with grain sizes ≈ 20-30 μm and with the sheet resistivities ≈ 100 Ω/• are produced.

A paste consisting of a nearly equimolar ratio of Cd and Te mixed with $CdCl_2$ (0.5 wt %) and propylene glycol is then screen printed onto the CdS layer. After drying the samples are then sintered in a N_2 atmosphere at 600-700 °C for an hour to form large grain size CdTe film and to drive off excess material. The thickness of CdTe obtained by this process is typically 5-10 μm. To form an ohmic contact to the CdTe a carbon paste containing a small amount of Cu (about 50-100 ppm) is commonly used. It is mixed with an organic binder, screen printed onto the CdTe and the sample then heated at about 400 °C for 30 minutes in a nitrogen atmosphere containg 1.0 - 1.5 mol %

O_2 [38,39]. A silver paste is screen printed on the top of the carbon paste to reduce the series resistance and a (Ag + In) "dot" electrode is screen printed on the top of CdS film to form a contact.

The addition of copper in the Carbon past has been found to improve the device efficiency [38,39]. This increase is due to an increase of $V_{o.c}$ and F.F and a decrease in R_s and the diode factor. There is an optimum concentration of Cu in the carbon paste and an optimum annealing temperature to make the CdTe layer p+_type to lower the contact resistance through the diffusion of copper into the CdTe.

It should be noted that the presence of $CdCl_2$, O_2 and Cu are considered to be essential for producing high efficiency devices [38-42].

It has been found that the CdS/CdTe cells produced by sintering at high temperatures > 650 °C have a degraded a spectral response for λ less than 700nm and this has been interpreted by assuming the formation of a CdS_xTe_{1-x} solid solution layer at the CdS/CdTe interface [43,44]. This layer has a smaller energy bandgap than CdS and thus absorbs the photons with wavelengths less than 640 nm.

The distribution of S and Te near the junction have been observed by (X.M.A) X-ray microprobe analysis and it confirmed that the CdS_xTe_{1-x} layer is indeed formed for sintering temperatures > 650 °C.

It was also observed that the long wavelength fall-off of the spectral response for the screen printed solar cells was shifted 35-40 nm towards longer wavelengths compared

to the fall-off observed for single crystal CdS/CdTe solar cells [45] compared with the electrodeposited solar cells [46]. This shift introduced a gain in the short circuit current of 13 % under A.m.1.5 illumination. Burgleman et al [47] attribute this behaviour to the presence CdS/CdTe two different phases of CdS_xTe_{1-x} at the CdS/CdTe interface; one $CdS_{1-x}Te_x$ phase formed in the CdS layer is responsible for the deterioration of the short wavelength response and other slowly graded $CdTe_{1-y}S_y$ phase is responsible for the shift in the long wavelength fall-off.

The photocurrent observed in the CdTe solar cells annealed at temperatures > 660 °C was less bias dependent under illumination then in the dark which was probably due to the stabilization of the interface states at the grain boundaries when illuminated [48].

Further it was found that the collection efficiency of the cells annealed at temperatures > 660 °C were less bias dependent than those of the cells annealed at lower temperatures. Such behaviour is observed if the junction is shallow and the diffusion length in the base region is large compared to the average light penetration depth. From EBIC measurements it was found that the cell annealed at the higher temperatures had a minority carrier diffusion length of 1 μm compared to 0.76 μm for the unannealed cell. It was therefore concluded that the less bias dependent spectral response and the improved diffusion length of the CdTe cells annealed at higher temperature was due to the improvement of the

crystallinity of the CdTe active layer.

The quality of the CdS/CdTe interface is also considered to be improved by the presence of the CdS_xTe_{1-x} phases which reudce the strain at the interface.

Too much $CdCl_2$ was found to be detrimental to device performance because it was found to degrade the grain structure at the interface. High quality cells were found to be produced by reducing the $CdCl_2$ content in the CdS paste to 0.05 % and increasing the sintering temperature to 680 °C. The highest efficiency obtained for a small area cell, 1.07 cm^2, was 11.3 %, [$V_{O.C} \approx 797$ mV, J_{SC} = 21.1 mA/cm^2, and FF = 0.67] [48].

The cost to produce a 7-μm thick layer of CdTe, 1m^2 in area has been estimated to be about $ 8.5/peak watt [50], which is high compared to the alternate method discussed .

Matsushita do not use a T.C.O. layer such as SnO_2, in their structure but instead use thick CdS. To further avoid the series resistance losses many cells about 6mm wide are used. They have considered that fewer and wider strip cells can be used if the SnO_2 was introduced in the structure but this would lower the processing temperature to less than 625 °C, too low a temperature to produce the most efficient cells [49].

3.3 Electrodeposition:

In 1976 Monosolar Incorporated in conjunction with the University of Southern California initiated research on the cathodic deposition of CdTe for solar cell

applications [50,51]. The initial aim was to produce a Schottky barrier device based on the structure Au/n-CdTe/I.T.O/glass. Bassol et al 1982 achieved a conversion efficiency ≈ 6% [52] by depositing a thin layer (≈ 500 °A) of CdS onto I.T.O coated glass prior to CdTe deposition (0.8μm) and then annealed the device at 250 °C - 500 °C before the evaporation of the Au barrier, 50-100 A° thick. A key step involved in the fabrication of the high efficiency electrodeposited CdTe/CdS solar cells was the TCJF (type conversion junction formation) process based on heating the as deposited-CdTe layers at around 400 °C in air. The junction formed after this annealing step was now close to the CdS-CdTe interface. The annealing step had in fact converted the original n-type CdTe into high resistivity p-type CdTe and formed a rectifying junction between CdS and type converted CdTe layer. By using this technique heterojunction solar cells with efficiencies > 10% were fabricated with CdTe and $Hg_{1-x}Cd_xTe$ absorber layers.

In June 1984, the technology developed by Monosolar was bought by SOHIO (Standard Oil of Ohio) which in turn was purchased by B.P. Solar International [53]. The electrolyte used for the CdTe deposition contained $CdSO_4$, TeO_2 and $CdCl_2$ and adding a mercury salt into the solution also permitted $Hg_{1-x}Cd_xTe$ film of various bandgap values to also be produced [54]. B.P solar have scaled-up this deposition process so that they can now produce modules (1ft*1ft) with efficiencies ≈ 10 % and developed the deposition process sufficiently to produce

small area cells less than 0.03 cm^2 with efficiencies ≈ 14.8% [55,56]. Key steps taken by B.P have been the replacement of the Au contacts, which were found to be unstable, by more stable contacts. Further development of the window layer - replacing the dip CdS with $Cd_{1-x}Zn_xS$ or ZnSe may improve the device efficiency further.

Alternative devices were developed by Ametek Ltd in the U.S.A [57] Ametek developed a device with an efficiency of 8% using a M.I.S. structure which consisted of stainless steel/Ni/1000 A° of Cd/2μm of CdTe/25A° of aluminium and 200A° of Ni. The device was annealed in air at 310 °C for 1 hour just after the CdTe deposition to improve the CdTe. The CdTe was found to remain n-type, highly resistive and also difficult to make low resistance contact to. The Cd layer was hence incorporated into this structure because it was thought that it would make an adequate contact to this material. However with this MIS structure it was found (i) the built-in voltage was limited to < 0.9V and (ii) the optical transmittance of the Ni was < 70%. These factors were considered to limit the device efficiency and the best cells produced where found to have n ≈ 8.6% (Vo.c.≈0.723V, Js.c≈18.7 mA/cm2 and F.F=59%). Such limitations were overcome by using a heterojunction structure [58,59]. The diffusion voltage obtained in CdTe/CdS was predicted to be 1.02 V and it could be further increased to 1.22V if CdZnS was used instead of CdS. The short circuit current was increased by using a transparent conducting oxide (TCO) and $Cd_{1-x}Zn_xS$ as a

window materials. Furthers problem associated with this structure were the high resistivity of the CdTe and the difficulty of making a low resistance contact to the CdTe.

Although Au was found to be an adequate back contact such contacts were found to unstable [54] and this led Ametek to develop a new device structure - the n-i-p solar cell [57]. This device had structure the glass/I.T.O./CdS/n-type CdTe/ZnTe/Ni. A low value of ▲Ev (valence band discontinuity) was expected at the CdTe/ZnTe interface [60] permitting easy hole transfer from the CdTe to the ZnTe and further the ZnTe (doped with Cu) was found to be a very stable contact for CdTe [61].

Further the ZnTe was transparent permitting the use of such solar cells in tandem structures [62]. Although devices with efficiencies ≈ 10.4% were produced and a production line developed to demonstrate that solar modules could be produced using such technology [57] Ametek withdrew from solar cell development in 1990.

3.4 Close Spaced Sublimation (C.S.S):

The close spaced sublimation (CSS) technique is similar to the closed spaced chemical vapour transport technique developed during the (1960,s), except that no transport agent is used [63]. Previously this technique was used for the epitaxial growth of CdTe [58,64] but now is applied to the deposition of polycrystalline CdTe thin films [65,66]. A diagram of the growth system used is given in fig.3.1. The critical parameters involved for

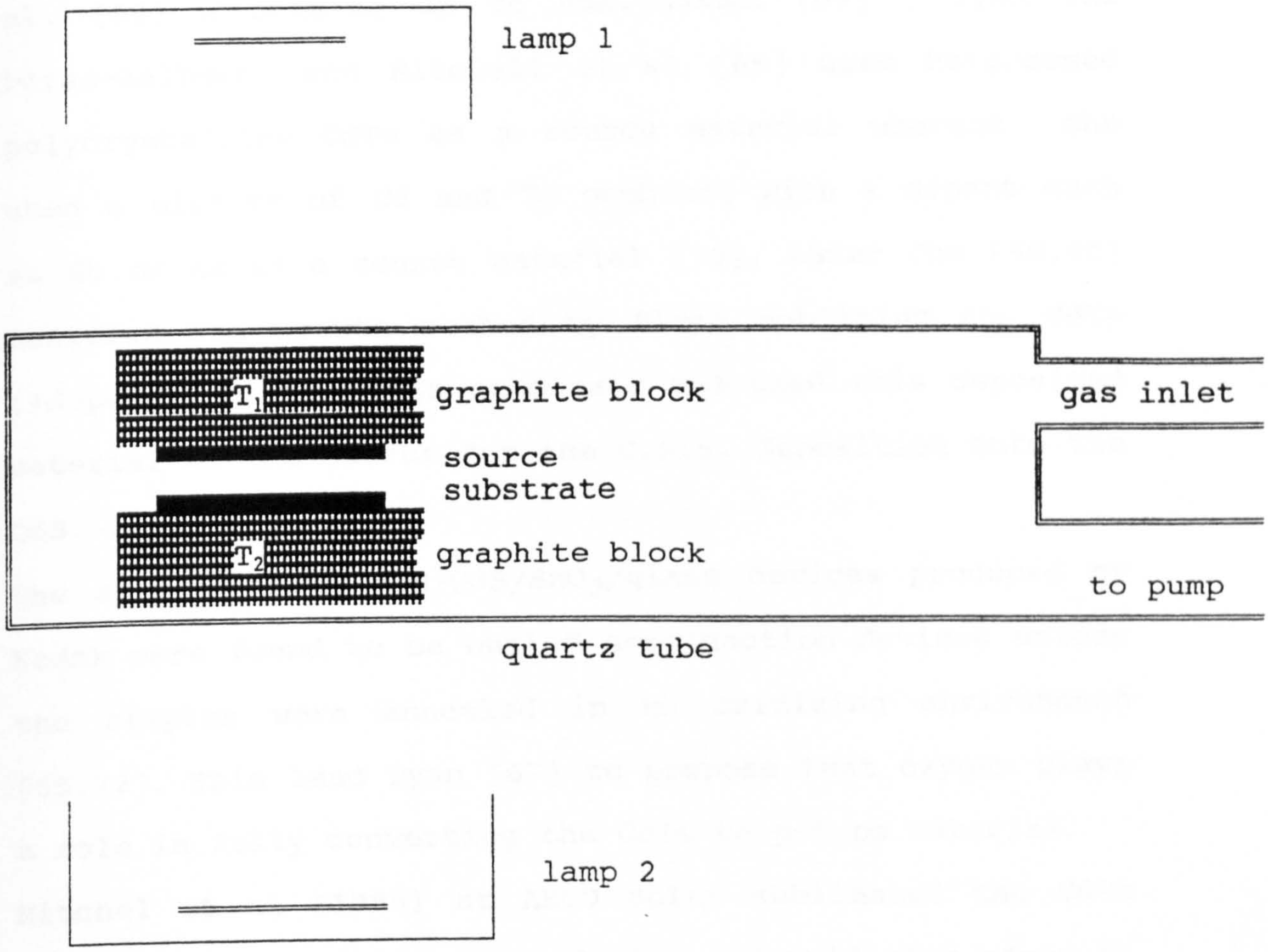

Fig.3.1 Diagram of the C.S.S. Apparatus for the Deposition of Cadmium Telluride Thin Films

the deposition of CdTe are the spacing between the source and the substrate, their temperatures and the temperature difference between them. Kodak [67] use a spacing, 1-2 mm, Chu [68] a spacing of 1mm and Mitchel et al. [66] a spacing up to 5mm. Kodak [69] (Tyan and Perez-Aalburn) and Mitchell et al [66] used hotpressed polycrystalline CdTe as a source material whereas Chu used a mixture of Cd and Te combined with a dopant such as Sb or As as a source material [70]. Later Chu [60,65] modified the growth method by first subliming the CdTe (+dopant) onto a glass substrate and used this deposited material as the source for the C.S.S. deposition onto the CdS.

The as-deposited CdTe/CdS/SnO_2/glass devices produced by Kodak were found to be buried homojunction devices unless the samples were annealed in an oxidizing environment [65,72]. This lead Tyan [67] to propose that oxygen plays a role in fully converting the CdTe to p-type material.

Mitchel et al (1985) at ARCO solar sublimated the CdTe onto the CdS using inert, reducing and oxidizing gases in the deposition chamber and found higher efficiency devices to be produced when oxygen was present in the growth chamber.

It was reported by Bonnet et al [72] that a $CdCl_2$ treatment was important for improving the film quality; when such heat treated films were used the solar cells produced had efficiencies > 11 %. Such cells however had a low value of F.F. (0.65) which was attributed to either a poor back contact to the p-type CdTe or a low doping

level in the CdTe ($\approx 10^{15}$ cm^{-3}).

It was reported by Chu et al [73] that the devices fabricated by incorporating Sb as a dopant into CdTe achieved an efficiency 10.5 %. Increasing the concentration of Sb in the CdTe decreased the resistivity to 200 Ωcm but beyond this limit no uniform or adherent films were obtained. The Kodak group reported that their doped CdTe films did not yield efficient solar cells [65].

One of the major problems with closed spaced sublimation is to produce pin-hole free, uniform films of proper composition. The thickness of the CdTe obtained by Tyan, Chu and Michell in their high efficiency CdTe solar cells were 4 μm, 10-15 μm and 10 μm respectively.

A major advantage of this process is a material utilization rate which is close to unity. Further this process permits a very high deposition rate ≈ 1-5 μm/min and the short deposition time used by Tyan and Perez-Albuerne [65] allowed the predeposited films to withstand high temperature processing. The equipment used for CSS is also simple and a low cost method of production (≈ \$ $3.5/m^{-2}$ for CdTe 10μm thick [49]). Chu determined that the grain size of the CdTe thin film was increased from 1μm to 3-5μm with well shaped faces when the substrate temperature was increased from 500°C to 600°C.

Mitchell et al. deposited CdTe using the CSS method using a substrate temperature of 600 °C. The CdTe produced had the sphalerite crystal structure rather than the wurtzite structure produced using lower temperatures and had

increased optical transmittance for photons with energies less than the energy bandgap.

It was also observed that a change in the substrate temperature strongly influenced the spectral response. As shown in fig.3.2 interface recombination equally effected the carriers generated at different depths in the CdTe by photons of different wavelengths. When the substrate temperature was increased the cell behaved less bias dependent but more wavelength dependent which meant that bulk recombination now dominated. The spectral response of the cells produced using higher substrate temperatures have much greater carrier generation at longer wavelengths under reverse bias conditions implying that there is an improvement of the interface which was probably due to an improvement in the CdTe itself [67].

Chu [74] recently reported the highest (world record) CdTe solar cell conversion efficiency, 15.8% under AM 1.5 illumination, with $V_{o.c} \approx 0.843V$, $J_{s.c} \approx 25.1$ mA/cm^2 and F.F = 0.75%. The front contact used for this cell structure was fluorine doped SnO_2 with a resistivity of 7-10 Ω/· and a transmittance greater than 90% over the visible spectrum. On the top of this a very thin film of CdS was deposited using the chemical bath deposition method [74]. The CdS/SnO_2:F/glass structure was then annealed at 350-425 °C in hydrogen for several minutes. It was observed using A.E.S.(Auger Electron Spectroscopy) that the ratio of Cd/S at the surface of the film increased when the film was annealed in this reducing

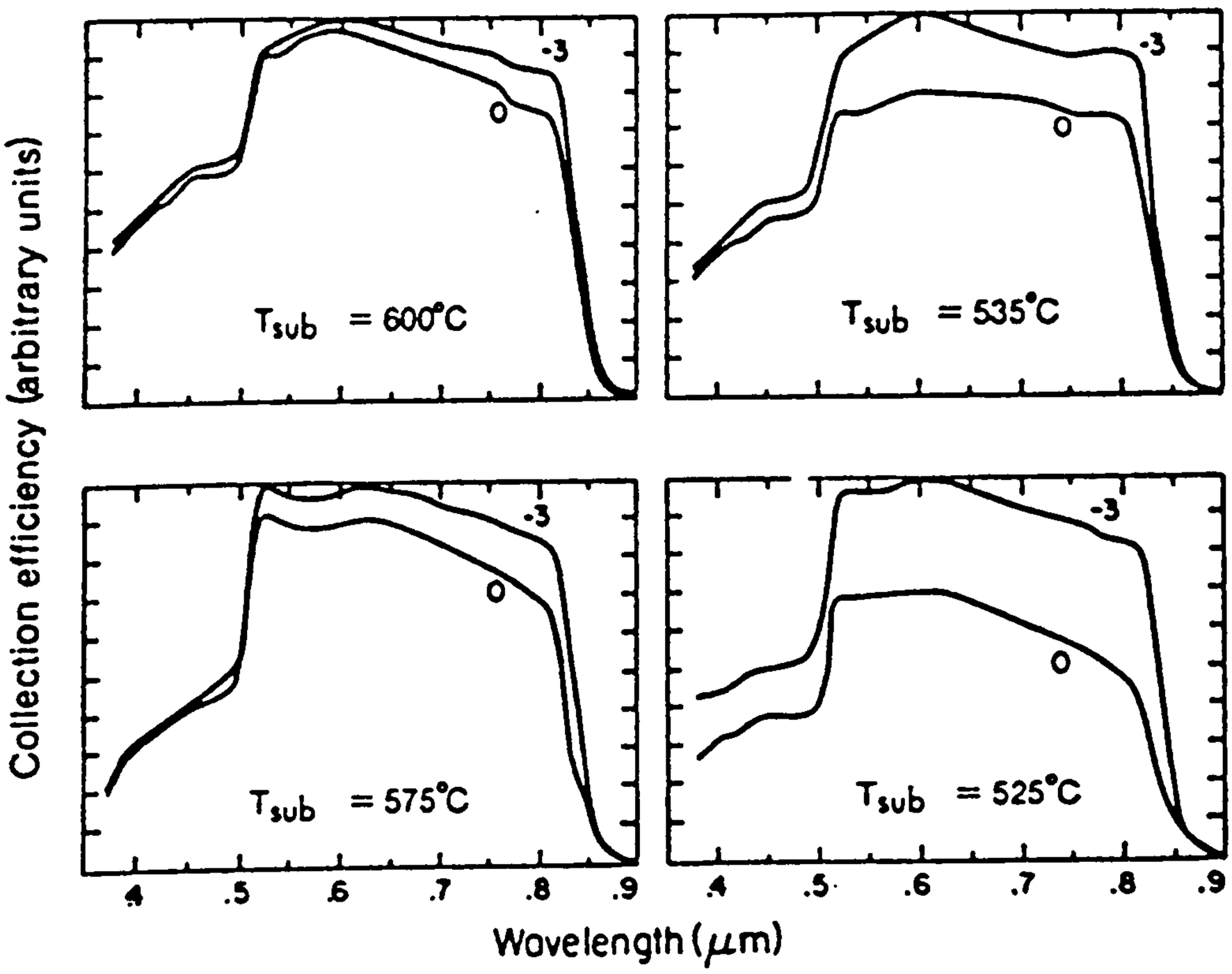

Figure 3.2(a) Spectral Response of the Cells Deposited at Different Substrate Temperatures

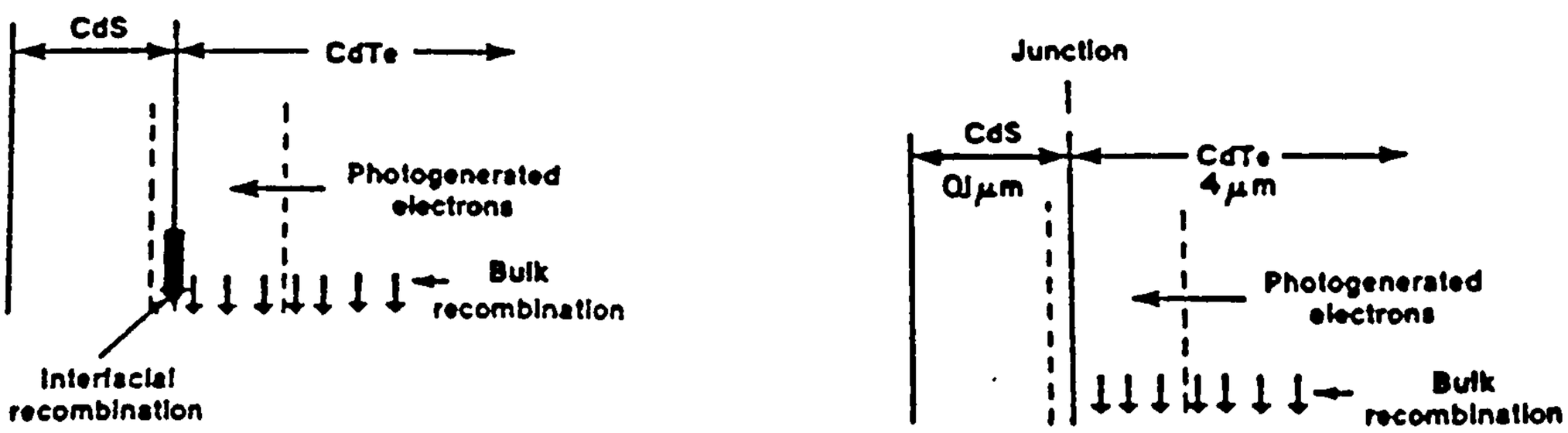

Figure 3.2(b) Proposed Model Basedon the Effect Different Substrate Temperature Upon the Deposition of CdTe

atmosphere [74]. It was thought when the CdTe film was deposited onto unannealed CdS the diffusion of sulphur from the CdS into the CdTe surface created defect states at the interface which acted as recombination centres. By producing a cadmium rich surface on the CdS the open circuit voltage and the short circuit current were both improved. Chu reported that a longer annealing time for the CdS is required when the thickness of CdS is reduced suggesting some dependence of this effect on the grain size of the CdS. If the thickness of the CdS was greater than 1000A° the short circuit current was substantially reduced. It should be noted that for the high efficiency cells the CdTe was 5μm thick and it had been given a post deposition heat treatment [74]. The cell was completed by forming a back contact of doped graphite paste. The I-V characteristic under illumination is shown in fig.3.3 [74].

Recently Solar Cell Incorporated have scaled-up a modified version of C.S.S. process to produce modules, 6844cm^2, with efficiencies of 7.7% [75].

3.5 Spray Pyrolysis:

Spray pyrolysis was initially developed by Chamberlin [76,77]. The process consists of spraying solutions containing the elements needed to form the compound onto a heated substrate where they react to form the compound; a post synthesis anneal is then used to drive off any excess materials. This process has been developed to

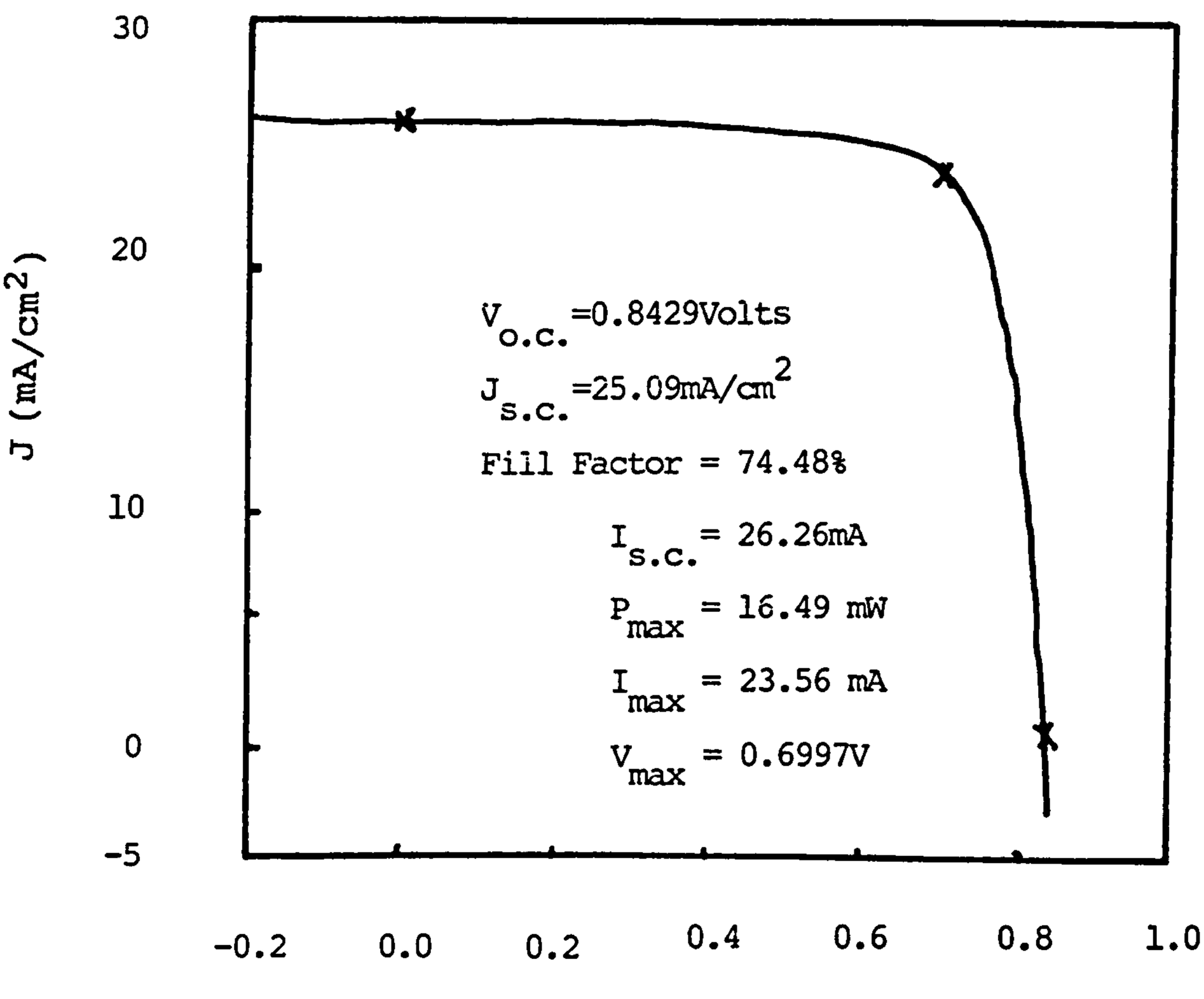

Figure 3.3 I-V Characteristic Under Illumination

produce layers of metallic oxides, sulphides, selenides and tellurides [25].

Photon Energy [78,79,44] have made the most progress in producing CdS/CdTe solar cells using this method. The first step in their process involves producing a layer of indium tin oxide (I.T.O.) on a glass substrate. This layer is formed by spraying a solution consisting of $SnCl_2$:H_2O and ammonium bifluoride onto a glass substrate , heated to 500°C. Photon energy reports that it is possible to produced I.T.O. layers with thicknesses up to 3900 A° and with resistivities ≈ 7Ω/· using this process [44].

The next step involves the deposition of a layer of CdS. This layer is formed by spraying a solution consisting of 0.1M $CdCl_2$, 0.11M thiorea and 20-200 p.p.m. of copper (in the form of cupric acetate) onto the I.T.O./glass substrate which heated in the range 375-400 °C.

The CdS layers produced typically have thicknesses ≈ 1.5 μm with carrier concentrations ≈ $10^{17}cm^{-3}$. Although there is an improvement in grain size for the thicker layers produced [80] the transmittance of CdS reduces with increasing thickness and 1.5μm is considered to be the optimum thickness for producing a good interface with the CdTe (subsequently deposited) while maintaining good transmissive properties.

Photon Energy do not give details of the solutions used to produce CdTe. They do however report that the grain size of the CdTe is typically 3μm near to the interface and that the grain size is smaller further from the

interface (1-4μm). The layers used are typically 6μm thick with carrier concentrations $\approx 5*10^{14}cm^{-3}$.

Prior to forming a back contact to the CdTe the CdTe is etched using a bromine/methanol solution to form a tellurium rich surface [81]. The back contact is then made using copper doped graphite paste [82] which is found to be more stable than Au or Te back contacts [44].

The highest efficiency solar cells produced have efficiencies of 12.3% ($V_{o.c.}$=783mV, $J_{s.c.}$=25mAcm^{-2} and F.F.=0.63) for a device area = 0.31cm^{-2}. They have also produced modules, 838 cm^2 in area with efficiencies $\approx$ 7.3%.

The advantages of this method are the high rate of production of these cells, (the deposition rates of the layers are typically $\approx$ 3μm/minute), the low capital cost of the equipment used and the absence of a need for highly skilled manpower in the production process. However the CdTe layer used needs to be quite thick ($\approx$3-6μm) to avoid the formation of pinholes in the layers which lead to shorting paths and hence lower device efficiencies. The cost of production of a 6μm thick layer of CdTe with an area of 1m^2 is about \$2/m^2 [50].

It should be noted the spectral response at longer wavelengths was found to be extended in these devices indicating that there was interdiffusion of CdS and CdTe at the interface to form a layer of $CdS_{1-x}Te_x$ [39]. Such interdiffusion was confirmed using S.I.M.S. (secondary ion mass spectroscopy) studies which measured the distribution of S and Te at the interface [44].

3.6 R.F. Sputtering:

Sputtering is a technique that can be scaled-up for large scale production and hence its use for producing CdS/CdTe solar cells has been investigated by many research groups [83,84]. The most substantial progress have been made by F. Abou. et al [84] and hence their work is discussed here.

The CdTe films are sputter deposited from a CdTe target using a 2 inch rf planar magnetron S-gun system that minimizes electron bombardment of the film surface. A typical deposition rate of 1-20 μm/h is obtained with an rf power of 50-500W. The sputtering parameters monitored during evaporation are the pressure (2mT), the Ar gas flow (3Sc cm) and the substrate temperature in the range (150°C-400°C). Doping of the film can be achieved by adding O_2 to the Ar gas or by adding Cu to the CdTe target and the CdTe thickness is simply controlled by altering the time of sputtering.

The O_2 doped films were found to have grain sizes ≈ 0.25-2 μm whereas the grain size of the Cu doped films are larger ≈ 0.3-4 μm in diameter.

In both cases the layers have the sphalerite crystal structure with most of the grains oriented with their [100], [110] or [111] axes aligned perpendicular to the substrate surface.

The doped layers had the carrier concentrations in the range 10^{16}-10^{18}cm^{-3} and the minority carrier life time determined to be 10^{-10}s for N_A.= 10^{16}-10^{17}cm^{-3}.

Photoluminscence was observed (at 4°K) for the as-deposited samples and for samples annealed at temperatures in the range 370-480 °C.

For the unannealed samples two peaks were observed, one at 1.63 eV was attributed to band to band transitions and the other at 1.58eV was attributed to bound exciton emission associated with cadmium vacancies.

For the annealed samples the 1.58 eV peak was found to be enhanced and it showed two different regions of emission, one region of emission was attributed to an exciton transition where as the lower energy emission was attributed to donor-acceptor recombination associated with copper or oxygen or their complexes with cadmium vacancies.

The photoluminscence from Cd rich films doped with Cu resulted in peaks which were associated with Cu, Cd and Te. The copper atoms substituting onto cadmium lattice sites were considered to act as acceptor impurities whereas the interaction of copper atoms with native defects could result in defect complexes that could act as donors.

The devices produced using the sputtered CdTe layers (within a CdS/CdTe/ back contact structure) were found to have an efficiency of 6.7 % ($V_{o.c}$ = 682 mV, $J_{s.c}$ = 19.3 mA/cm^2 . F.F. = 0.51) for a device area ≈0.08 cm^2) [84].

Capacitance voltage measurements on these devices were interpreted as indicating the production of a p-i-n device rather than a simple heterojunction device and

they also indicated the presence of an iterfacial layer with a high density of interface states.

Devices have also been produced by sputtering I.T.O. directly onto single crystal p-type CdTe without the use of a CdS layer [85]. An efficiency of 8% was achieved [$V_{o.c.}$ = 820mV, $J_{s.c}$ =14.5 mA/cm^2 and F.F = 0.55]

It was found that such devices were actually buried homojunction devices rather than heterojunction devices; the surface of the p-type CdTe had infact been converted to a layer of n-type CdTe about 1μm thick. The efficiency of these devices degraded with time. It was found that the reason to this degradation was that the n-type surface layer created by surface damage gradually became p-type resulting in the devices now becoming the less efficient I.T.O./CdTe hetrojunction.

3.7 CVD and MOCVD:

The apparatus used for the deposition of CdTe thin films using CVD (chemical vapour deposition) is shown in fig.3.4 [68]. A cadmium source , a tellurium source and a substrate are placed in a fused-silica reaction tube in a multizone furnace with each zone separately heated and controlled. A carrier gas such as hydrogen or helium is used to carry the cadmium and tellurium vapours to the surface of the heated substrate (≈550 °C) where they combine to form CdTe.

M.O.C.V.D. (metal organic chemical vapour deposition) is similar to C.V.D except for the choice of the starting chemicals and temperature regimes used. In both cases, a

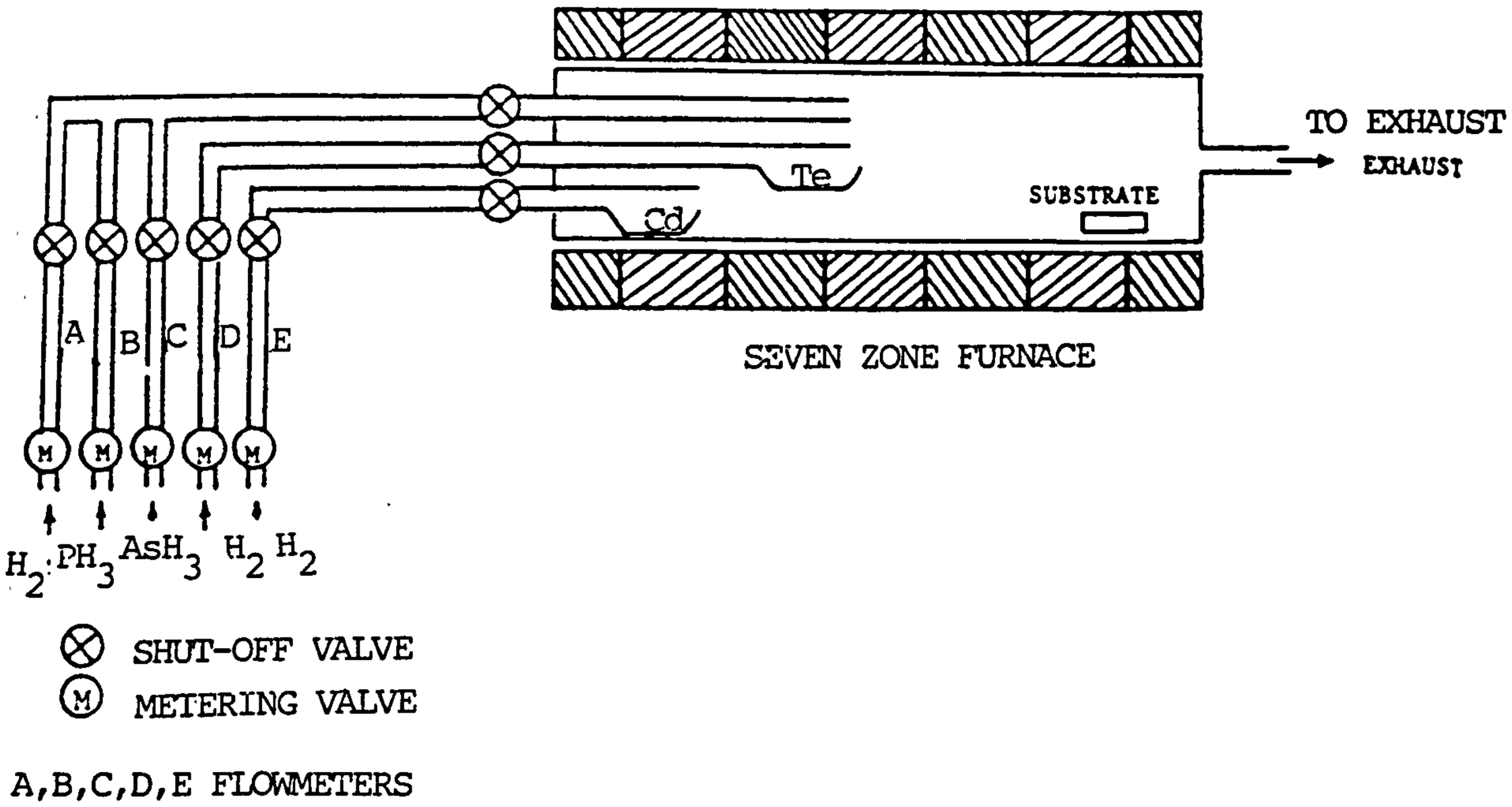

Figure 3.4 Diagram of the M.O.C.V.D./C.V.D. Apparatus Used for the Deposition of CdTe Thin Films.

suitable set of feedstock gases are chosen so that when they are passed over the substrate at some elevated temperature, they react and CdTe is formed on the substrate.

The starting materials for MOCVD are however organic compounds such as dimethylcadmium (DMCd), a source of cadmium, and dimethyletelluride (DETe) or di-isopropyltelluride (DIPTe) which are sources of tellurium. This technique can be used with relatively low substrate temperatures and is flexible for controlling the incorporation of dopants into the CdTe films. The films produced by this technique have high resistivities , 10^6-10^4 Ωcm , and carrier concentrations ≈ 10^{14} cm^{-3}. There is flexibility in controlling the conductivity of the films produced by intrinsic and as well as extrinsic doping. When the tellurium to cadmium molar ratio in the reaction mixture is increased slightly (less than 1%) the deposit is p-type, and when the tellurium to cadmium molar ratio is reduced the deposit is n-type. The p-type doping is attributed to Cd vacancies and n-type doping to tellurium vacancies [86]. A minimum resistivity ≈ 200 Ωcm is obtained by controlling the Cd/Te ratio to about 1.02 in the mixture but above or below this ratio the resistivity is found to increase. This increase is attributed to the formation of defect complexes associated with Cd vacancies or Te interstials.

It is found that the electrical resistivity can also be controlled by extrinsically doping the material by adding AsH_3 or PH_3 to the reaction mixture during the deposition

process [68]. It is found that there is an optimum value of AsH_3 - to - cadmium molar ratio of about $2*10^{-3}$ at which the resistivity is minimum but above that it increases due to interaction of the dopants with native defects.

The energy band gap of the films is found to be 1.5eV which is equal to that determined for single crystal CdTe.

The minority carrier diffusion length in p-type CdTe (cadmium deficient and arsenic doped) thin films grown on W/graphite substrates is found to be about 2μm which is considerably higher than that measured in n-CdTe thin films (L $\approx$ 0.8μm) [87].

Chu [88] has used CVD since 1981 to make CdTe solar cells. He reported an efficiency of 8.2% for small area ($\approx$1cm^2) solar cells in 1985. Instead of using the superstrate configuration, Chu made devices by depositing the CdTe onto tungsten coated graphite substrates; he actually found that the carbon doped the CdTe film p-type. When Chu switched to making superstrate devices he found the devices produced had higher efficiencies $\approx$ 9.85%. Honey well (Schafer 1988 [89]) also investigated the use of MOCVD to produce CdTe cells and were able to develop a low temperature (under 300 $^{\circ}$C) MOCVD process for producing CdTe.

Stirn at the Jet Propulsion laboratory has also used MOCVD to produce thin films of CdTe and higher gap CdTe alloys. Stirn fabricated solar cells with the callaboration of Ametek who supplied him with

glass/SnO_2/CdS substrates. The CdTe films were then deposited at JPL and the devices were completed by depositing ZnTe and nickel at Ametek. This combined effort resulted in a solar cell efficiency of 9.4%.

Rohatgi [90] at Georgia Tech also investigated the potential of using MOCVD technique for making CdTe. He managed to produce solar cells with η = 9.7%. For these cells $V_{O.C} \approx 0.73V$, $J_{S.C} \approx 22.16$ mA/cm^2 and F.F. ≈ 0.6.

A major problem associated with CVD and MOCVD growth is the formation of pin holes at temperature > 550 °C. The temperature used in the CSS process is higher than this but the exposure time is smaller, and it is found that thinner layers free from pinholes can be produced.

Material utilization in CVD is expected to be 75% in a commercial process, and the cost involved in producing the CdTe material would be about \$ 6.40/m^2 for layers 15 μm thick, which is high compared to the alternate methods of deposition.

M.O.C.V.D is even more expensive than C.V.D.; > 30 \$/m^2 to produce CdTe layers, 1μm thick, mainly because of the very high cost of the organometallics compounds used [49]

3.8 Atomic Layer Epitaxy (A.L.E):

Atomic layer epitaxy is a novel technique developed by Michrochemistry Ltd., Finland for depositing semiconductors. The details of the method are discussed by J. Skarp et al [91]. Essentially the deposition is controlled by the adhesion of the evaporant to the substrate being much greater than the cohesion of the

evaporant atoms at the substrate temperature used such that a layer of evaporant one atomic thick adheres to the substrate but subsequent atoms evaporated do not adhere to this layer. Other elements may however deposit on this layer at this temperature and in turn the former material may deposit on them. It is therefore possible to form the material atomic layer by atomic layer.

The solar cell structure developed by Microchemistry has the structure glass/I.T.O./CdS/$CdS_{1-x}Te_x$/CdTe/back contact. The novelty of this structure is the inclusion of a graded layer of $CdS_{1-x}Te_x$ at the interface in attempt to reduce the strain resulting from the mismatch in lattice parameters of CdS and CdTe (9.7%) which could result in interface states.

The results obtained are impressive; for a device with an active area of 12 mm^2 an efficiency of 14 % was achieved (with $V_{o.c.} \approx 804mV$, $J_{s.c.} \approx 23.8mA/cm^2$ and F.F ≈ 0.73). The reverse saturation current density, J_o was $\approx 10^{-11}{}_{A/cm^2}$ and the ideality factor, $\eta \approx 1.7$.

The result indicate that the density of interface states at the junction or within the CdTe depletion region was reduced by the inclusion of the $CdS_{1-x}Te_x$ buffer layer. This information is useful because it supports the evidence from other studies [47] that the interdiffusion of CdS and CdTe to form a $CdS_{1-x}Te_x$ layer during a post-sythesis heat treatment is beneficial to device performance. For different samples the highest $V_{o.c}$ achieved was 0.84 Volts, the highest $J_{s.c}$, $26mA/cm^2$ and the highest F.F., 0.73. The highest $J_{s.c.}$ value was

obtained using either very thin CdS layer (20 nm) or using Cd_{1-x} Zn_xS instead of CdS. Michrochemistry believe that the F.F. can also be improved by reducing the series resistance further by improving the doping of the CdTe and by using an improved back contact.

It should be noted that after the CdTe deposition Microchemistry used a $CdCl_2$/methanol heat treatment, followed by bromine/methanol etch prior to depositing a Cu/Au back contact. The $CdCl_2$/methanol annealing step in particular was found to be essential for producing high efficiency devices.

The problems associated with this method are the slow deposition rates involved [91] and problems of the scale-up of the technology to produce large area modules. The major advantage is the excellent control of the materials deposited; this permits detailed investigations of what efficiencies can be achieved with CdTe technology.

3.9 Molecular Beam Epitaxy (M.B.E.):

M.B.E. is the most advanced technique for growing semiconductor layers. It is essentially a thermal evaporation technique which uses the best equipment available; the elements are evaporated using Kundsen cell sources in an ultra-high vacuum system and under such vacuum conditions the rate of evaporation of each element is accurately controlled by the temperature of the source material.

This technique has been used to produce CdTe by Rohatgi et al [92] by coevaporating Cd with Te onto the

heated substrates, and to produce $Cd_{1-x}Zn_xTe$ by coevaporating Cd, Zn and Te. It is also possible to extrinsically dope these layers by co-evaporating a dopant with the elements e.g [93] have used arsenic and antimony as p-type dopants and indium, as n-type dopants. For solar cell applications the CdTe and $Cd_{1-x}Zn_xTe$ have been deposited onto glass/I.T.O./CdS substrates [92]. The substrates were baked for 3-4 hours at 250 °C before film growth, the substrate temperature raised to 275 °C for film growth to commence and the substrate temperature raised raised to 300°C for the remainder of the deposition. The growth rate was kept constant during the deposition to 1μm/hour.

Both the CdTe and $Cd_{1-x}Zn_xTe$ layers deposited were found to have the sphalerite crystal structure and were free from second phase material as determined using X-ray diffraction. Electrochemical stripping of the layers in conjunction with the surface photovoltage measurements were used to demonstrate the uniformity of the material and the sharp interface formed with the CdS.

The CdTe solar cells produced were found to have an efficiency, $\eta \approx 7.6\%$ ($V_{o.c.}$= 666mV, $J_{s.c}$=17.5 mA/cm^2 and F.F. = 0.63) whereas the $Cd_{1-x}Zn_xTe$ devices had an efficiency, η=3.6% ($V_{o.c.}$ = 511 mV, $J_{s.c.}$ = 11.4 mA/cm^2 and F.F = 0.48). M.B.E. would be for too expensive a technique to produce commercial solar cell devices but it will remain a tool to investigate in detail the properties of the CdS/CdTe solar cell. The relatively low efficiencies achieved to date using this method perhaps

confirm the importance of the $CdCl_2$ heat treatment (which was not used in this work) and the need for some interdiffusion of the CdS and CdTe at the interface to reduce the density of interface states present.

3.10 Pulse Laser Deposition :

"Laser driven physical vapour deposition" (L.D.P.V.D.) is a novel technique developed at the University of Torledo, U.S.A, to evaporate layers of CdS, CdTe and alloys such as $Cd_{1-x}Zn_xTe$ [94,95]. A diagram of the deposition system used is given in fig.3.5 In this process the source material is heated using a XeCl eximer laser operating at a wavelength of 308 nm. The laser pulse duration is typically < 30 n-Sec and is considered to increase the temperature of the evaporant material to well above it melting point during this time. The technique is therefore considered to congruently evaporate the elements constituting the source material and to produce highly stoichiometric layers.

The layers of the CdS and CdTe produced using this technique are however found to consist of small, randomly orientated grains ≈ 0.11μm in diameter. The grain size was improved by depositing a layer of $CdCl_2$ onto the glass/I.T.O./CdS/CdTe structure using L.C.V.D. and annealing the device in a 15% O_2/N_2 mixture at 400 $^{\circ}$C for 30 minutes. Such an anneal was found to have recrystallised the CdTe and CIS with columnar grains, ≈ 1μm in diameter extending through the device. The back contact was formed by evaporating 50 A$^{\circ}$ of Cu followed by

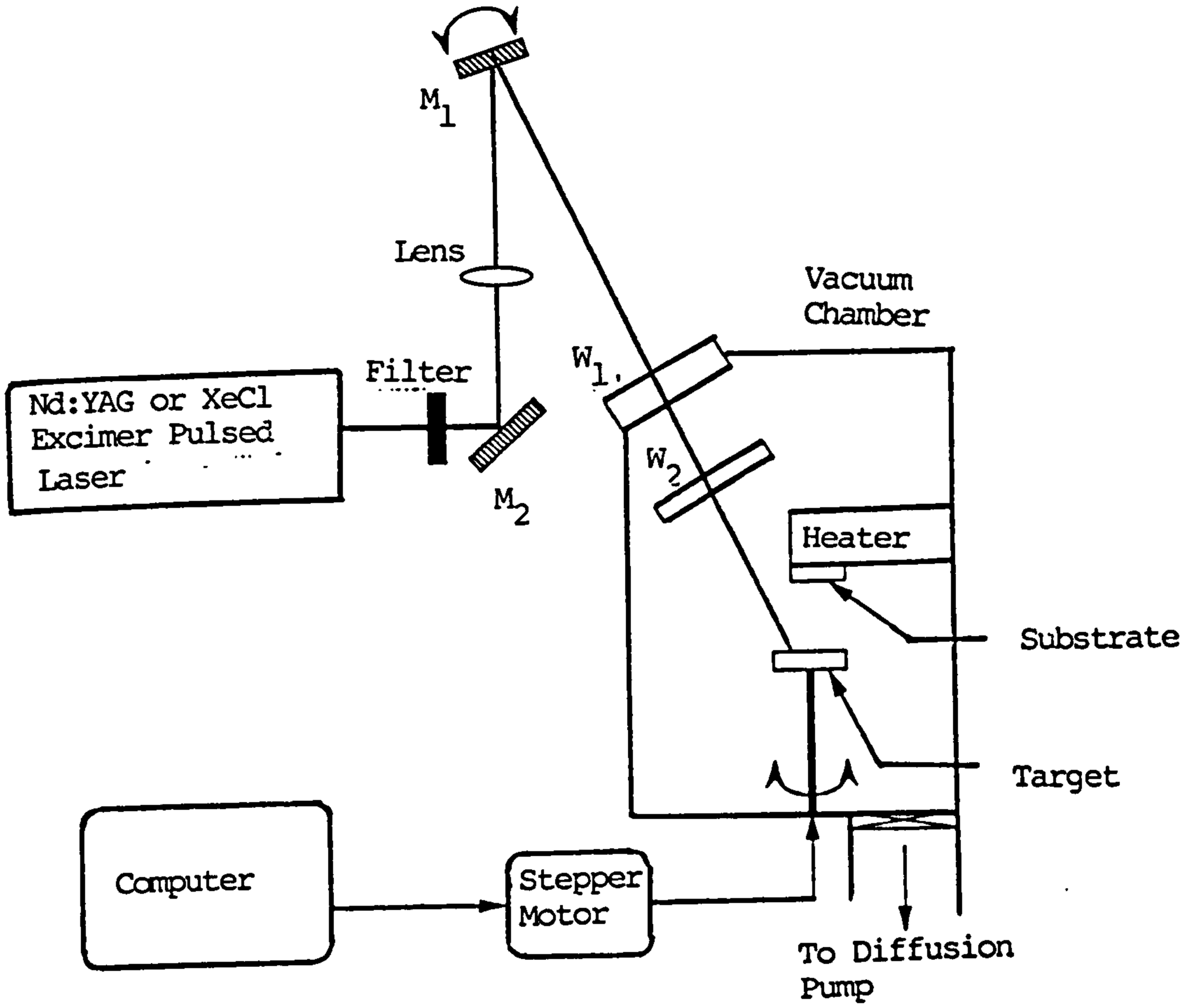

Figure 3.5 Diagram of the System Used for Laser-Driven Physical Vapor Deposition of CdTe Thin Films

100-200 A° of Au or Ni. The devices were then heat treated in air at 150 °C for 30 minutes to improve the contact.

The small area cells (≈0.08cm^2) produced using this technique had efficiencies > 8% ($V_{o.c.}$ = 750mV. $J_{s.c.}$ = 19 mA/cm^2 and F.F=0.6).

It should be noted that the recrystallised CdTe had the sphalerite crystal structure and were well orientated with the <111> direction perpendicular to the plane of the layer.

3.11 P-type Doping of CdTe and Ohmic Contact Formation

The major problems associated with producing high efficiency solar cells using polycrystalline CdTe are :-

(i) adequate and controlled doping of CdTe and

(ii) the formation of stable ohmic contacts to p-type CdTe.

The two problems are interrelated. With polycrystalline CdTe many extrinsic dopants have the tendency to segregate at the grain boundaries and to more easily diffuse down the grain boundaries particularly when the samples are heated . Shunting paths through the layers and enhanced recombination centres at the grain boundaries thus result which can severely reduce the performance of the devices made using such layers. Annealing the CdTe samples after growth is important to not only enhance the grain growth within the samples but to also move the impurity atoms onto substituitional sites to act as effective dopants. Thus it is often

observed that solar cells produced using extrinsically doped CdTe have low efficiencies. The diffusion of atoms from the contact material through the grain boundaries at room temperature is also a mechanism which can reduce the solar cell efficiency with time i.e. produce unstable solar cells.

The grain boundaries in CdTe can also be highly resistive. The series resistance, R_s, can be dominated by the potential barriers at the grain boundaries (φ_{gb}) and at the contacts (φ_b). The magnitude of φ_{gb} and φ_b are in fact strongly influenced by the carrier density with the grain adjacent to these barriers. Thus "doping" the CdTe and forming an "ohmic contact" in practice is usually a complex combination of reducing φ_{gb}, φ_b and increasing the doping concentration with the grains.

As reported by Bube [96] it is very difficult to form a true ohmic contact to p-type CdTe because no metal has a higher work function than that of p-type CdTe. ($\varphi_{CdTe} \approx$ 5.7eV).

Further the method normally used for forming ohmic contacts to single crystal p-type samples, of forming a p^+ layer at the sample surface by indiffusing a dopant material is not easily applicable because of in diffusion of the impurities at the grain boundaries leading to unstable devices.

Although metals such as gold and copper have been used as contact materials the contact resistance is not as low as desirable and further such contacts are unstable [97,98].

The most successful approach to p-type "doping" the CdTe

has involved annealing the as-grown CdTe in the presence of $CdCl_2$ and oxygen. Copper is also very often present in the system and it is not yet conclusively established whether its presence is essential or not. Certainly the highest efficiency devices produced from the CdTe layers deposited using the C.S.S. method [74], electrodeposition [55], screen printing [36], spray pyrolysis [78] etc have used this heat treatment. The mechanism of CdTe doping is not fully understood but it probably reduces φ_{gb}, φ_b and increases the doping within the grains. The $CdCl_2$ anneal in recrystallising the CdTe to produce columnar grains must certainly influence, φ_{gb} [99]. The $CdCl_2$ anneal is also thought to reduce the density of recombination centres at the interface or in the CdTe depletion region perhaps by promoting the interdiffusion of CdTe and CdS at the interface to form $CdS_{1-x}Te_x$ [82]. Oxygen and copper are thought to be p-type dopents [70,100] although their interaction with native defects may be more complex [101].

To form a low resistance contact to such p-type CdTe the approach used by most workers involves etching the CdTe surface to produce a tellurium rich surface on the CdTe which is found to be strongly p-type and highly conductive. Such a surface is produced by etching in a bromine/methanol solution (≈0.1%) [55].

The contact material is then deposited onto the thin "p^+" surface. For research purposes gold and copper doped graphite paste are the two most common contact materials used [55,68]. Michrochemistry Ltd [102] and Solar Cells

Incorporated [103] have recently reported that they use Ni-Al contacts in their modules.

The solar cell with highest efficiency produced to date was produced using a back contact formed using a mixture of HgTe and carbon paste [104]. HgTe is in fact one of the few materials with a work function greater than that of CdTe and its diffusion into CdTe is expected to produce narrow energy bandgap, p^+ $Hg_{1-x}Cd_xTe$. The contact resistance of HgTe to p-type CdTe was determined to be as low as 0.1 Ωcm^2 when it was deposited onto p-type CdTe using C.S.V.T growth at 550 $^{\bullet}C$ [98]. The long term stability of such contacts is however not yet proven and they may be unstable.

Some workers report that prior to producing the tellurium rich surface they etch their samples using potassium hydroxide or hydrazine [105,106]. This etching step is considered to be to be important to remove $CdTeO_3$ or other oxides that may have formal on the CdTe surface when the samples were annealed in air [107].

Ametek [57] have elegantly avoided both the problems of doping the CdTe and forming an ohmic contact to p-type CdTe by developing an alternative device structure - the n-i-p solar cell. This device has the structure glass/I.T.O./CdS/n-type CdTe/ p^+-ZnTe/Ni contact. The CdTe used was as-grown i.e. n-type with a very high resistivity where as ZnTe was heavily doped p-type by co-evaporating ZnTe with Cu. The devices were found to be very stable with efficiencies ≈ 10%.

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CHAPTER IV

EXPERIMENTAL PROCEDURE

4.1 The System Used for the Deposition of Cadmium and Tellurium Thin Films:

The deposition system fig.4.1 consisted of a glass bell jar mounted on a stainless steel baseplate which was evacuated using an oil diffusion pump (backed with a rotary pump) to achieve a vacuum pressure in a range 10^{-6}-10^{-7} Torr. The materials to be sublimated were contained in quartz crucibles (made at University of Newcastle) and the crucible heated using cylindrical tantalum heaters fig.4.2 and fig.4.3 purchased from the R.D. Mathis Company (U.K). The crucibles were "detachable" to permit easy cleaning of the crucibles and loading of the source materials.

The current passed through the source heaters was controlled using a thyrister switch which was connected to a programmable temperature controller (type 455) which were supplied by C.R.L limited.

The temperatures of the evaporation sources and substrate were monitored using K-type thermocouples supplied by T.C.Ltd and these provided feedback to the controllers.

Two shutters were used, one close to the substrate to prevent deposition onto the substrate and another shutter just above the quartz bottles containing the cadmium and tellurium could be adjusted to cover both sources or just one source to prevent either cadmium or tellurium vapour or both reaching the substrate. The substrate plays an

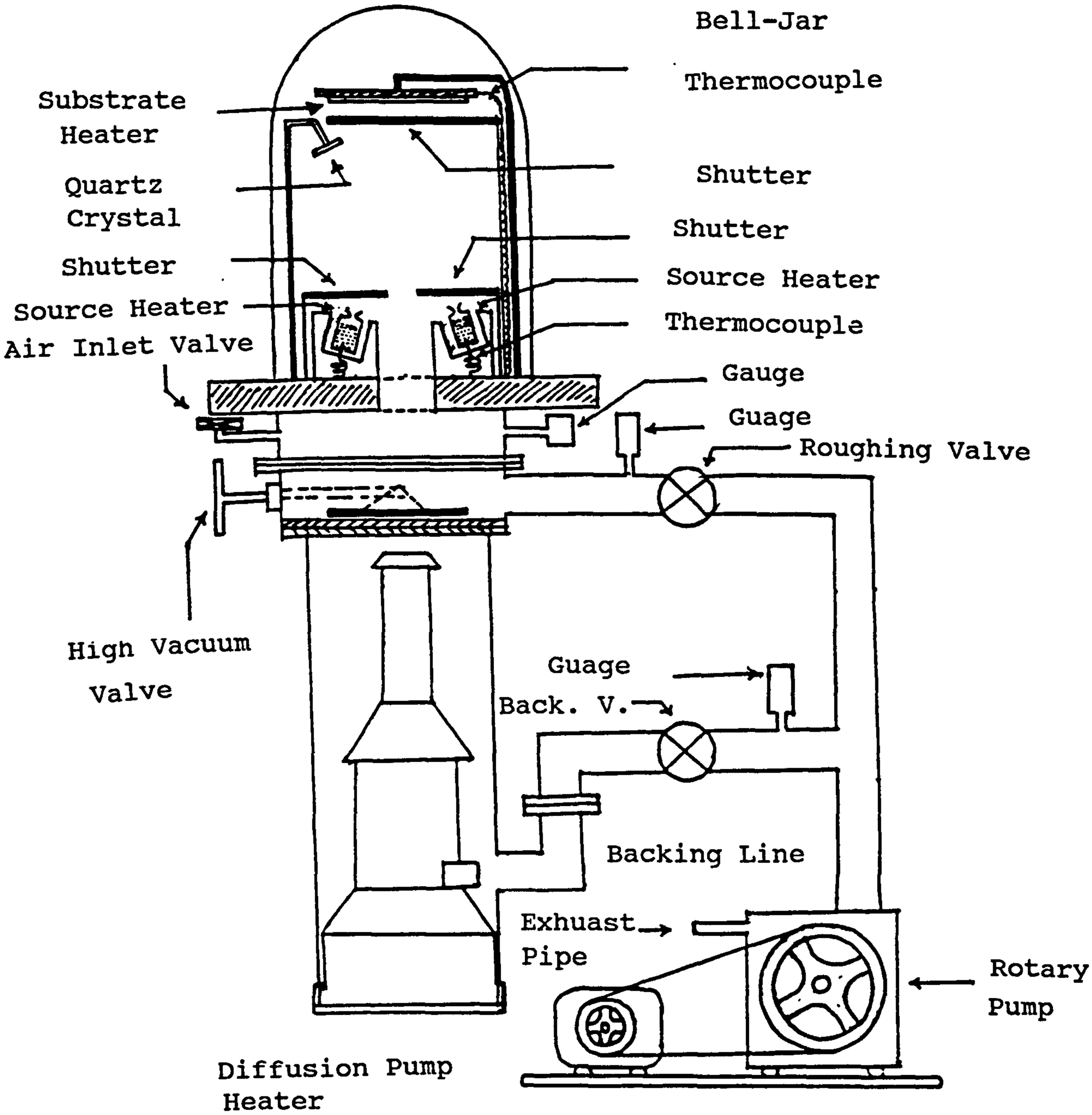


Figure 4.1 Deposition System Used to Deposit Alternate Layers of Cadmium and Tellurium Thin Films

(a) (b)

Figure 4.2 (a) Quartz Ampoule for the CdS Evaporation
(b) The Detachable Quartz Ampoule Used for the CdTe Evaporation

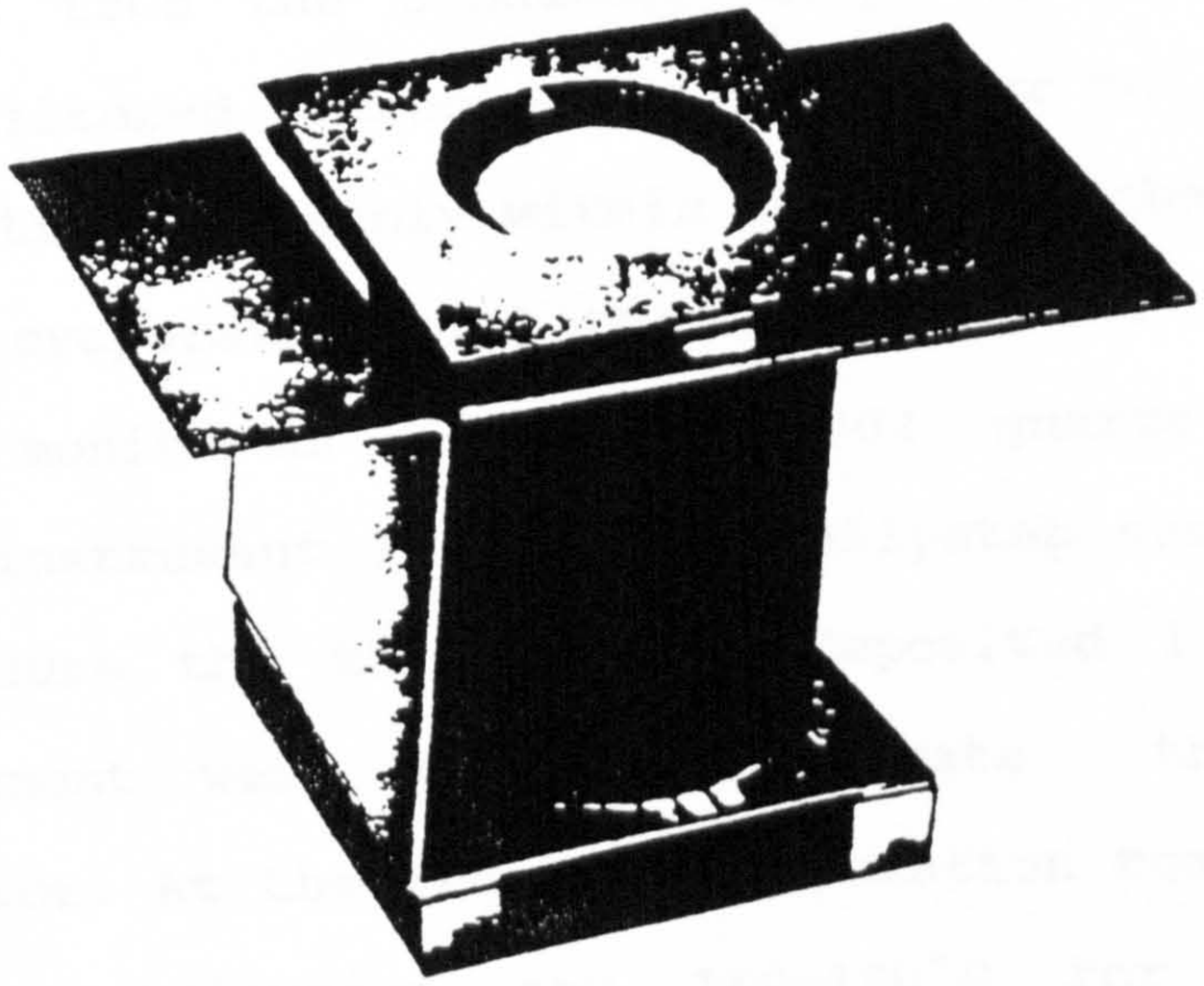


Figure 4.3 A Tantalum Heater Supplied by R.D. Mathis and Used to Heat the Evaporant Material

important role during the growth of thin films. It is essential that the substrate be uniformly cleaned and free from extraneous matter.

The presence of dust particles on the substrates during deposition leads to pin holes in the films, which can result in deterioration of the film properties.

The contamination on the substrate surface might be due to inorganic particles. Such contamination comes from atmospheric born dust and/or skin and clothing particles and some times from solvent impurities and skin oils.

The substrates to be used were first cleaned in a solution of Decon 90 and distilled water in a ratio of 1:6 and then placed in an ultrasonic bath for twenty minutes. They were then thoroughly rinsed in deionised water and then in methanol, followed by a further rinse in an isopropyle alcohol condenser for several hours. After removal from the condenser they were immediately dried using filtered nitrogen gas just prior to insertion into the substrate assembly within the vacuum chamber.

The rate of evaporation and thickness of the deposited films were monitored using a IL002 quartz crystal monitor. An instrument known as a Tallystep was used to directly measure the thickness of deposited layers and such measurement were used to calibrate the quartz crystal monitor. At the required evaporation temperature, 220-240^{o}C for tellurium and 160-190°C for Cd, the alternate layers of tellurium and cadmium could be deposited.

4.2 The Annealing System :

Once the stack of repeated cadmium and tellurium thin films were deposited it was then necessary to thermally anneal the layers to react them to form cadmium telluride. A diagram of the system used is shown in fig.4.4.

The system consisted of a glass bell jar mounted on a stainless steel base plate.A rotary pump attached to the system was used to produce a vacuum pressure of the order of 10^{-2} torr. It was possible to admit nitrogen to the system via a gas inlet valve to permit annealing of the samples in a nitrogen environment. The samples were annealed using a resistively heated tantalum boat which had a 2mm thick copper plate placed on it to more uniformly heat the Cd/Te stacks. The temperature of copper plate was monitored using a K-type thermocouple inserted into a hole drilled into the copper plate.
The boat was heated by passing a large current through it via a transformer rated 240 volts, 10 Amps primary and 12 volts, 200 amps secondary. The transformer in turn was connected to a 0-240 volts variac permitting the annealing temperature to be increased up to 600 C.

4.3 The Deposition System for CdS Thin Films

A diagram of the deposition system is given in fig.4.5. The deposition system consisted of a glass bell jar mounted on a stainless steel base plate which was evacuated to a pressure in the range 10^{-6}-10^{-7} Torr using an oil diffusion pump backed by rotary pump. The

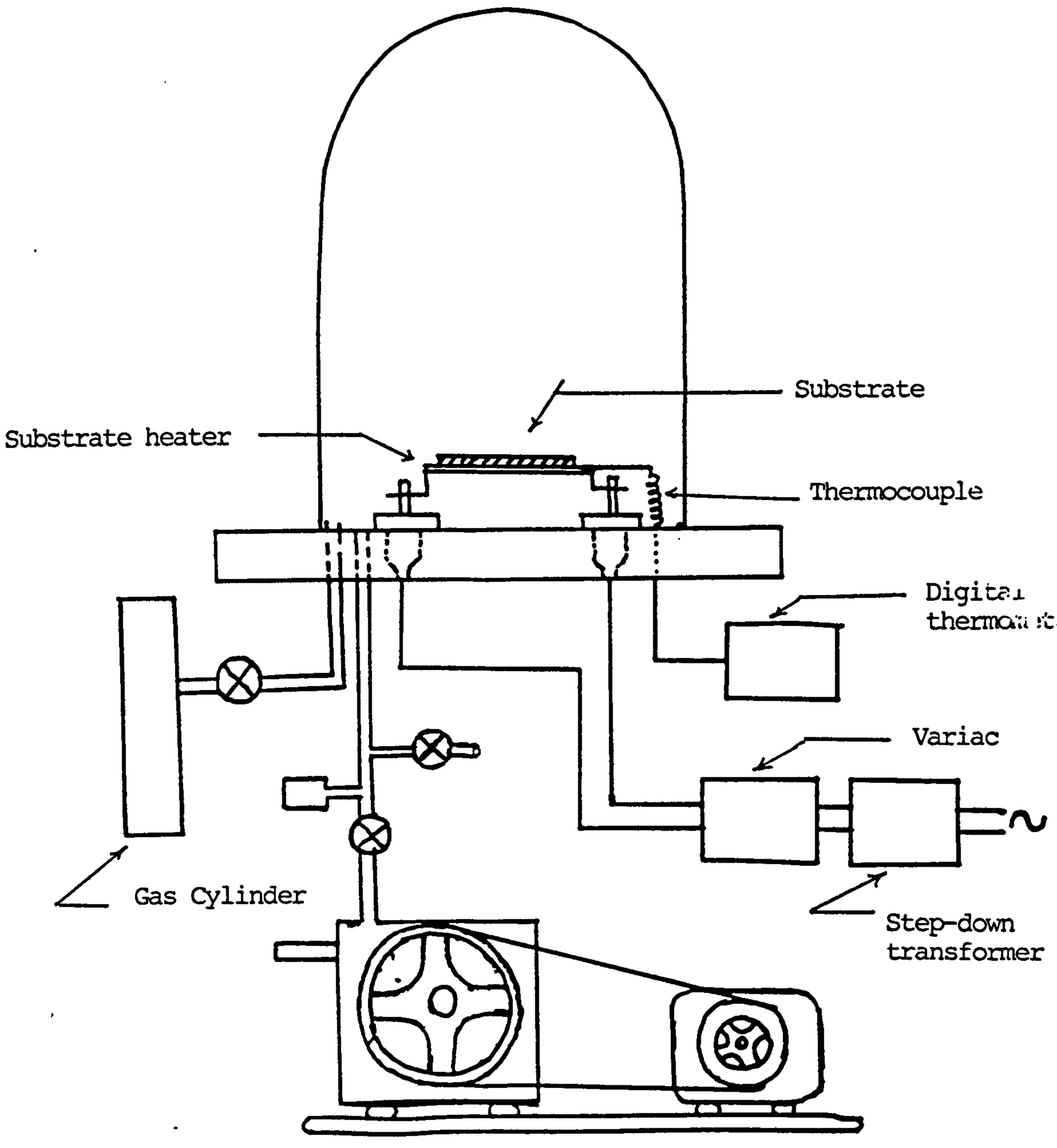


Figure 4.4 Annealing System Used for SEL Processing of CdTe

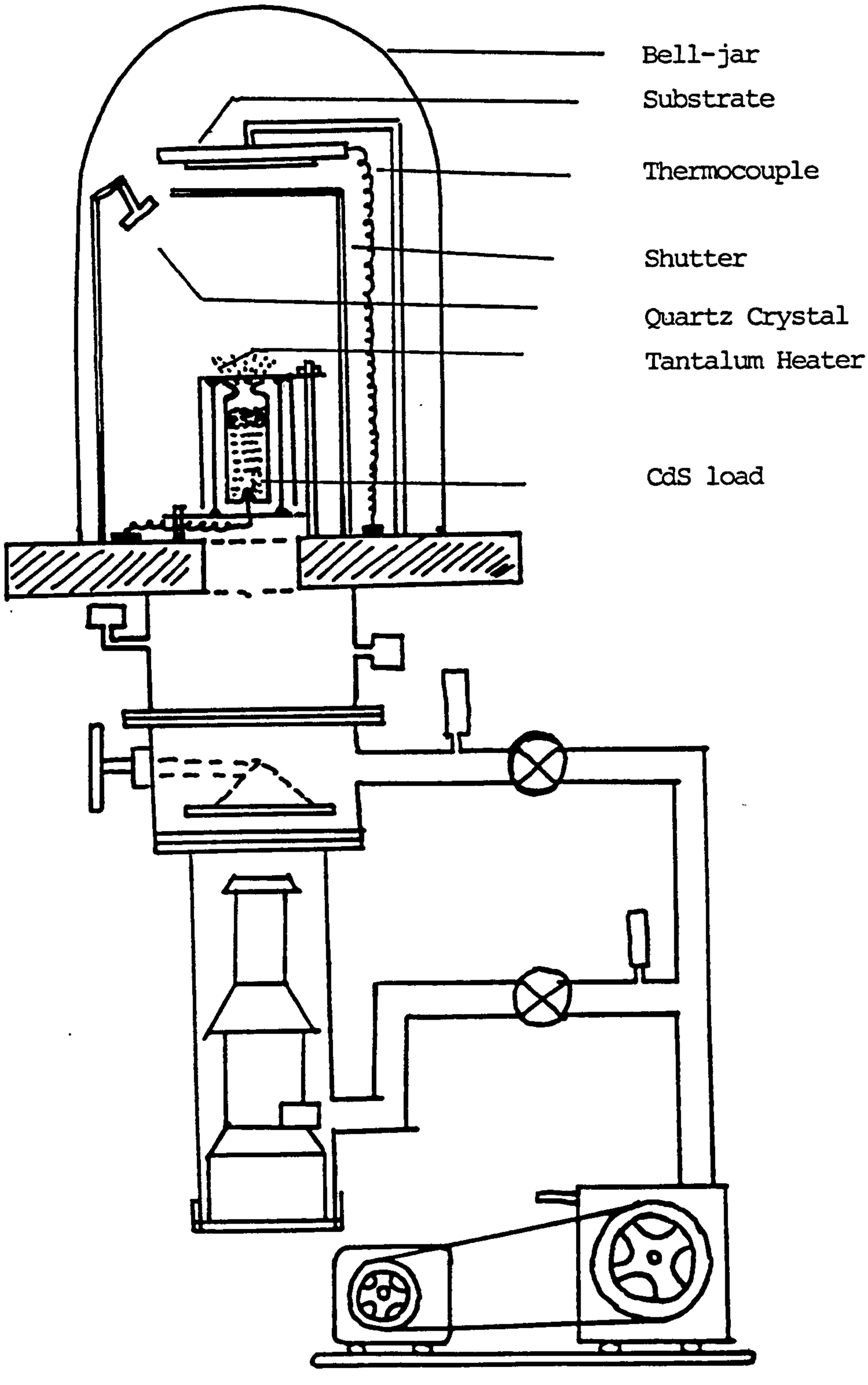


Figure 4.5 The Deposition System Used to Deposit Cadmium Sulphide Thin Films

substrates were heated using a 350w circular resistance heater and the temperature monitored using a K-type thermocouple operating in the range (0-1100°C). The thermocouple was used to provide feedback to a temperature controller which could programmed in an "auto" or "manual" mode.

A tantalum source heater supplied by R.D.Mathis Co. was used to heat the material to be evaporated. The power supplied to the heater using a programmable temperature controller (type 455 controller/programmers with 504 thyrister switches supplied by C.R.L. Ltd) [1]. A K-type thermocouple supplied by T.C.Ltd. was used to monitor the temperature of the evaporant and to provide feedback to the temperature controller.

A cylindrical quartz crucible with a narrow opening at the top end was used to contain the evaporant material. Quartz wool was added above the evaporant material to avoid the ejection of lumps of heated material.

Such a type of arrangement of quartz crucible and tantalum heater (similar to one used by Himrane [2]) permitted the evaporant to be heated uniformly up to a temperature of 1100°C.

A quartz crystal monitor (model IL002, supplied by Intellimetrics) was used to monitor the rate of the evaporation and thicknesses of the films deposited. Continuous water cooling was supplied to the quartz crystal operated using a freq. of 6 MHz during the evaporation. A manual shutter close to the substrate was used to control the deposition time.

4.4 Optical Transmittance and Reflectance Measurements of CdTe and CdS Thin Films:

A Cary 17-D spectrophotometer was used to measure the variation of the transmittance and reflectance of a semiconductor sample with wavelength of incident light within the a spectral range, 3500 - 180 nm. A block diagram of the instrument is shown in fig.4.6. Light from the lamp enters the monochromator which disperses the light and a particular wavelength is selected with the use of a narrow slit. Light of the selected wavelength strikes the rotating mirror which directs the light beam alternatively through the sample and reference path. The two light beams converge on a detector and the relative intensties of the two beams which strike the detector provide a measurement of the amount of light absorbed or transmitted by the sample.

The absorption or transmittance versus wavelength measurements were automated using a "scan-drive system" which changed the wavelength setting of the monochromator and which drove the chart recorder.

For transmittance measurements the light beam was incident on the substrate material i.e soda lime glass or Corning 7059 glass and the Cary 17-D was adjusted for 100 % transmittance over the wavelength range 0.4 to 2.5 um. The substrate material was then replaced by the semiconductor sample i.e. the CdTe, CdS or I.T.O. thin film deposited on the substrate using a lever outside of the sample compartment. Using this arrangement the

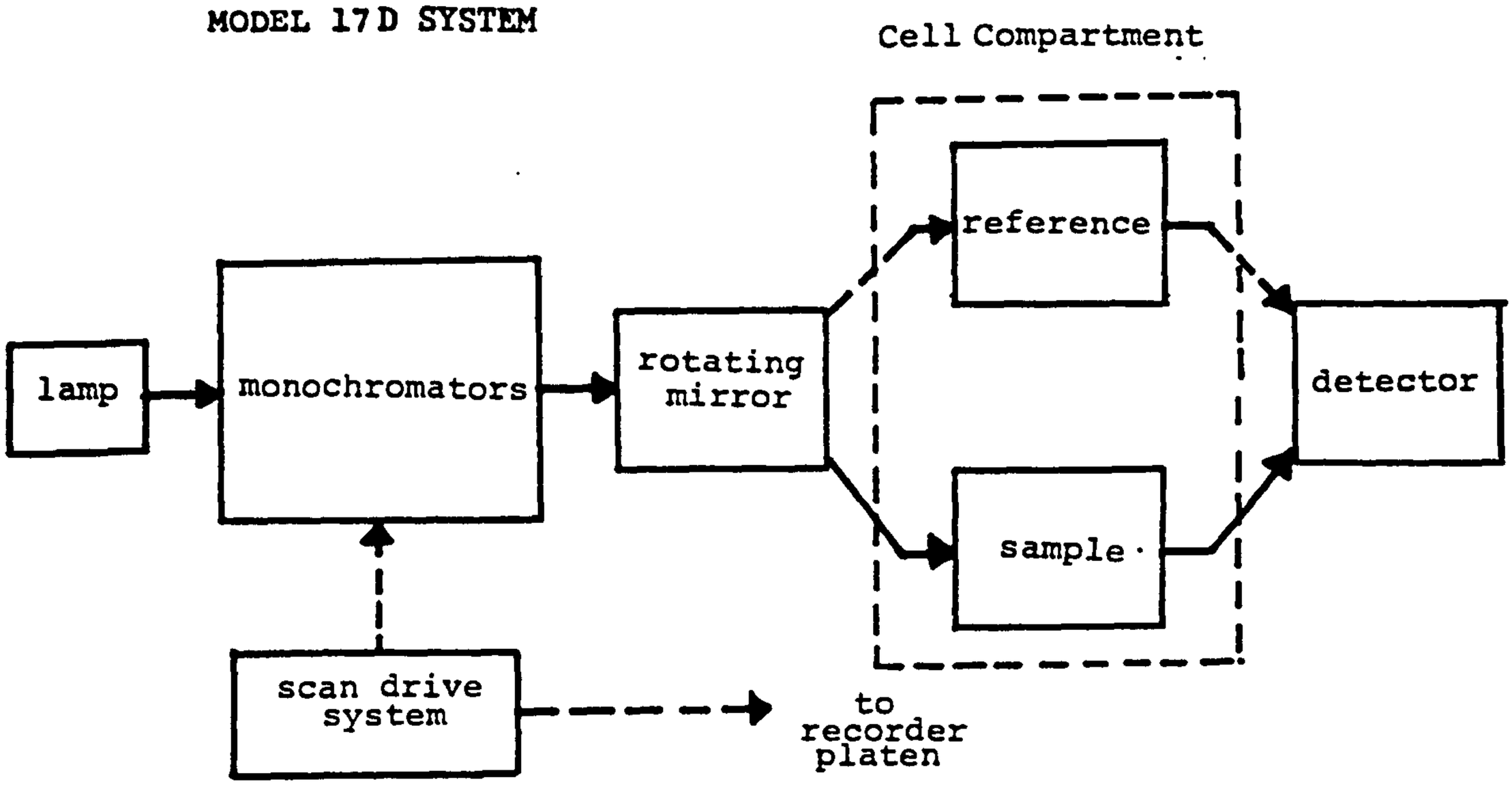


Figure 4.6 Block diagram of the Model 17D optical system

FIGURE

transmittance through the film was compared with the 100 % transmittance through the substrate. Such an arrangement is shown in fig.4.7.

For reflectance measurements, the percentage of light reflected from a reference mirror was measured over the wavelength range 0.4 to 2.5 um and then the mirror was replaced with the thin film deposited on the soda lime glass or Corning 7059 glass substrate. By comparing the reflectance of the sample with the reference, the percentage of light reflected at a given wavelength was measured.

The transmittance and reflectance values at a given wavelength were used to calculate the absorption coefficient, α, at that wavelength using the expression given by Ray[3,4,5]:

$$\alpha = (- 1/d)[\ln T / (1-R)^2] \qquad 4.1$$

where d is the sample thickness. By calculating the values of α for wavelengths in the range 400-2000nm it was possible to plot graphs of α versus hv and $(\alpha hv)^2$ versus (hv)[see section 2.4].

4.5 Measurement of Film Thickness:

The talystep was used to determine the thickness of the Cd and Te layers and the CdS layers. A schematic diagram of the tallystep is given in fig.4.8. The stylus is traversed across the sample surface and its vertical movement converted into an electrical signal, which is

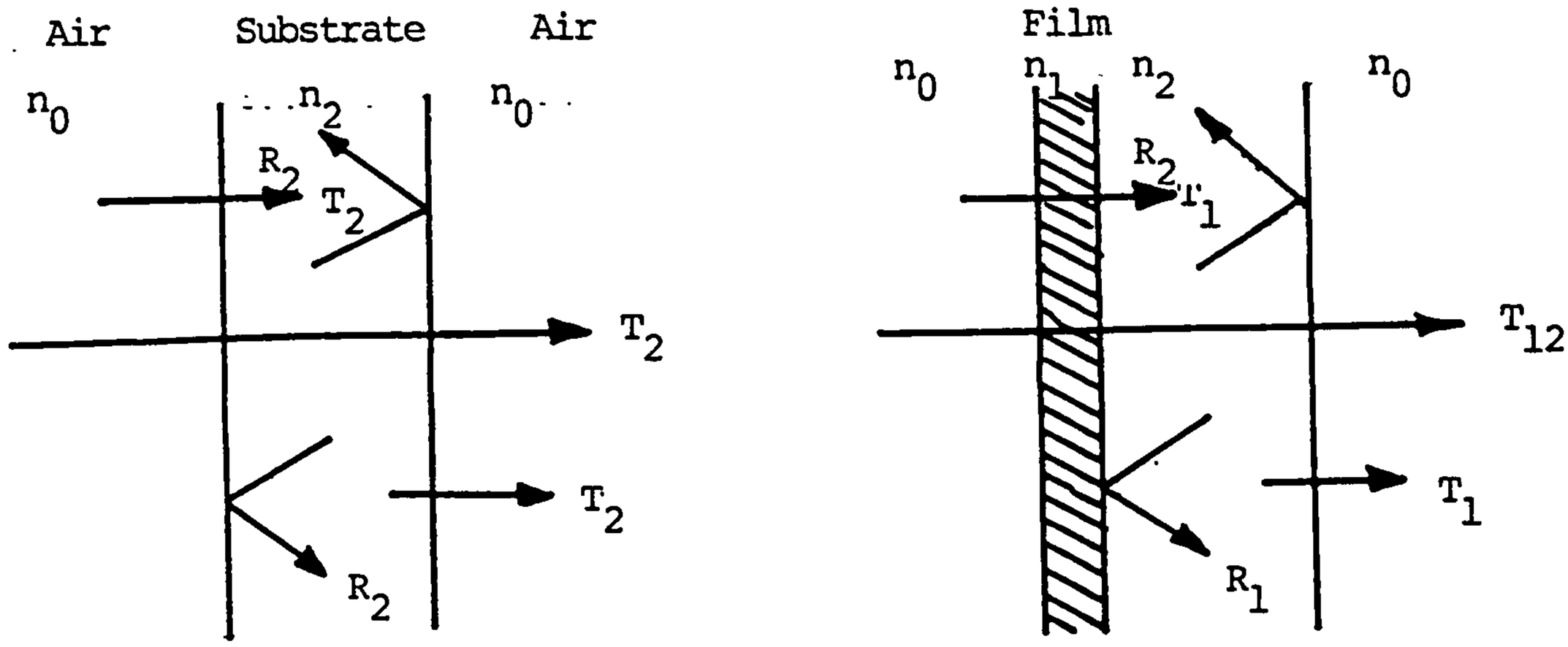


Figure 4.7 (a) Tranmittance Measurements

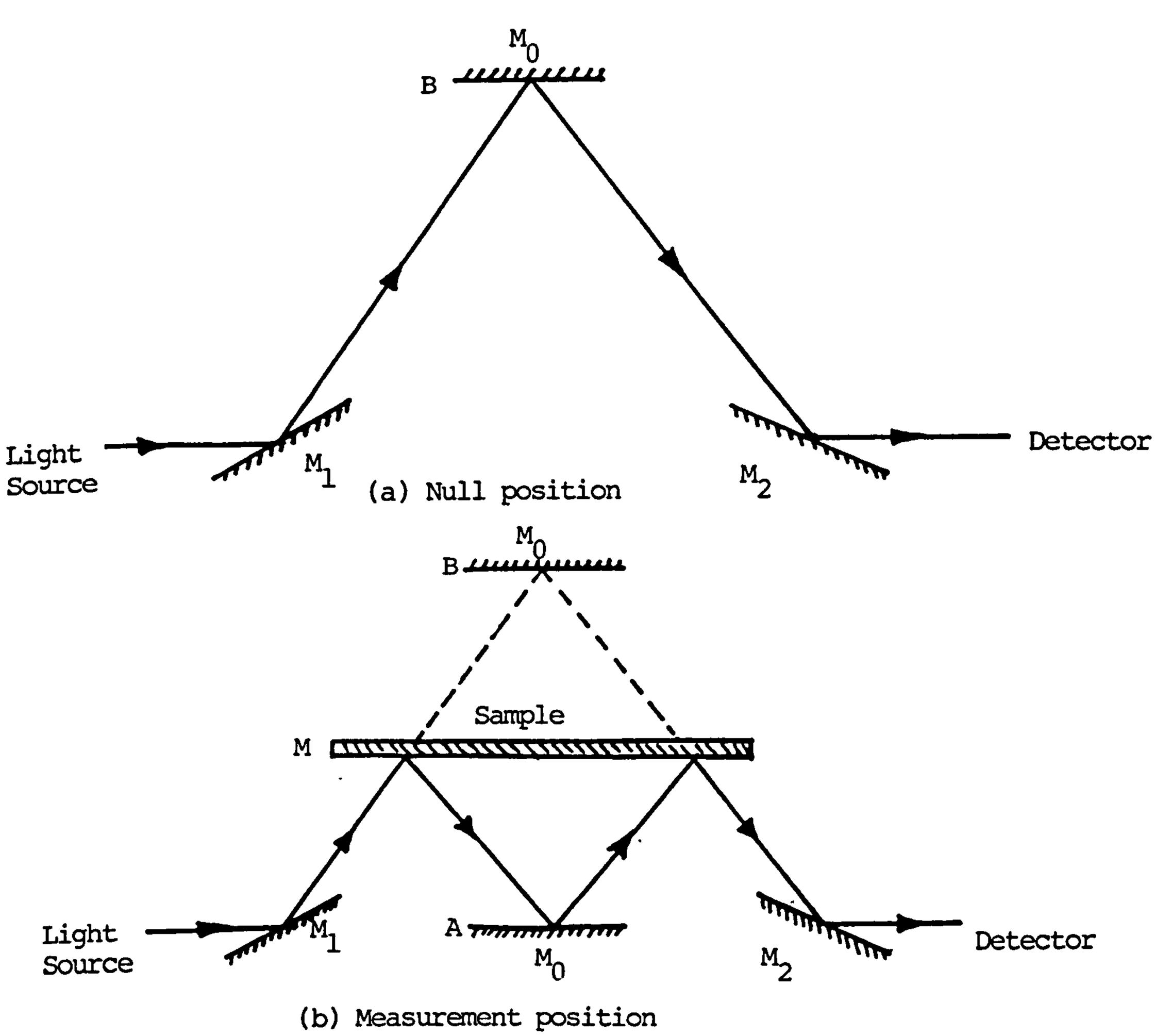


Figure 4.7 (b) Reflectance Measurements (V-W)

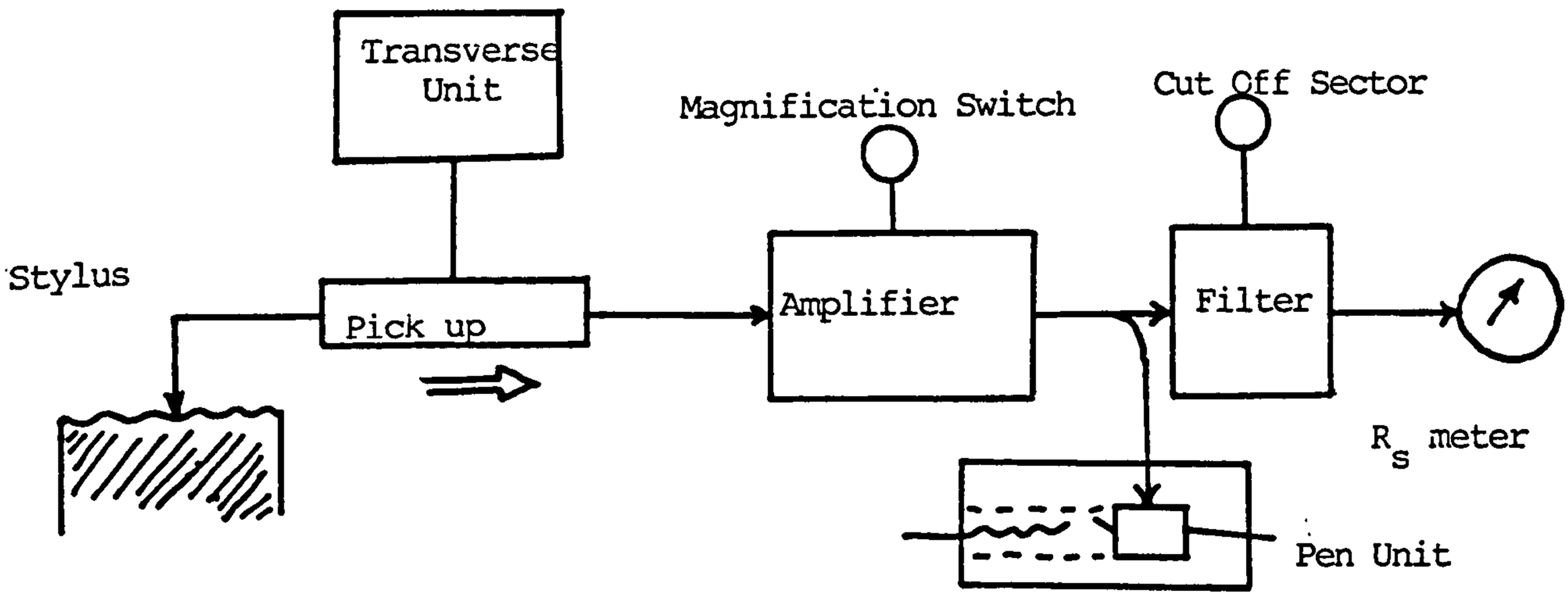


Figure 4.8 Block Diagram of Talystep

amplified and used to operate the recorder. The sensitivity of the instrument was such that it would respond to changes of thickness of + 0.01 um.

To obtain accurate measurements for the thickness of the films with different surface roughnesses an electronic filter with a cut-off facility was built into the instrument. Care was taken to avoid external vibration because with such a sensitive instrument these could effect the readings taken.

4.6 Methods Used to Determine the Electrical Properties of Films Deposited:

(i) Four-Point Probe Method :

The four point probe method was adapted for semiconductor resistivity measurement by Valides in 1954 [6]. As shown in fig.4.9 the probes are arranged in-line with equal spacings S_1, S_2 and S_3. A constant current source (225 supplied by Keithly Instruments) is used to pass a current through the outer probes, 1 and 4, respectively and a Solartron, 7065 microprocessor voltmeter was connected across the two inner probes, 2 and 3. The potentials at points 2 and 3 are given by the following formulae [6] :-

$$V_2 = @I/2\pi \{1/S_1 - 1/(S_1 + S_3)\} \qquad 4.2$$

and

$$V_3 = @I/2\pi \{1/(S_1 + S_2) - 1/S_1\} \qquad 4.3$$

Thus the measured voltage between the pt 2 and 3 becomes

$$V = V_2 - V_3 \qquad 4.4$$

$$V = @I/2\pi \{1/S_1 + 1/S_3 - 1/(S_2 + S_3) - 1/(S_1 + S_2)\} \qquad 4.5$$

For four point probe spacings that are equal i.e

$S = S_1 = S_2 = S_3$, the above equation reduces to

$$@ = 2\pi S(V/I) \qquad 4.6$$

For greater accuracy $@ = 2\pi S(V/I)F$ 4.7

where F is a constant which is the product of several independent correction factors :-

$$F = F_1 F_3 \{\ln(2)F_2/\pi\} \qquad 4.8$$

F_1 corrects for sample thickness, F_2 corrects for lateral dimensions, and F3 corrects for the placement of the probes relative to the samples edges.

For very thin film samples for which F_2 and F_3 reduce to unity [7]. It can be shown that :-

$$@ = (\pi t/\ln(2))(V/I) = 4.532\ t\ (V/I) \qquad 4.9$$

The sheet resistance, $@_s$ expressed in units of ohms per square is given by,

$$\rho_s = \rho/t = (\pi/\ln(2))(V/I) = 4.532(V/I) \qquad 4.10$$

Large currents may cause resistive heating with the sample and cause significant errors in the measurements and hence the current used for such measurements was kept sufficiently small to avoid the I-V characteristic becoming non-linear.

(ii) Van der Pauw Method :-

Van der Pauw [8,9] derived an expression for the specific resistivity of a flat sample of irregular shape which would be valid if the following conditions are met

1. The contacts should be at the periphery of the sample.
2. The contacts must be negligibly small.
3 The thickness of the sample should be uniform over the entire surface area. and
4. The sample should not contain isolated holes.

For the sample of the arbitrary shape and thickness, t, given in fig.4.10 the resistivity is given by :-

$$\rho = \{\pi t/\ln(2)\}\{(R_{12,34} + R_{23,41})F/2 \qquad 4.11$$

where the resistance $R_{12,34}$ is defined as

$R_{12,34} = V_{34}/I_{12}$ i.e the ratio the voltage across the terminals, 3 and 4 and current passed between terminals 1 and 2 and

$$R_{23,41} = V_{41}/I_{23} \qquad 4.12$$

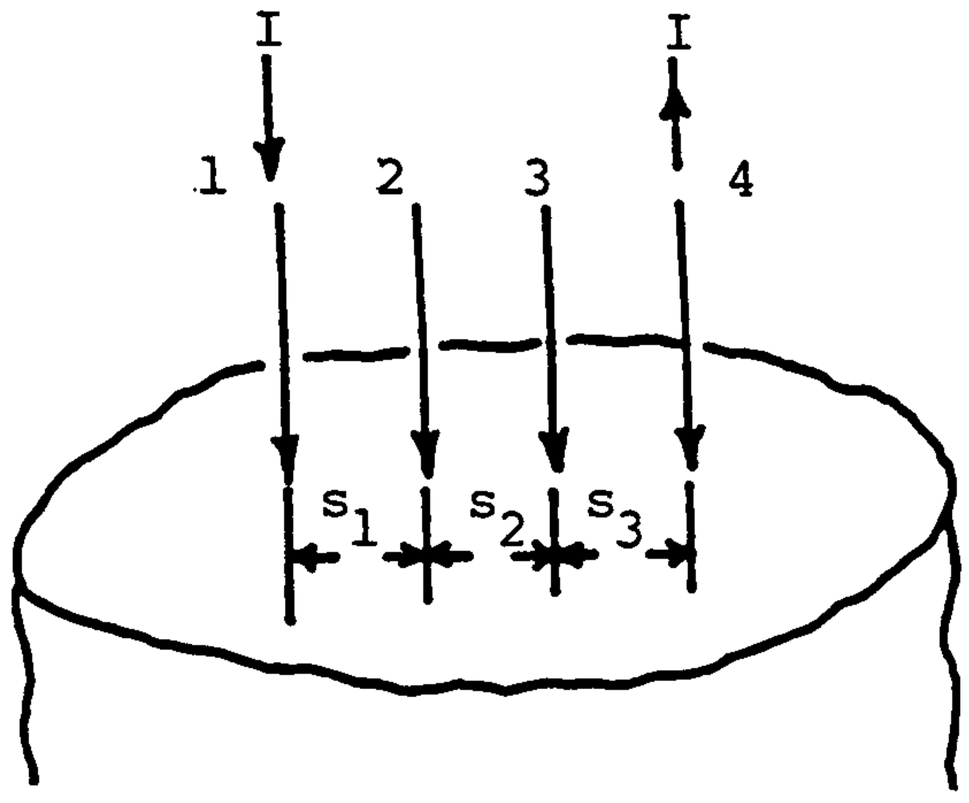
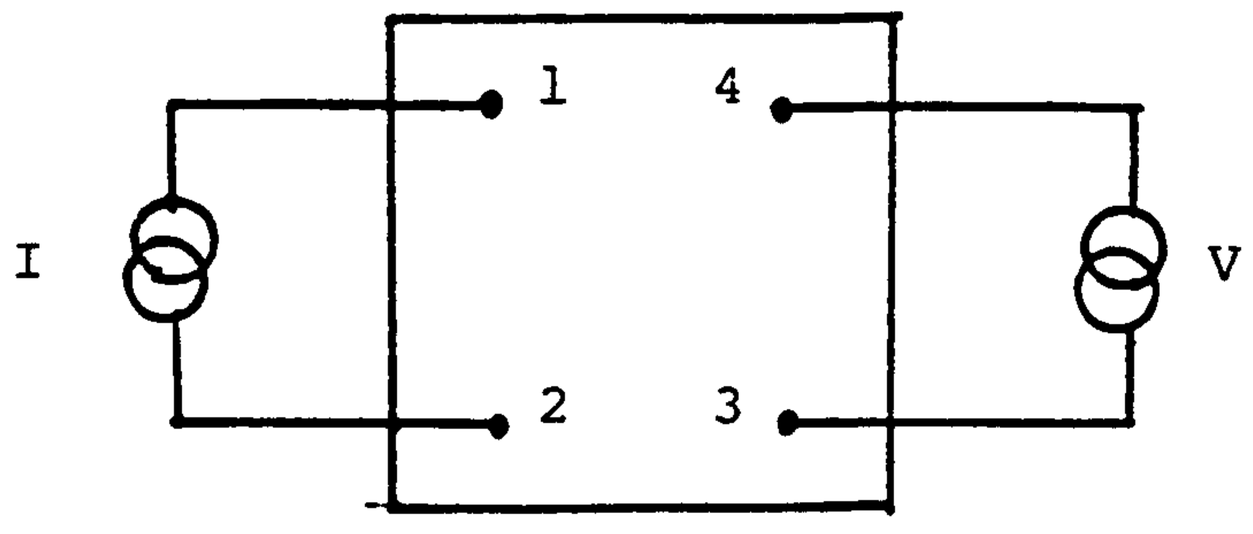
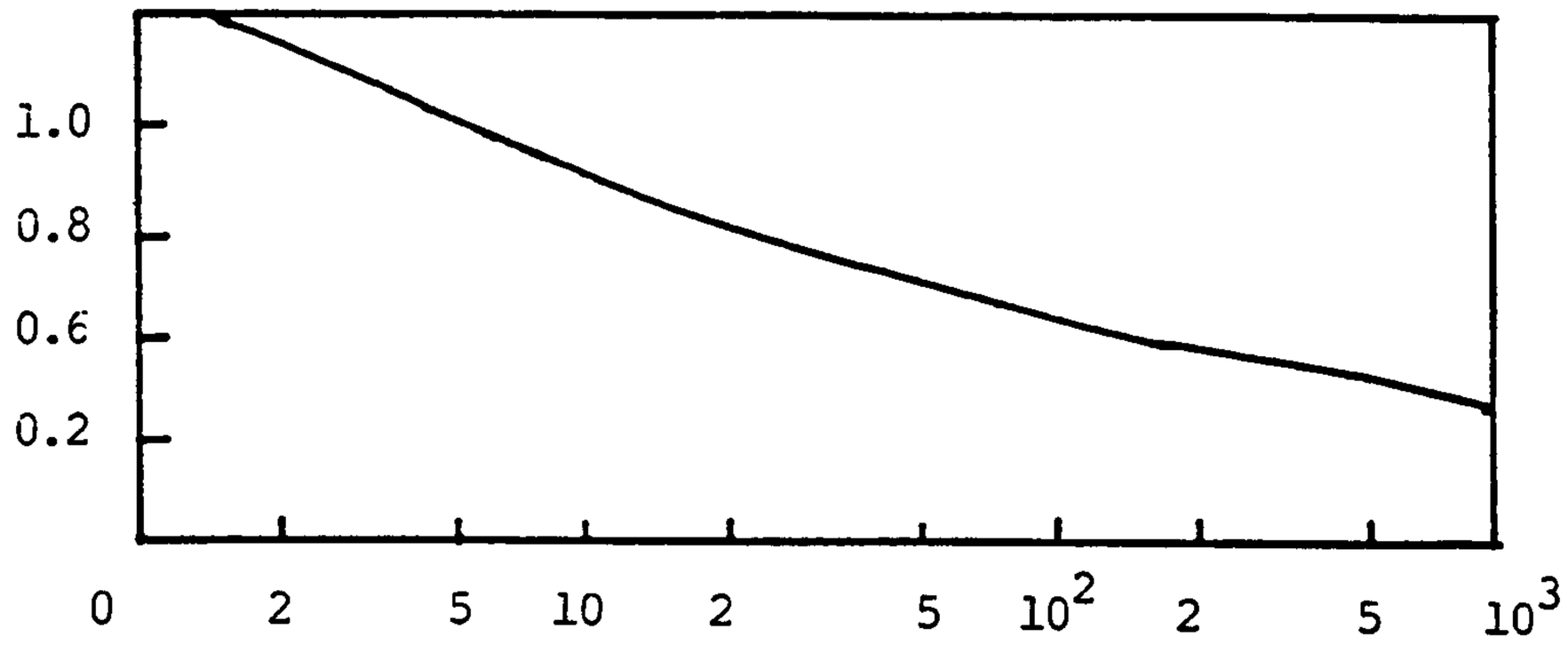
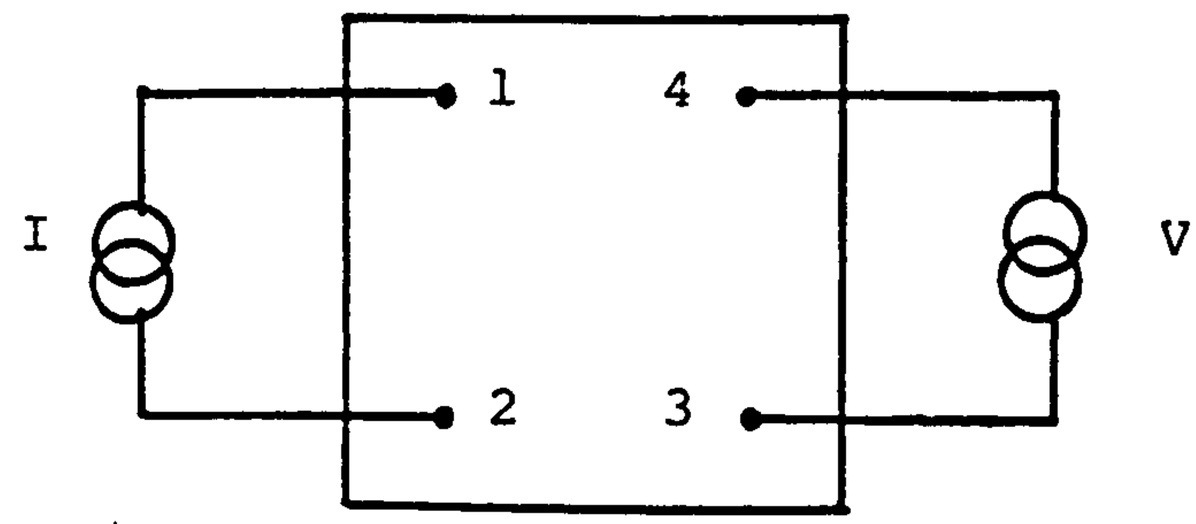


Figure 4.9 A Colinear Four-point Probe





(a)



(b)

Figure 4.10 Experimental Arrangement for Using the Van der Pauw Technique to Measure the Resistivity and Hall Constant

i.e. the ratio of the voltage across terminals 4 and 1 to the current passed between terminals 2 and 3. Therefore, the sheet resistivity is given by

$$\begin{aligned} \rho_s &= \{\pi/\ln(2)\}(R_{12,34} + R_{23,41})F/2 \\ &= 4.532\ (R_{12,34} + R_{23,41})F/2 \end{aligned} \qquad 4.13$$

The Van der Pauw equations assume the use of very small contacts, but actually the influence of non-ideal contacts has been calculated. Errors associated with non ideal contacts can be eliminated if either a Clover-leaf or a Maltese cross geometry is used [8,10]. In this work the evaporated gold was used as the contact material to the layers. The gold contact pads were deposited at the four corners of the square shaped CdTe samples. Silver paint was then used to attach wires to the gold pads. The contacts for the square shaped samples could also be made at the mid position of each the sides rather than at the corners [11] and the results from such measurements compared to the former arrangements.

When a magnetic field is applied at right angles to the current, a potential difference, V_H, is produced across the film in a direction mutually perpendicular to the current, I, and magnetic field, B, and its magnituide is directly proportional to the product of current density and magnetic flux density and inversely proportional to the film thickness i.e.

$$V_H \propto BI/t \quad \text{or} \quad V_H = R_H BI/t \qquad 4.14$$

where R_H is the "Hall constant" of the material. The Hall mobility, μ_H, is defined by :-

$\mu_H = R_H/@$ where @ is the bulk resistivity of the sample.

If the sample is assumed to be uniformly doped and for n-type material, electron conduction dominates and for p-type material hole conduction dominates (i.e. we can assume we do not have "mixed conduction" [12] (which is true for wide bandgap semiconductors) then the electron concentration in n-type material, n, and the hole concentration, p, in p-type material are given by :

$n = 1/R_He$ for the R_H determined for the n-type material and $p = 1/R_He$ for the R_H determined for the p-type material.

4.7 Thermoelectric Measurements

When two probes one hot, and the other cold, are placed in contact with a semiconductor, charge carriers diffuse from the hot region to cold region of the semiconductor. For a n-type semiconductor the hot end appears to be positive relative to the cold end and vice versa for a p-type semiconductor. The transport of the charge carriers creates a potential difference between two probes and a "thermal E.M.F." is said to be generated. The magnitude of the thermal E.M.F. depends on the temperature difference between the cold and the hot probes and is given by [13]:-

$$E = \alpha_T \blacktriangle T \qquad 4.15$$

α_T is the "thermoelectric co-efficient" expressed as the potential difference per degree C change in temperature between the cold and hot junction. This quantity is related to the density and effective mass,

m^*, of the charge carriers by the Pisarki formula [14-17]:-

$$\alpha_T = \pm(k/q)\{B+\ln 2(2\pi m^* kT)/nh^3\} \qquad 4.16$$

B is a constant which depends on the dominant "scattering mechanism" within the semiconductor sample. The following values of B are given by [13]:-

B = 1 for amorphous semiconductors

B = 2 for acoustic phonon scattering.

B = 3 for (polar) optical phonon scattering.

B = 4 for ionized impurity scattering, and

B = 2.5 for neutral impurity scattering.

A diagram of the apparatus used to determine, α_T, is given in fig.4.11. Essentially E was measured for different values of, $\blacktriangle T$, and from the slope of the resulting graph, α_T, determined.

Assuming that each sample was uniformly doped and that Pisarki formula was valid the carrier concentration was calculated assuming values of B in the range 1 to 4.

4.8 S.E.M Studies:

The scanning electron microscope (S.E.M.) used in this work was a Cambridge Instruments Stereoscan 120

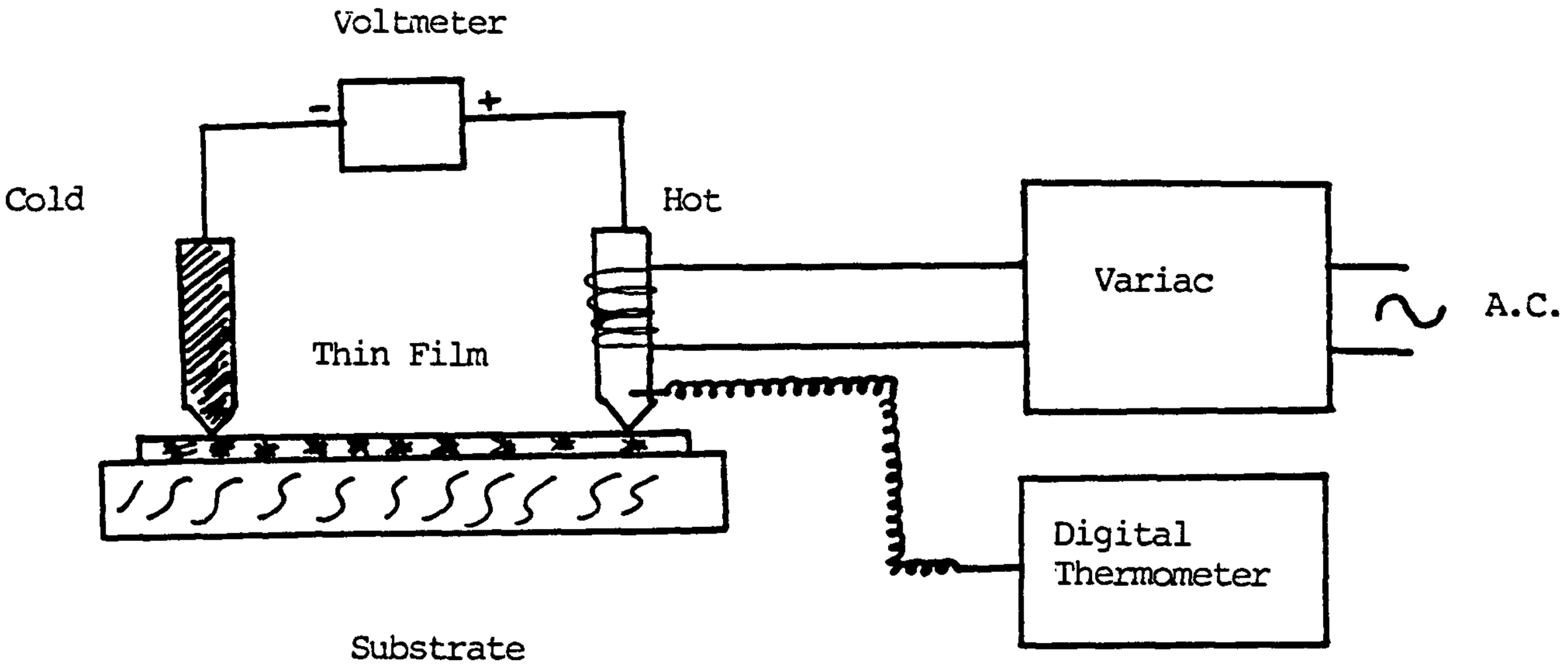


Figure 4.11 Diagram of Hot-probe Apparatus

model. A diagram of the S.E.M. is shown in fig.4.12. The electrons ejected from the electron gun are accelerated towards the anode. After passing through one or more lenses, the image of electron source is formed in the plane of specimen with a diameter of a few tenths to a few tens of nanometeres. A scanning generator "rasters" the electron beam over the surface and the "secondary electrons" produced by the specimen are detected by an "electron collector". An amplifier enhances the signal generated and the amplified signal used to control the intensity of the electron beam in the "display cathode-ray tube". Because the electron beam in this instrument is being scanned in the same way as the main beam in the main electron optical column, an image of thin film is produced. The S.E.M. was used in this work in the "secondary electron mode " to observe the topography and surface morphology of the thin films produced. Such observations also permitted the film thickness and grain size of the films to be measured directly and also to determine whether pinholes were present in the layers.

4.9 X-ray Diffraction :

X-ray diffraction is a very useful, non-destructive method for investigating the properties of materials. A diffraction pattern can only be observed when the incident radiation has a wavelength comparable to the

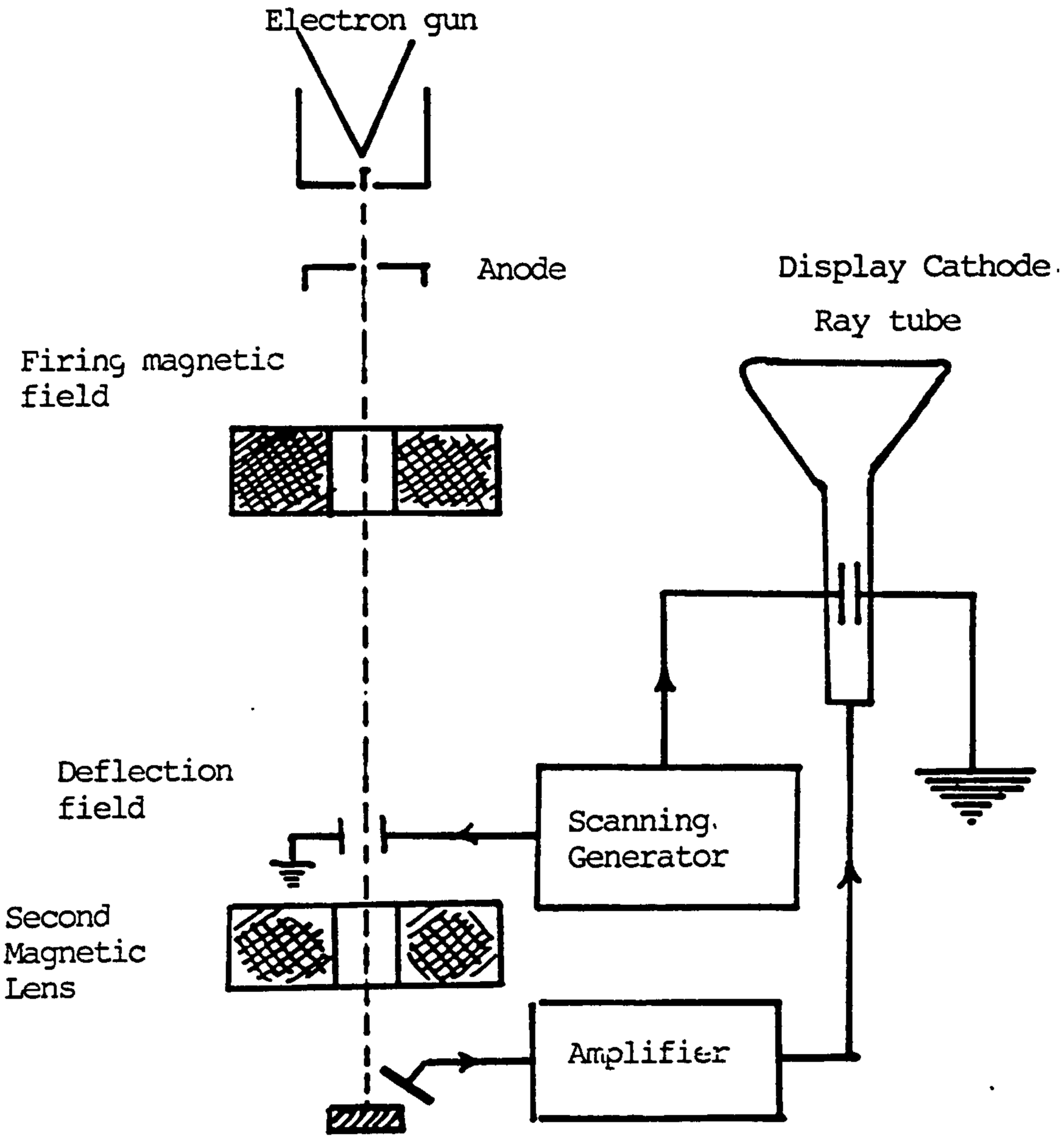


Figure 4.12 Schematic Diagram of SEM

spacing of the crystal planes and further the Bragg condition is satisfied [18]:-

$$n\lambda = 2d \sin\theta \qquad 14.17$$

where $n = 1,2,3,...$

λ = the wavelength of the radiation

d = the inter plane spacing

and θ = the angle of reflection

The films of CdTe produced in this work were polycrystalline and therefore the "powder diffraction method" was used. Using this method the diffraction pattern of a thin film is recorded by measuring the intensity of X-rays reflected from the sample [19]. The instrument used was a Philip PW 1049 / 10 Bragg-Brento diffraction meter which was located in the University of Newcastle. This instrument used CuKα radiation (λ = 1.5418 $\mathring{A}$) and a diagram of this system is shown in fig.4.13. The data obtained is compared to the X-ray powder data collected by the "Joint Committee for Powder Standards" (JCPDS) - part of the American society for testing materials. They give the values of 2θ, corresponding values of d and relative intensities of the X-ray reflections to be obtained from a given compound or element with a particular crystal structure. It is thus possible to identity the compounds or elements present, their crystal structure and possibly their relative proportions in the material from the observed data.

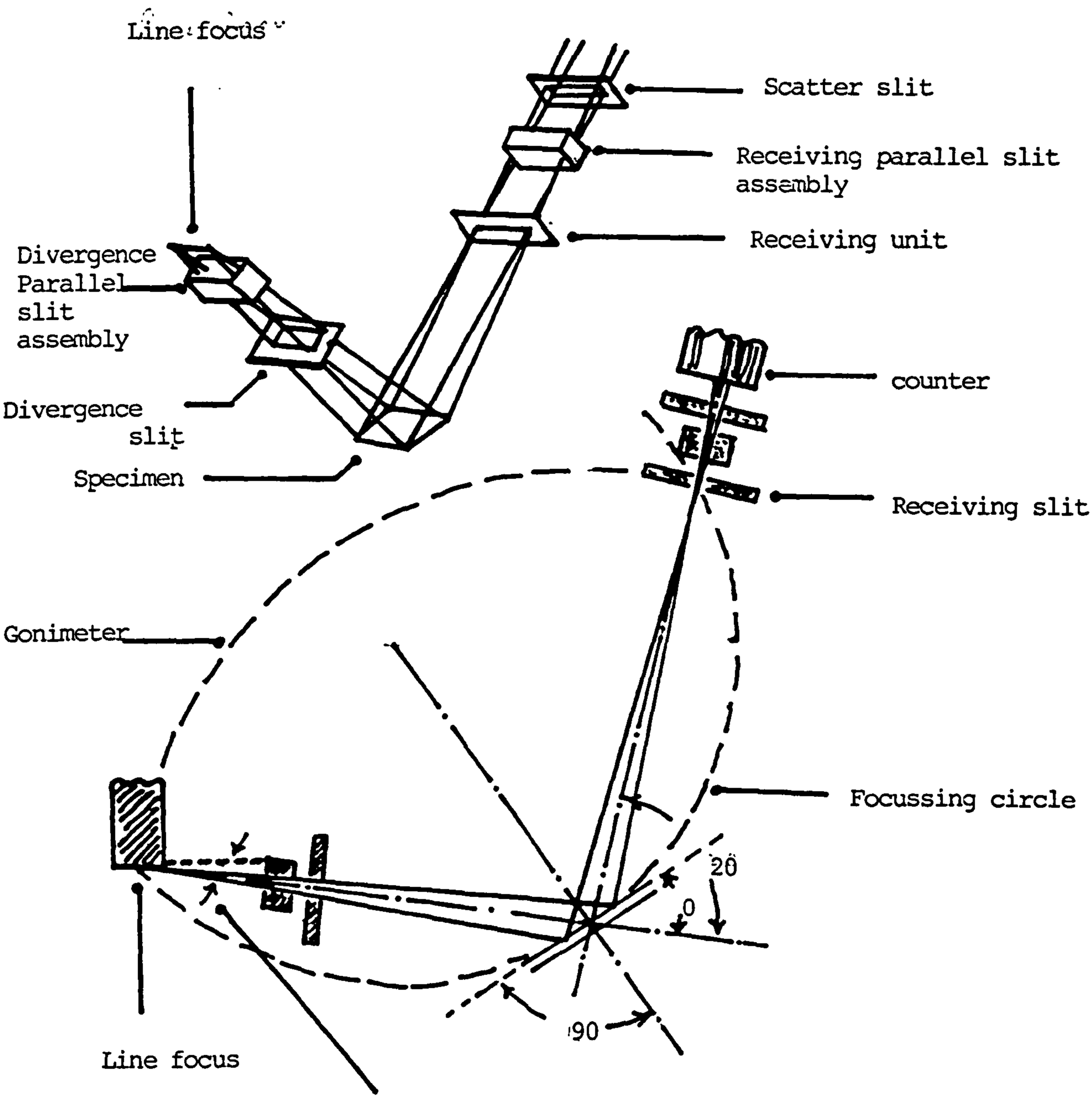


Figure 4.13 The Phillips X-ray Diffroctometer

The finite width of the X-ray diffraction peaks also yields information because the width is related to such important effects as microstrain, faulting and crystal size. For polycrystalline thin films the width is usually related to the grain size [20].

Following the analysis of Scherrer [20,21], the "Crystallite dimension", L, is related to the broadening, B using the following relation :-

$$L = C\lambda / \beta\cos\theta \qquad 4.18$$

L = Crystallite dimension perpendicular to the diffraction plane.

λ = X-ray wavelength

θ = diffraction angle

C = a constant depending on the broadening measurement

B = Broadening on the 2θ scale expressed in radians, due to crystallite size.

If the broadening is measured as the full width half maximum (FWHM), the constant, C, has a value equal to 0.94 [21].

4.10 C-V Measurements:

A computer controlled Hewlett-Packard LCR bridge Model HP 4274A was used to determine the capacitance versus voltage behaviour of the device at different frequencies ranging from 100 Hz to 100 KHz. Such a bridge is capable of measuring the capacitance from PF to Farads. These measurements were done under dark at

ambient temperature of ≈ 16°C. For a fixed selected frequency, the reverse bias voltage was varied from 0 to -2 Volts.

4.11 Spectral Response Measurement:

A diagram of the system used for measuring the spectral response is given in fig.4.14. The light source used was a 50 W tungsten lamp which was supplied with power using a Fornell B30/20 stabilised power supply. The light from the lamp was focussed onto the input slit of a Hillger and Watts manochromator. The monochromator could be manually adjusted so that the light emerging from the output slit had a wavelength in the range 400 - 1000 nm. The emerging light is then focused either onto the solar cell or onto the reference photodiode and the solar cell could be measured directly using a current to voltmeter amplifier and recording the voltage using a digital voltmeter [22]. Spectral response data for the reference silicon photodiode, supplied by the National Physical Laboratory is given in table 4.1.

The spectral response or the "current responsitivity", $R_{I,\lambda}$ of a device is defined as the ratio of the photocurrent, I_p, generated to the power of incident radiation at a given wavelength, p_λ, i.e.

$$R_{I,\lambda} = I_p/p_\lambda \qquad 4.19$$

For solar cell :-

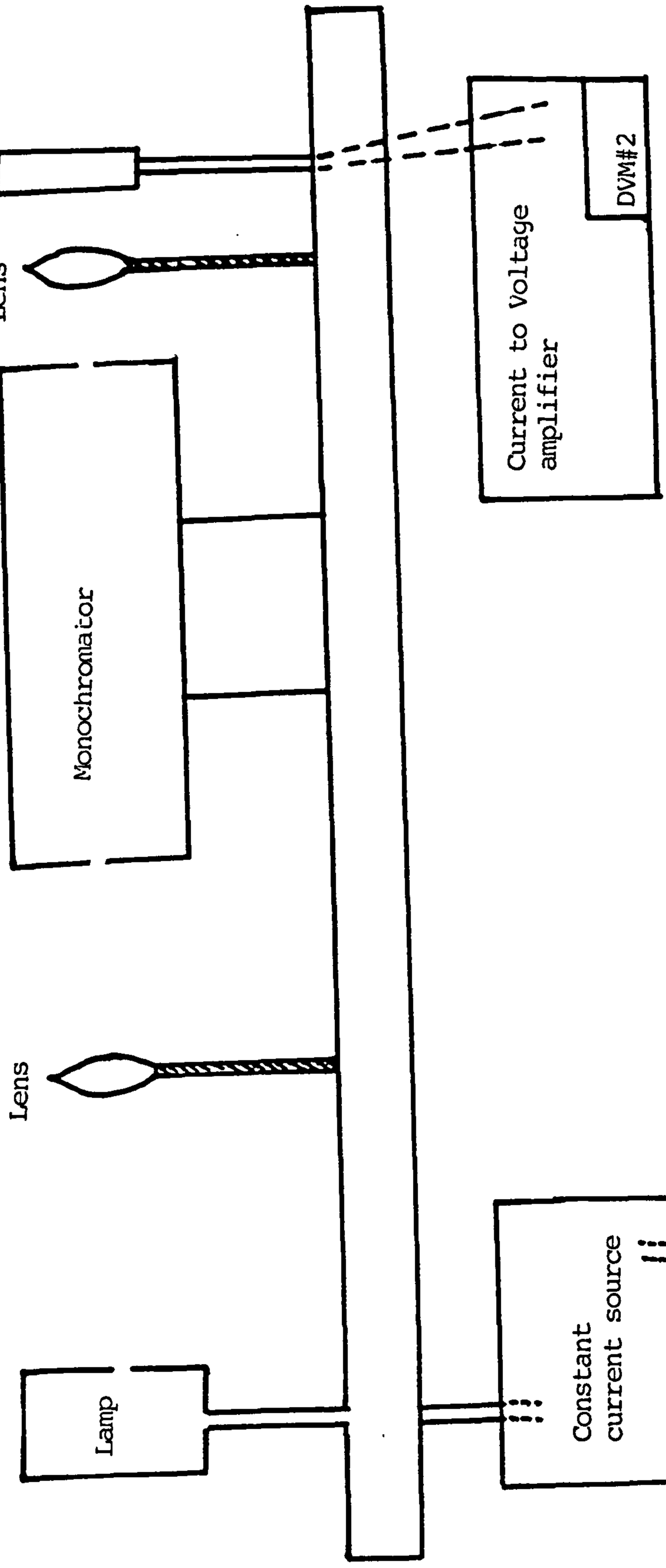


Figure 4.14 Apparatus for Measuring the Spectral Response

Table 4.1 Spectral Response Data for Si Phototdiode.

WAVELENGTH (nm)	RELATIVE RESPONSE	SPECTRAL RESPONSE A/W
546.1	1.000	0.208
600	1.169	0.252
650	1.366	0.284
700	1.600	0.333
750	1.845	0.384
800	2.079	0.432
850	2.269	0.472
900	2.358	0.490
950	2.209	0.459
1000	1.636	0.340

$$R_{s.c.} = (I/p_\lambda)p_1 \qquad 4.20$$

For reference diode :-

$$R_{R.D} = I_{p2}/p_\lambda \qquad 4.21$$

and hence

$$R_{s.c.}=I_{p1}\ \ R_{R.D.}/I_{p2} \qquad 4.22$$

For a given wavelength ,λ , of light incident with power, p_λ, then if I_{p1} and I_{p2} are recorded for the solar cell and reference diode respectively and $R_{R.D.}$ is taken from the table (4A) then the spectral response, $R_{s.c.}$ at that wavelength can be calculated.

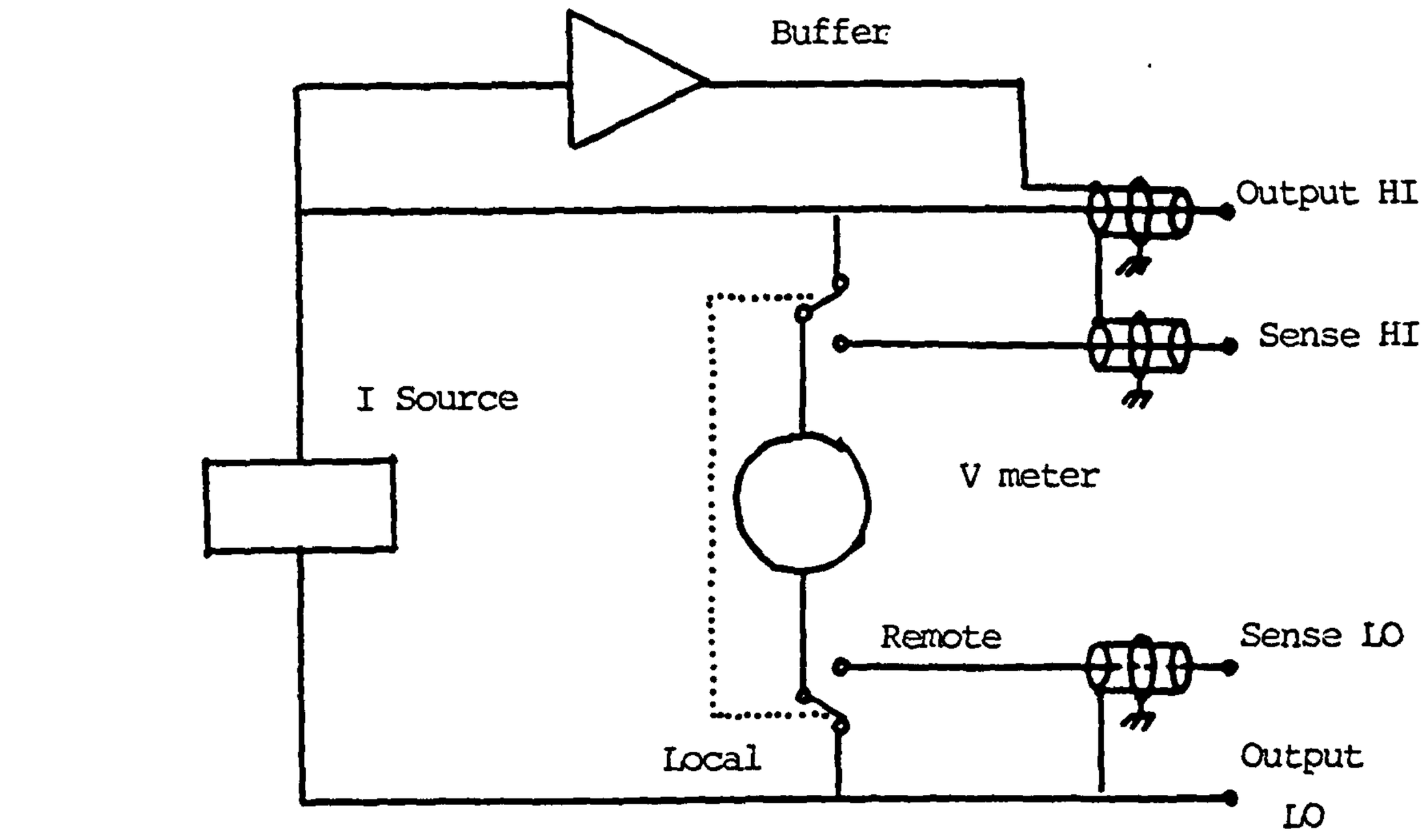
The "quantum efficiency", Q.E., is defined as the number of electron-hole pairs generated per incident photon of light. It is related to the spectral response, $R_{I,\lambda}$, by :-

$$Q.E. = R_{I,\lambda}(hc/q\lambda) \qquad 4.23$$

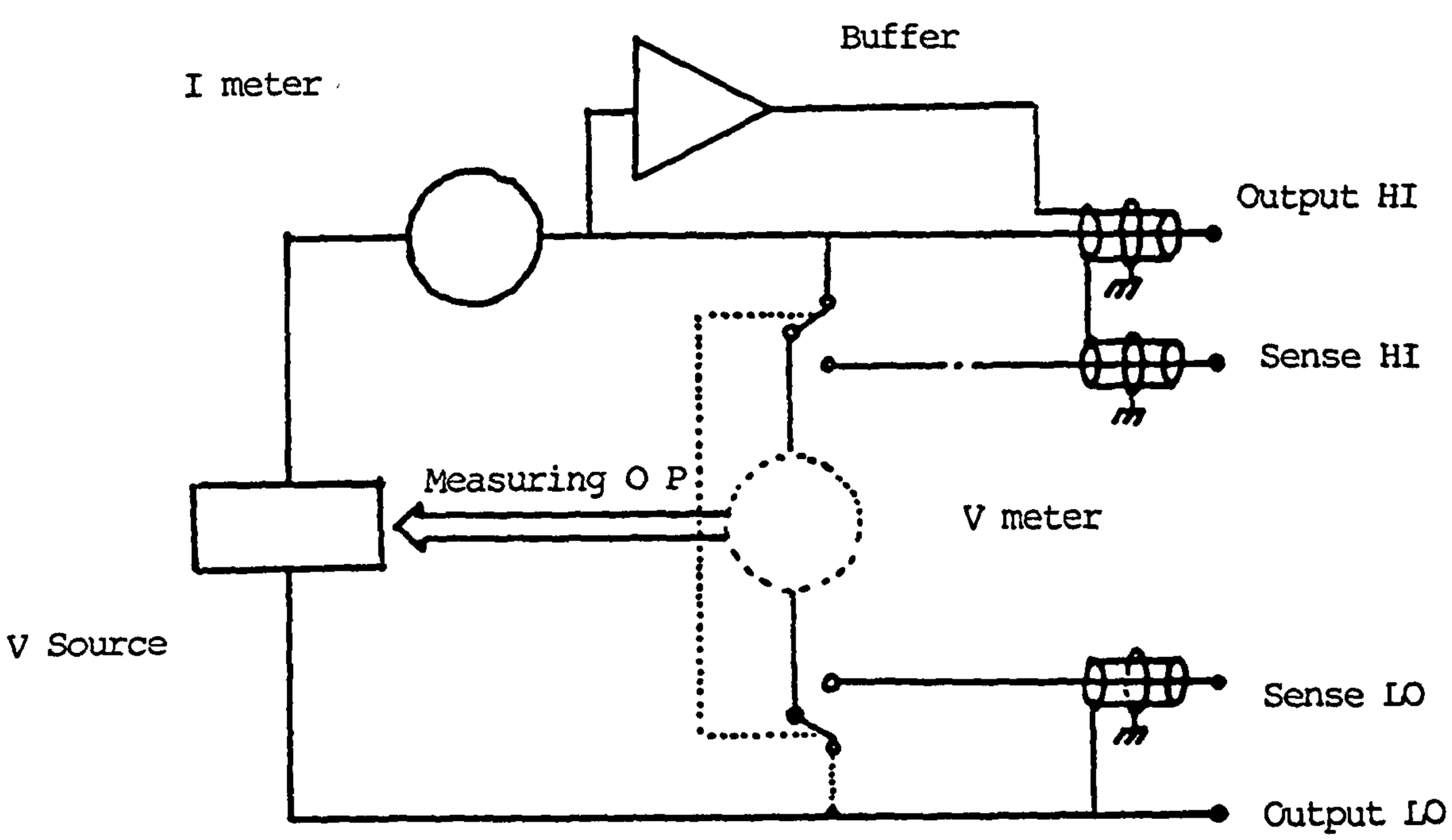
Thus it is possible to present the spectral respose either in the form Q.E. versus λ or $R_{I,\lambda}$ versus λ.

4.12 I-V Measurements:

The I-V characteristics of the solar cells produced were measured using the system shown in fig.4.15 The Keithly Instruments " 238 current source measurement unit " was



(a)



(b)

Figure 4.15 Connection Used to

(a) Supply I, Measure V

(b) Supply V, Measure I

the most important part of the system. This instrument could supply a constant current and measure the corresponding voltage across the device or supply a constant voltage and measure the corresponding current through the device. The instrument was designed to be interfaced easily to a bench top computer, in this case a Nimbus computer, so that the setting of the constant current or constant voltage and recording of the corresponding voltage or current could be controlled using computer software. The temperatures could be altered in the range (-20 to 90 °C) by altering the temperature of the water bath under the base plate permitting the I-V to be measured at different temperatures in this range.

For measuring the I-V characteristics under illumination a 2 kW tungsten lamp was used as a source of light. The intensity of light incident onto the samples under test was adjusted to be the intensity corresponding to that of an A.M.O. spectrum by using a GaAs standard cell [23]. For the "simulated A.M.O spectrum" incident on the solar cell the I-V characteristic under illumination could be displayed on the computer console and the output parameters obtained i.e. $V_{o.c.}$, $J_{s.c.}$, F.F. and A.

The intensity of light incident on the solar cells could be easily altered by placing the metallic grids between the light source and the solar cell. Altering the intensity of light incident in this way permitted corresponding values of $V_{o.c.}$ and $J_{o.c.}$ to be determined for the each different intensity of light incident on the

solar cell because :

$$V_{o.c.} = AkT/q \ln(J_{s.c.}/J_o) \qquad 4.24$$

A plot of ln $J_{s.c.}$ versus $V_{o.c.}$ enables J_o and A to be determined from the slopes and intercepts of the straight line graphs obtained.

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CHAPTER V

RESULTS AND DISCUSSION

5.1 The Morphology of the CdS Films Deposited:

The CdS films deposited were observed directly in a scanning electron microscope using the secondary electron mode of operation. Films with thickness > 1.5μm were found to be free from pinholes and for substrate temperatures > 200°C to consist of columnar grains as shown in fig.5.1. For a substrate temperature of 200 °C the lateral grain size was typically 1-2μm. These observations are consistent with those of other workers [1,2]. The achievement of columnar grain growth was essential because the Cd and Te layers were to be deposited onto CdS/I.T.O./glass substrates and then reacted to form CdTe. It was anticipated that better CdTe layers would be formed and the interface better if the substrate used was as good in crystalline quality as possible. The results were comparable when using Corning 7059 glass substrates and when using I.T.O. or SnO_2 coated glass substrates i.e. columnar grain growth and layers free from pinholes were observed in all three cases provided that the CdS thin film thickness was greater than 1.5 μm.

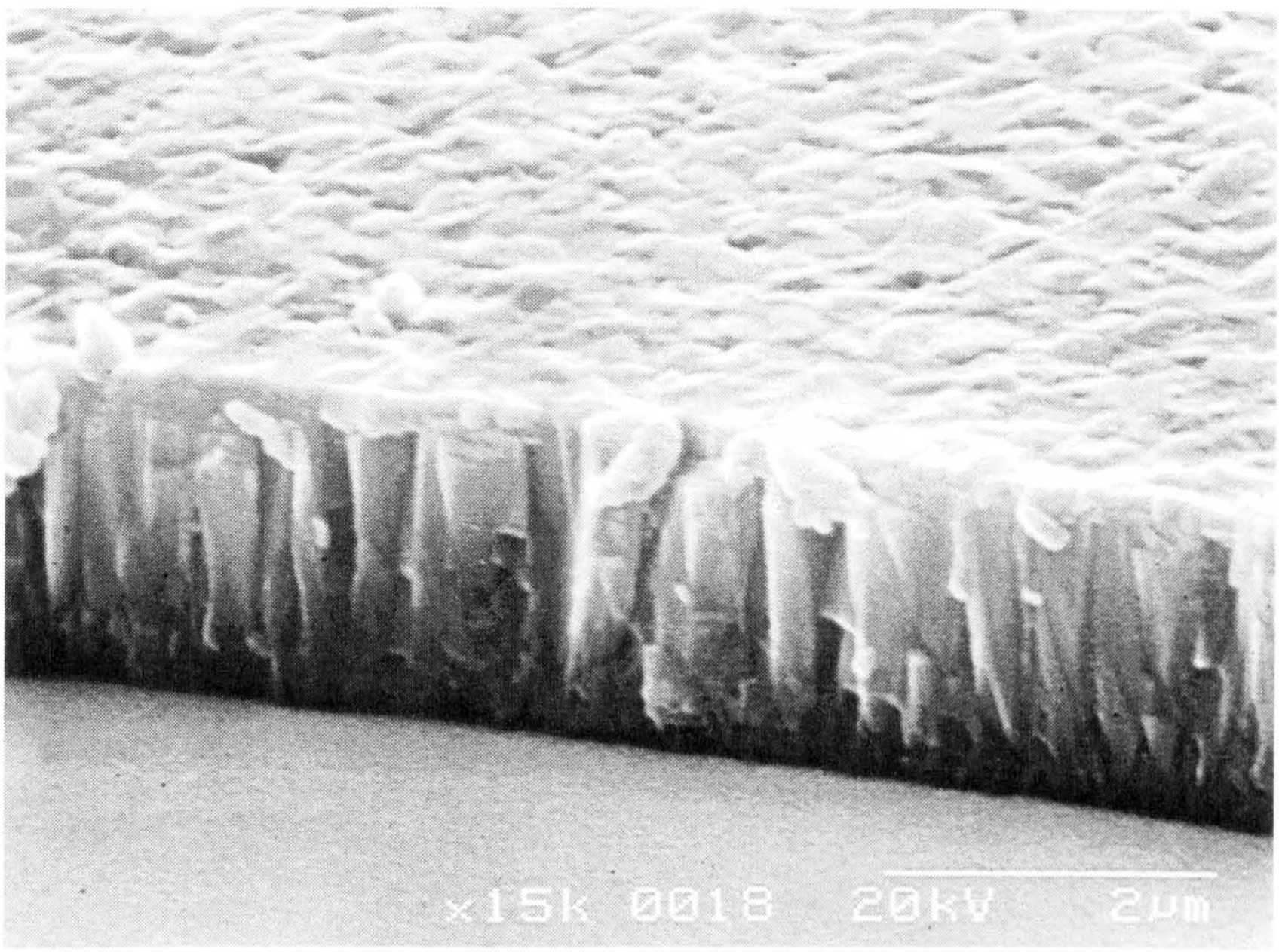


Figure 5.1 Edge View of CdS SEM Micrograph of Cross-section of CdS Film Grown at Substrate Temperature of 200°C

5.2 X-Ray Diffraction Data:

The variation of intensity of X-Rays diffracted versus 2θ for CdS layers deposited using different substrate temperatures, a source temperature of 800°C, a deposition rate 60 A°/Sec and of thickness, 1.8 μm is given in fig.5.2. From the X-ray powder fiche data fig.5.3 it is evident that the CdS films have the wurzite crystal structure, with the c-axis of this structure normal to the substrate. Such observations are consistent with those of [1]. As shown in fig.5.4, the decrease in the (FWHM) of the <002> with an increase of substrate temperature is an indication of improvement of the crystallinity and of the grain size of the CdS thin films with increasing substrate temperature used.

5.3 Optical Properties of the CdS Thin Films Deposited

The optical properties of the CdS thin films were determined using transmittance and reflectance measurements. Data for a typical CdS layer produced using a CdS source temperature of 800°C, a substrate temperature of 200°C and using a deposition rate < 80 A°/ sec is given in fig.5. The film is highly transmissive in the infrared region with a sharp absorption edge at a wavelength of 520 nm below which the film is highly absorbing. A wavelength of 520 nm corresponds to a photon energy, 2.39 eV, which is slightly less than the accepted value for the energy bandgap of CdS (2.42 eV). The interference fringes observed in the T versus \ data were used to determine the thickness of the CdS thin film

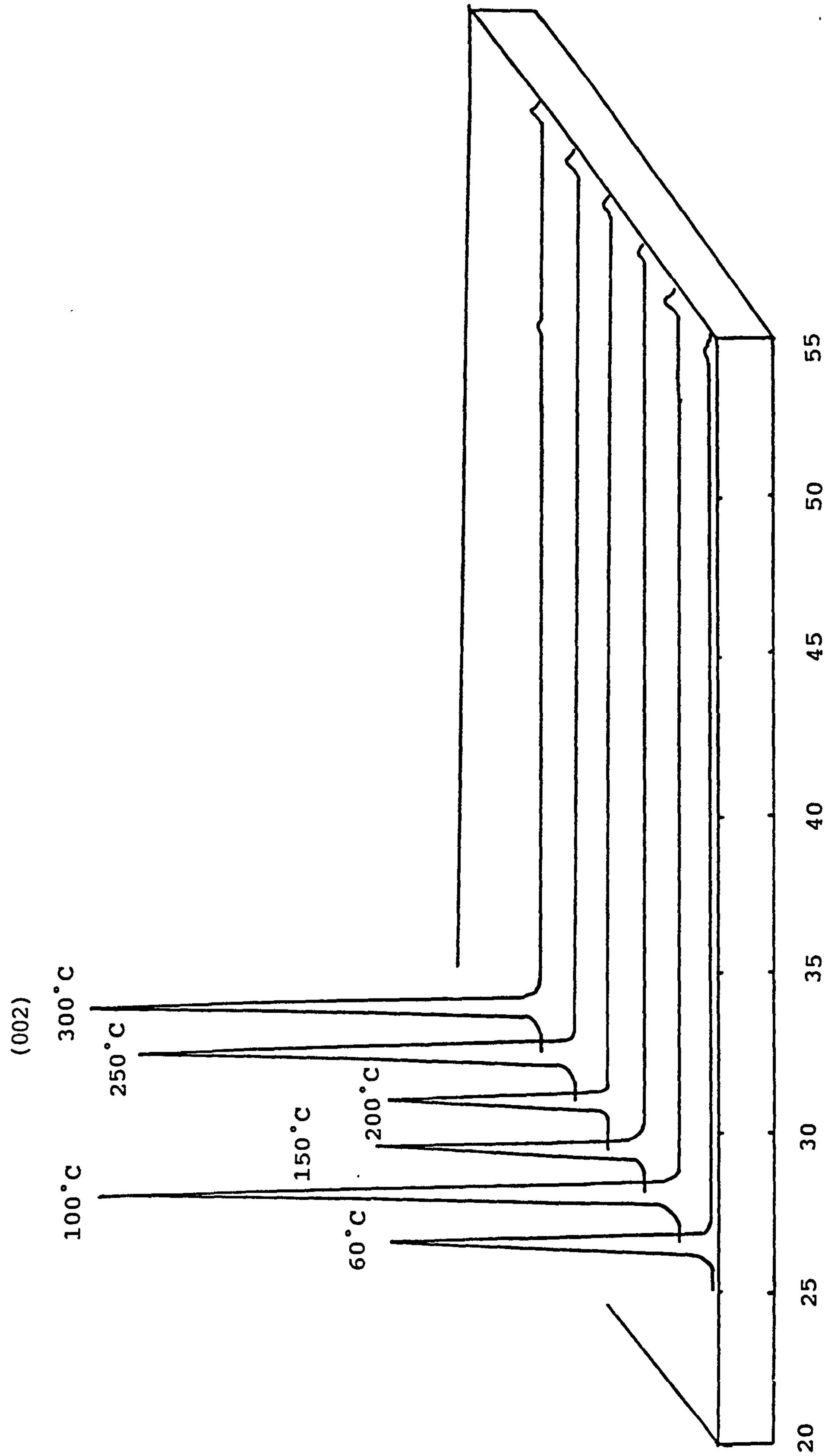


Fig.5.2 X-ray Diffraction Data for CdS Layers Deposited Using Different Substrate Temperature

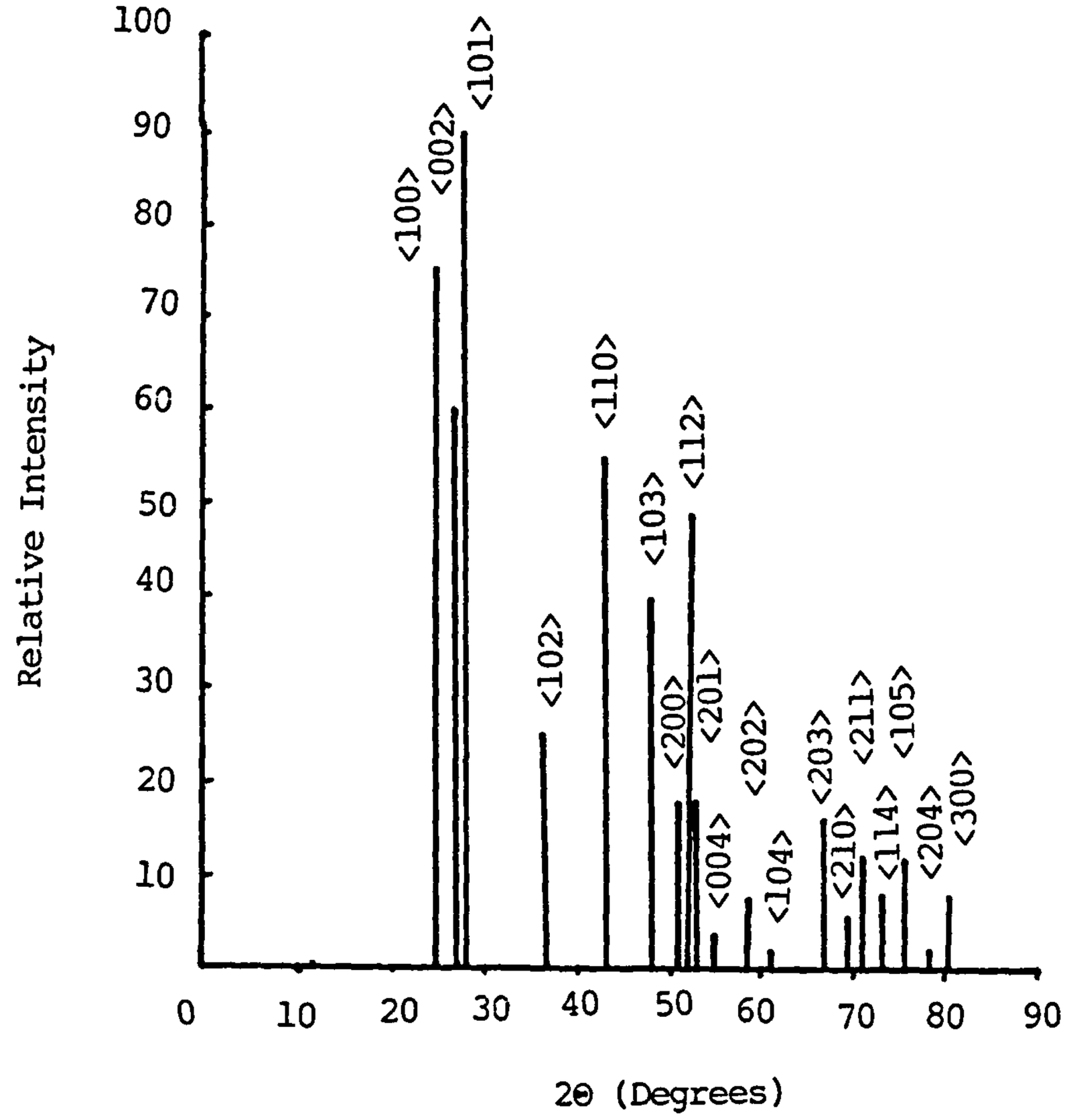


Figure 5.3 X-ray Diffraction Pattern of Hexagonal CdS Crystals.

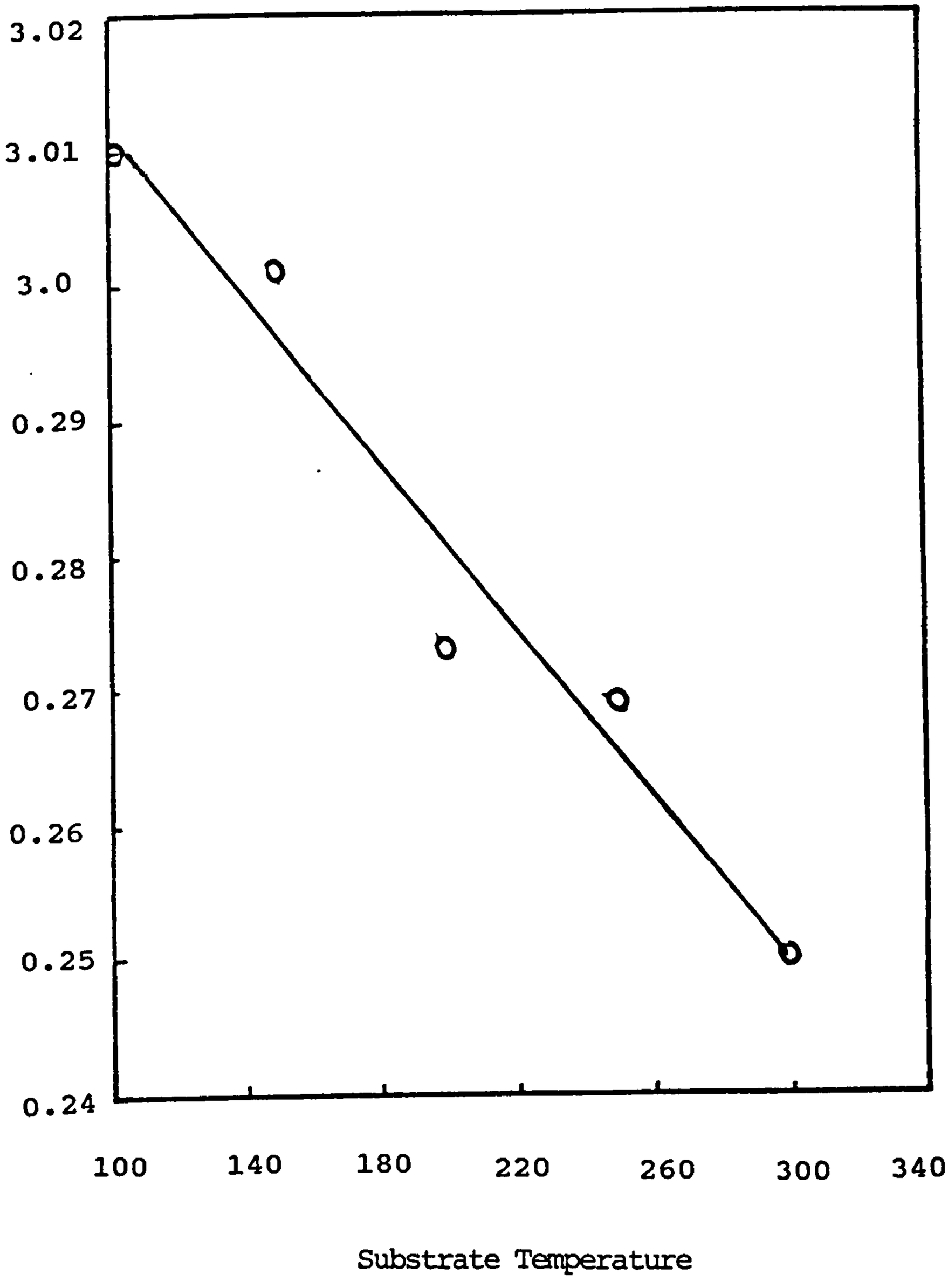


Figure 5.4 Variation of F.W.H.M. of the (002) Peak With Substrate Temperature (°C)

deposited e.g for the sample shown in fig.5.5 the thickness is 1.8 ± 0.1 μm. which corresponds to that measured using the Talystep and that measured by direct observation in the S.E.M. to within ± 4%. The variation of reflectance of a CdS film with wavelength is also given in fig.5.5.The reflectance is low < 2% across the wavelength range (400-2000nm) and the behaviour is similar to that observed by [3]. who attribute such behaviour to scattering from the uneven CdS surface.

The transmittance and reflectance values were used to determine the obsorption coefficient, α , at different wavelengths in the range 400-600nm using the formula given by Ray[4]:

$$T = (1 - R)^2 \exp(-\alpha d) \qquad 5.1$$

where T is the transmittance, R the reflectance and d the film thickness.

For the data given in fig.5.5. the variation of α with λ is given in fig.5.6. The variation is very similar to that observed by other workers e.g. [3,5-7].

For a direct bandgap semiconductor, α , should be given by [8,9] :-

$$\alpha = C/h\nu \, (E_g - h\nu)^{1/2} \qquad 5.2$$

and hence a plot of $(\alpha h\nu)^2$ versus hν should be a straight line with an intercept on the hν axis equal to Eg. Such a plot is given in fig.5.7 for the data given in fig.5.5. The plot is a good straight line with an intercept on the hν axis equal to 2.4 ± 0.2eV which

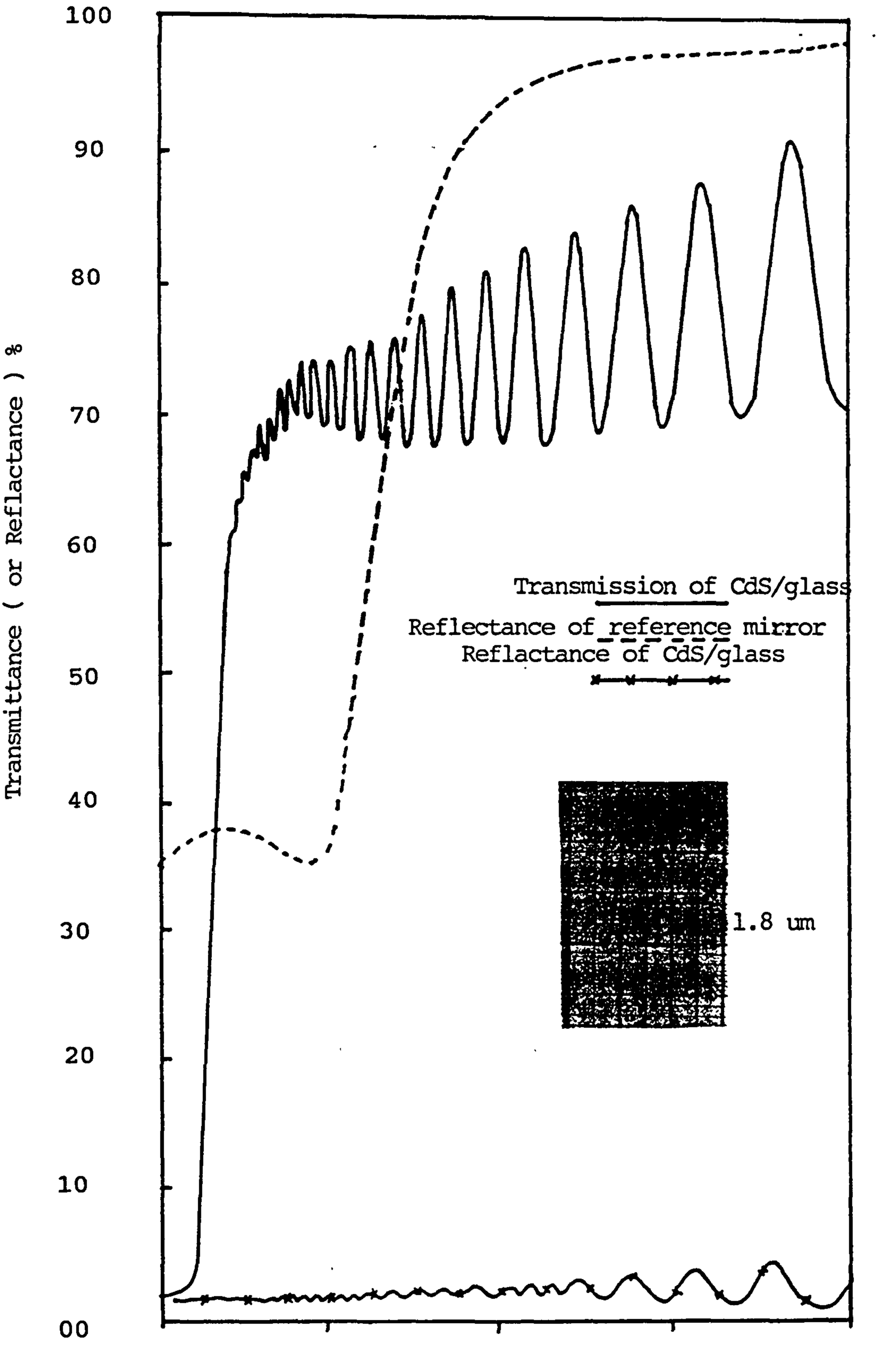


Figure 5.5 Transmittance and Reflectance Versus Wavelength for a CdS Thin Film. Data Obtained Using Tallystep is Also Shown

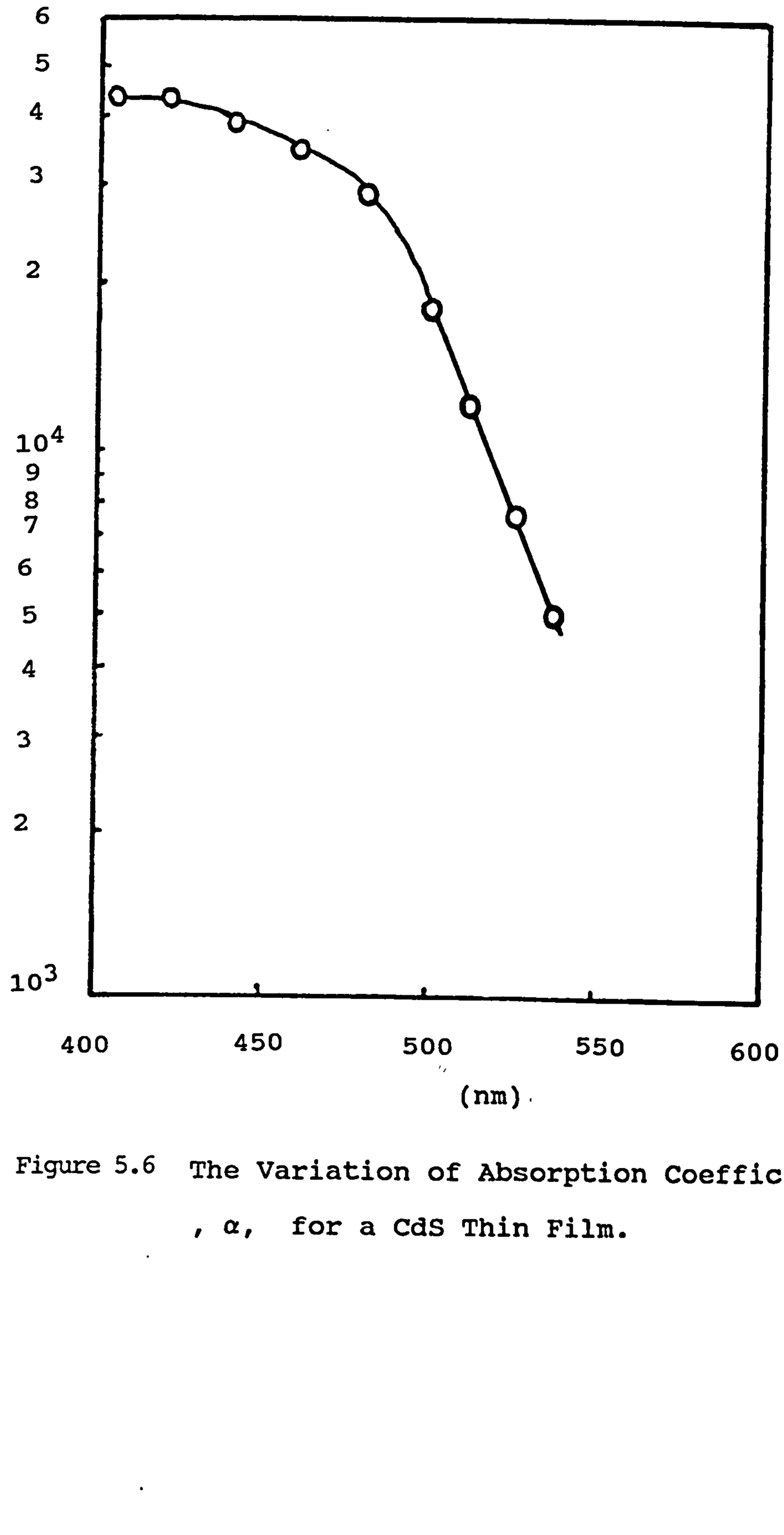


Figure 5.6 The Variation of Absorption Coefficient , α, for a CdS Thin Film.

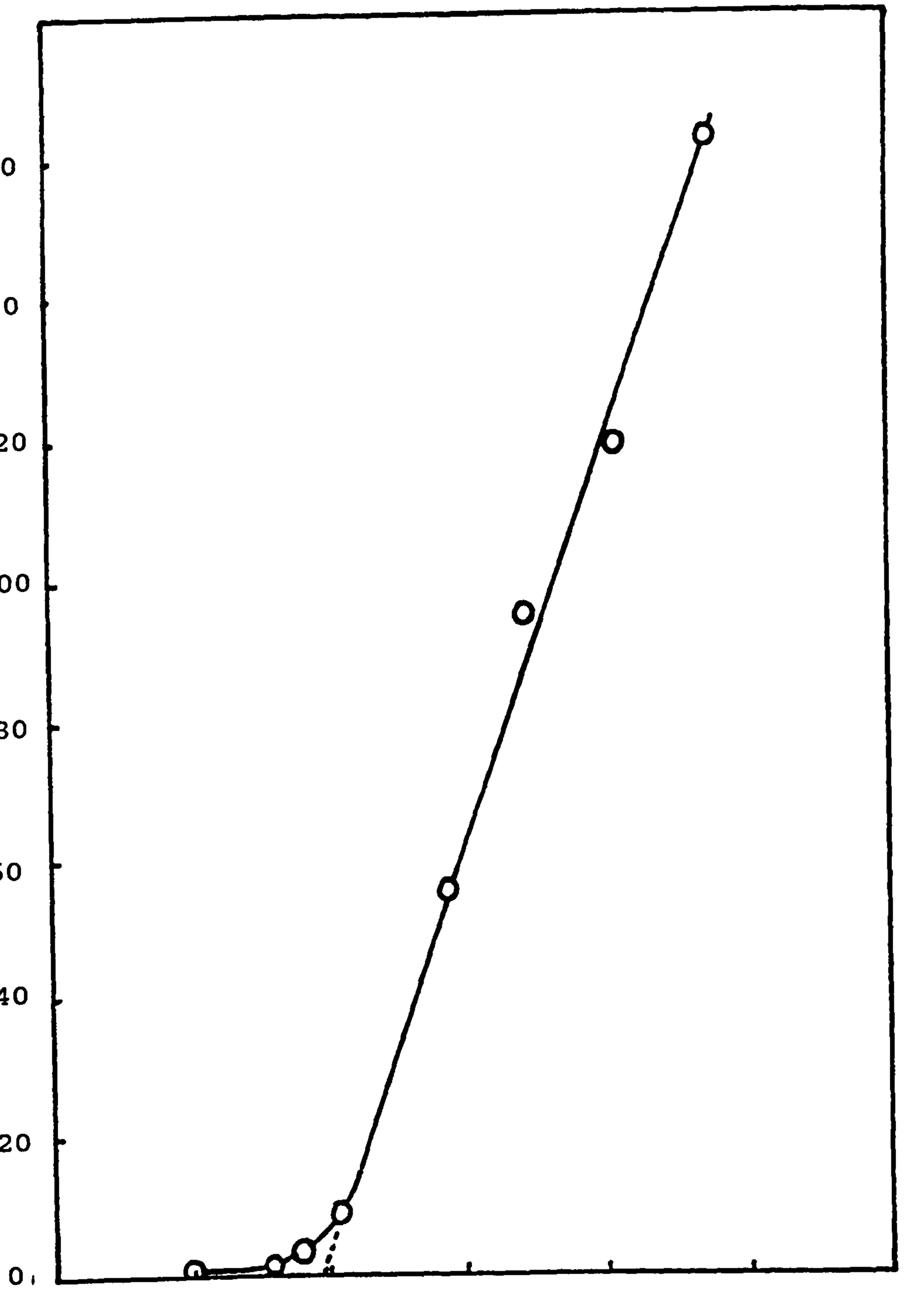


Figure 5.7 Variation of $(\alpha h\nu)^2$ Versus hv for a CdS Thin Film

corresponds well with the accepted value of Eg for the CdS.[1,3,10,11].

The variation of transmittance versus wavelength for layers produced using substrate temperatures < 200 °C are given in fig.5.8. It is apparent that using lower substrate temperatures results in layers with reduced transmittances in the wavelength range 0.6-2.0μm. Using substrate temperature > 200°C did not significantly improve the transmittance of the layers.

5.4 Electrical Properties of the CdS Thin Films Deposited

The resistivity of each deposited CdS film was measured using the four-point probe method and using the Van der Pauw technique, the latter method using indium contacts thermally evaporated onto the CdS layers. The resistivity was measured for the layers deposited using different substrate temperatures and different deposition rates for a constant CdS source temperature (800°C) and for a film thickness ≈ 2 μm .

The variation of the resistivity with substrate temperature for constant deposition rate ≈ 60A°/Sec is given in fig.5.9 and the variation of resistivity with deposition rate for a constant substrate temperature of 200 °C in fig.5.10.

It is evident that the resistivity of the films increases with an increase of substrate temperature and with an increase in deposition rate. Such behaviour is consistent with the observations of [12-17] and is attributed to a deviation from stoichiometry of the deposited CdS layers,

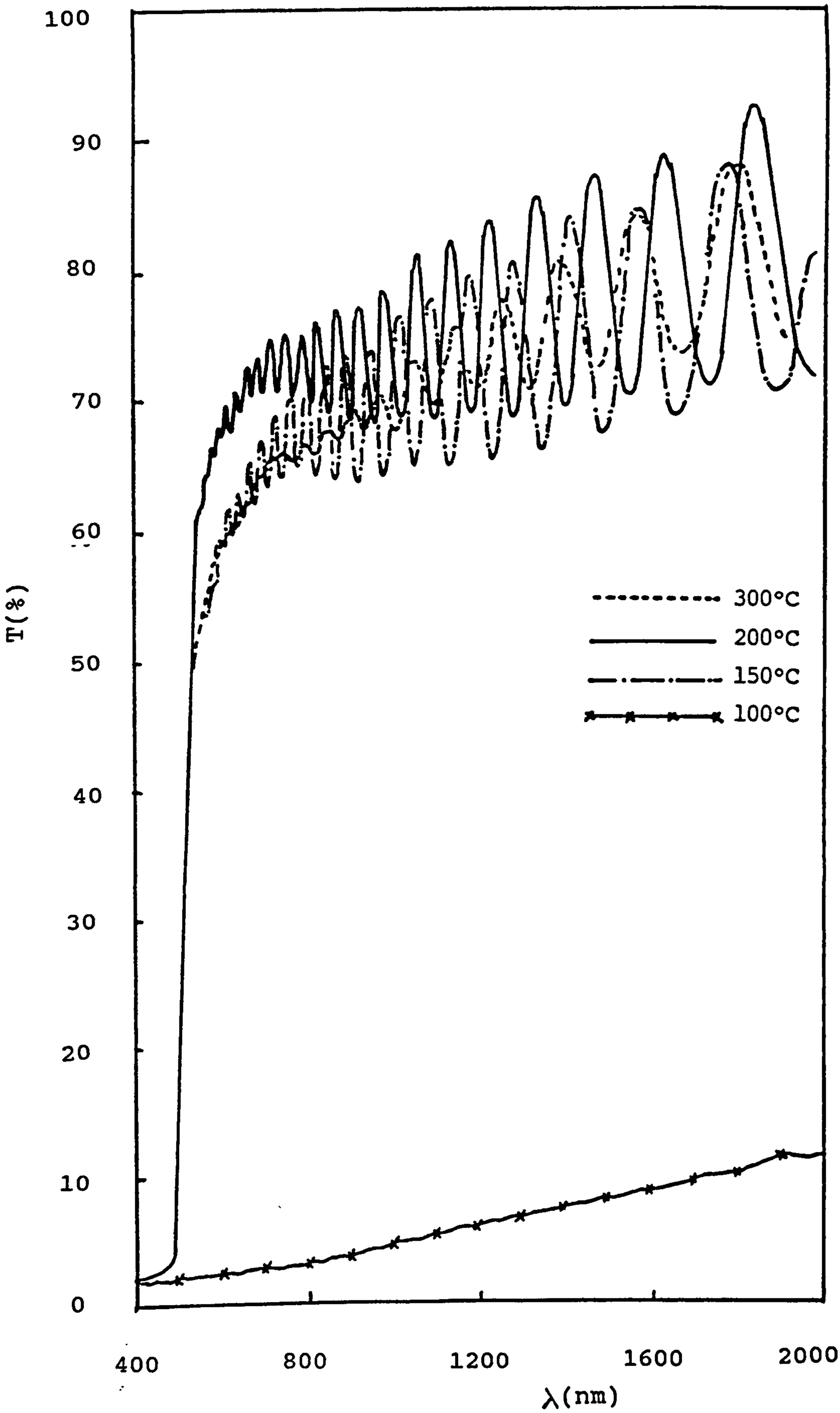


Figure 5.8 Transmittance Versus Wavelength for CdS Thin Films Deposited Using Different Substrate Temperatures

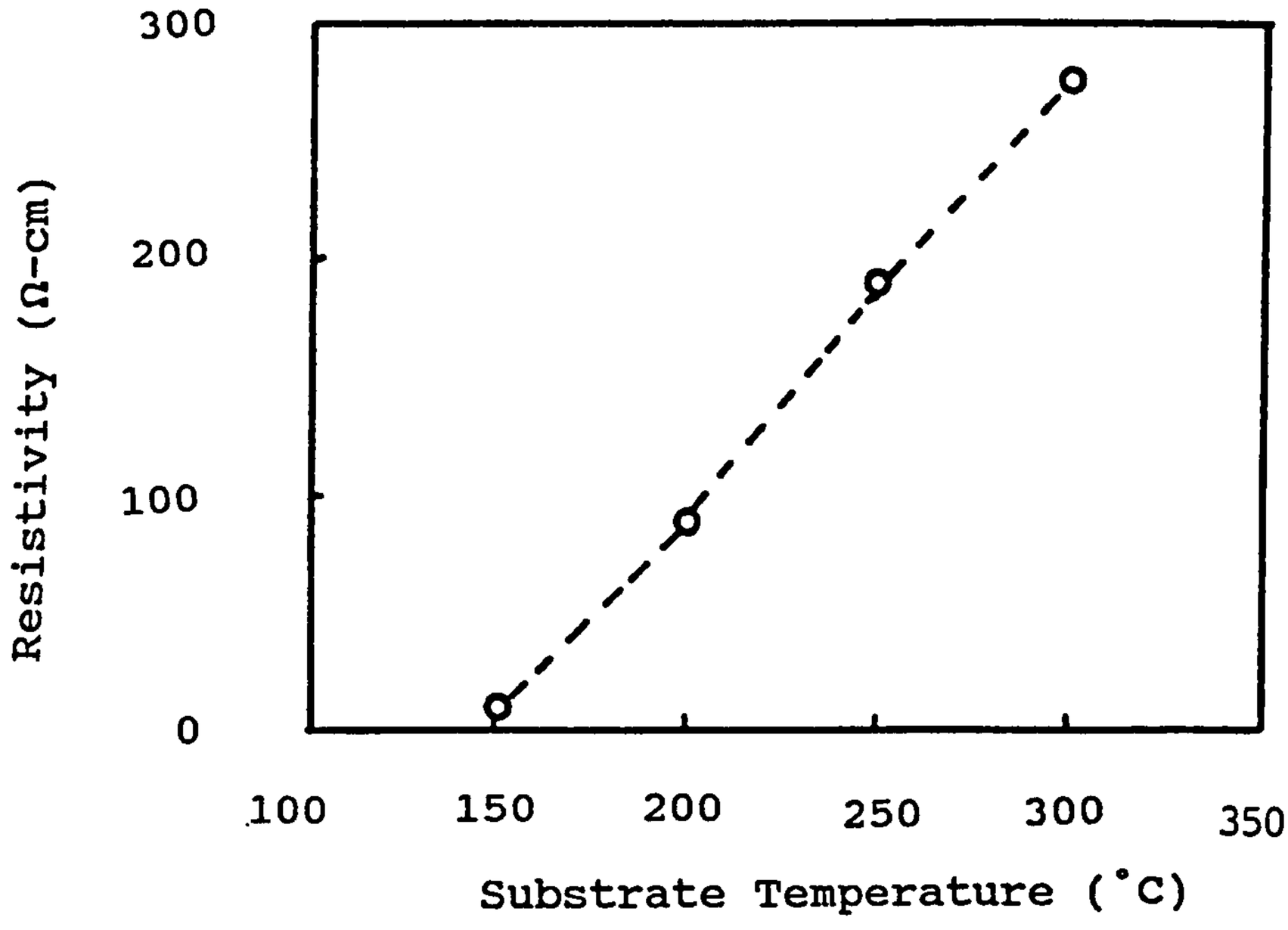


Figure 5.9 Variation of Resistivity of the CdS Films Deposited Versus Substrate Temperature

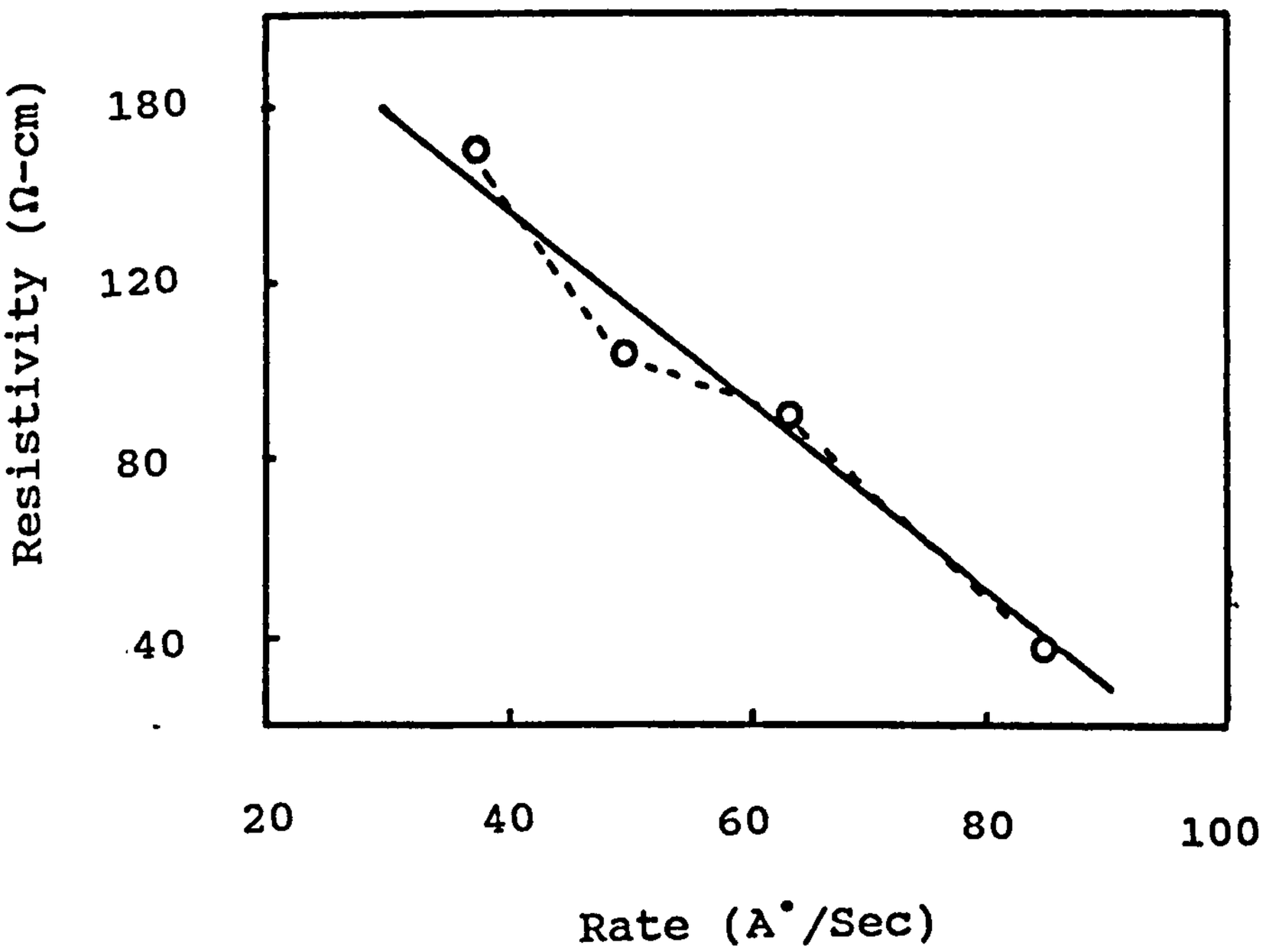


Figure 5.10 Variation of the Rsistivity of the CdS Thin Films Deposited Versus Deposition Rate

in particular, the resistivity of the layers being reduced by the presence of sulphur vacancies in the layers [17,18]. At low substrate temperatures (< 150°C) the reevaporation rate of sulphur is higher than that of cadmium leaving the films cadmium rich with a high concentration of sulphur vacancies where as for higher temperatures (>150°C) the reevaporation rates start to converage and hence the films become more stoichiometric and hence more highly resistive.

For a given substrate temperature, deposition rate and CdS film thickness it was possible to reduce the CdS resistivity further by extrinsically doping the layer using impurities such as indium or gallium [13,16,17,19]. Using a CdS source temperature of 815°C, a substrate temperature, 200 °C, a CdS film thickness of 2μm, a CdS deposition rate of 60A°/Sec and an indium source temperature of 450 °C the CdS resistivity was reduced from 50-100 Ωcm to 10^{-2} Ωcm. It was not however conclusively established whether the reduction of resistivity was entirely the result of uniform extrinsic doping because in polycrystalline layers a high concentration of dopant at the grain boundaries can lead to high conductivity paths through the layers [11]. Such paths can result in low shunt resistances when such the layers are used in devices as well as regions where electron-hole recombination may be enhanced. Such problems have been avoided by some workers by combining the two methods i.e. using undoped CdS to form the junction and then using extrinsically doped CdS to lower

the series resistance and to make easier the formation of an ohmic contact to the material [20].

5.5 Deposition of Te Thin Films:

The thin films of Te were deposited using thermal evaporation using the evaporation system described in section 4.1.

The tellurium was supplied in the form of sticks (150 mm * 25 mm dia) from Johnson Matthey Ltd and it was 99.9995 % pure. It was first ground to a fine powder, 6.0 grams of it placed into the quartz bottle, quartz wool placed on top of it (to avoid spattering) and the crucible inserted into the source heater assembly. The vacuum chamber was evacuated to a pressure of 10^{-6} - 10^{-7} Torr. The substrate was heated at a rate of 4°C/min to the required temperature (in the range 60 to 200°C) and left at this temperature for 30 minutes to achieve steady and uniform heating of the substrate.

Initially the source material was heated at the rate of 5°C/min and then sintered at 100°C for 20 minutes to allow thorough outgassing of the evaporant material. The source temperature was then increased at the rate of 10°C/Sec to the evaporation temperature (typically 270 °C). A typical Te source temperature/time heating profile is shown in fig.5.11.

The deposition rate monitored by the quartz crystal monitor was 15-16 Hz (corresponding to 8-10 A°/Sec) for a Te source temperature of 270°C but it was found that the deposition rate varied approximately 20% during

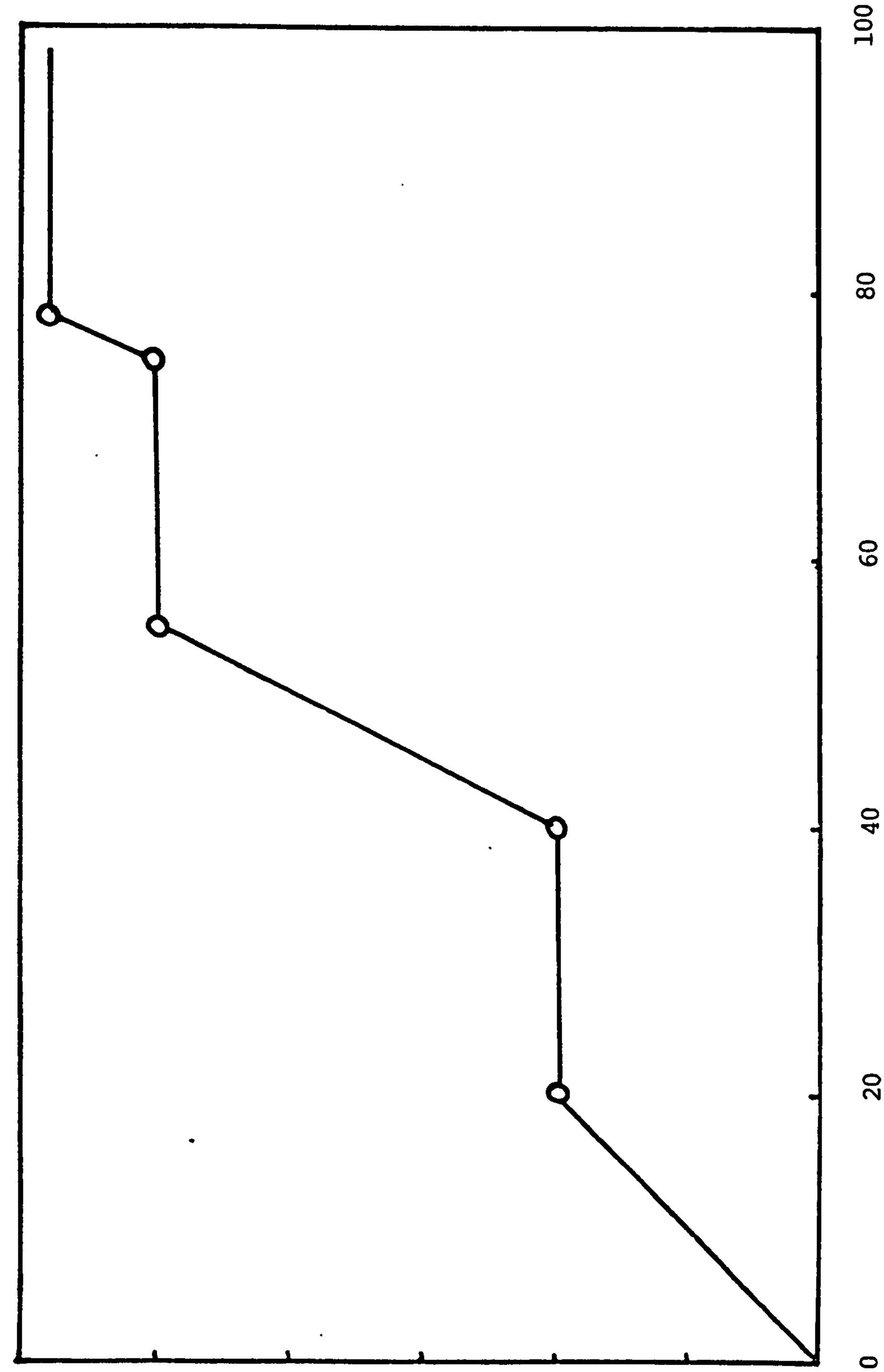


Figure 5.11 The Temperature Versus Time Profile Used for Heating the Tellurium Source Material.

the deposition. It was therefore decided to heat the evaporation source using the manual mode on the temperature controller during the deposition to keep the deposition rate constant.

It was observed that the films deposited at higher substrate temperatures had non-uniform surfaces with pinholes present. Silvery, white, shiny, adherent, uniform films of Te free from pinholes were obtained using unheated substrates (at a temperature of 16°C) for Te source temperatures in the range 220-260 °C.

The quartz crystal monitor in the system was used as a guide to the thickness of Te deposited. A calibration graph showing the actual film thickness measured using the Talystep versus the frequency of oscillation of the quartz crystal in quartz crystal monitor, for a Te source temperature of 270 °C is shown in fig.5.12. The linear behaviour for film thicknesses > 1000 A° indicates that the sticking coefficient during the deposition of the film remains constant for Te thicknesses up to 1 μm.

5.6 Deposition of Cd Thin Films :

The cadmium used was in the form of shot, 1-3 μm in diameter and supplied by Johnson Matthey limited and it was 99.9999% pure. Typically 6 mg. of cadmium was placed into the source heater assembly. The deposition chamber was then evacuated to a pressure 10^{-6} - 10^{-7} Torr. A typical source temperature time heating profile for the cadmium source in shown in fig.5.13. Initially the temperature of the source material was increased using a

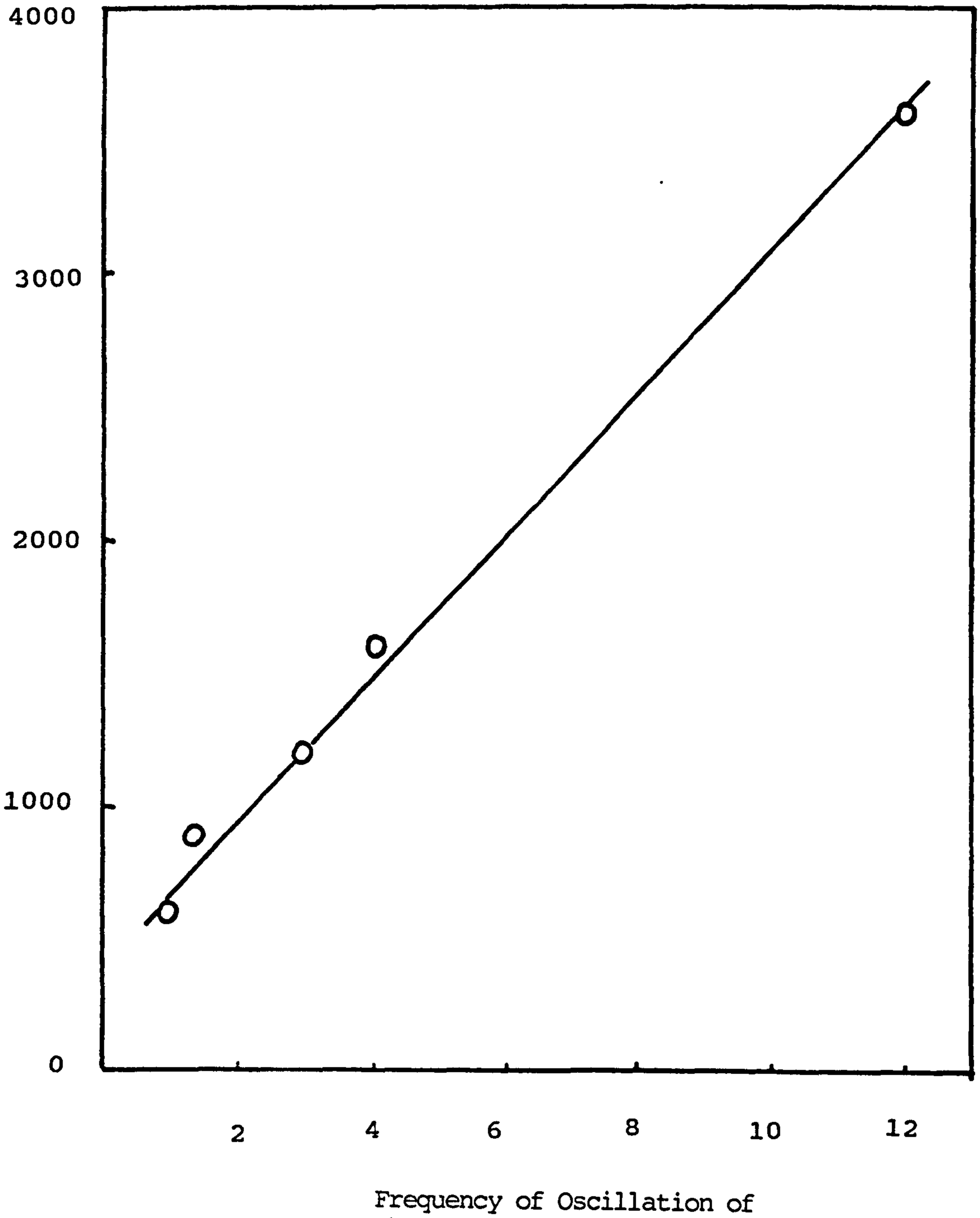


Figure 5.12 The Variation of Measured Tellurium Thickness Versus Frequency of Oscillation of the Quartz Crystal (T_{sub} = 16°C and T_{Te} = 270°C)

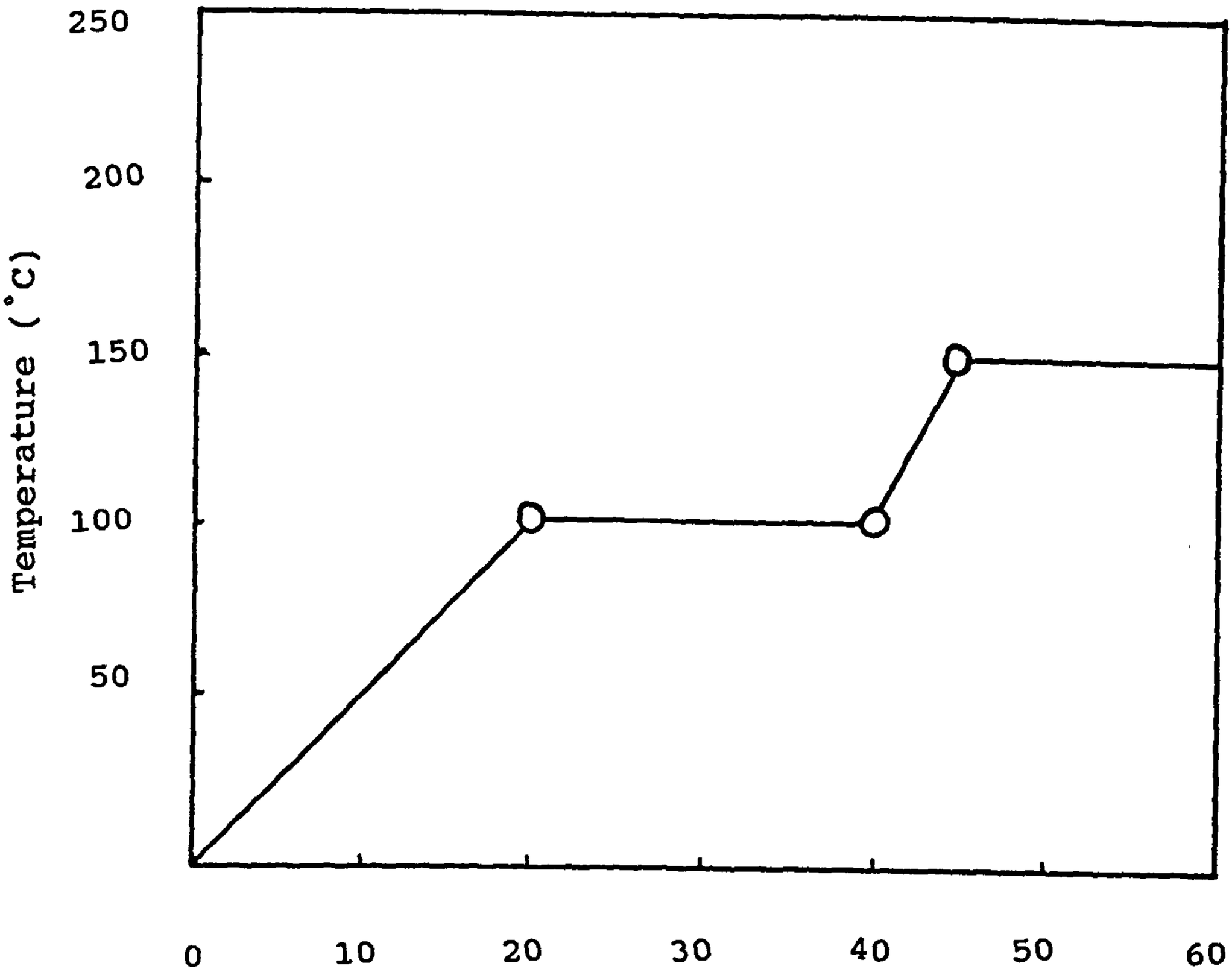


Figure 5.13 Typical Temperature-Time Heating Profile Used With CdS Source

rate of 5°C/min, it was then held constant at 100°C for 20 mins and then increased again using a rate of 10°C/min until the evaporation temperature (typically 150°C) was reached . The cadmium layers deposited on glass substrates were found to be very non-uniform for all the conditions used i.e. for source temperature in the range 150-170°C and substrate temperatures in the range (15-200°C). It was therefore decided to deposit Cd films onto tellurium layers that had already been deposited onto glass substrates. The deposition of Cd onto such tellurium layers resulted in uniform films free from pinholes for a Cd source temperatures in the range 120-150°C. A standard source temperature of 135°C was adopted so that the quartz crystal monitor in the system could be calibrated to permit the controlled deposition of cadmium with the rate of 10 A°/ Sec.

The variation of cadmium film thickness deposited as measured using the Talystep versus the frequency of oscillation of the quartz crystal monitor is shown in fig.5.14. The linear behaviour for Cd thicknesses in the range 1000-10,000 A° indicates that the sticking coefficient of Cd on Te was constant. The frequency of oscillation of the quartz crystal during the deposition was hence used to determine the film thickness deposited.

5.7 The Formation of CdTe by Annealing Cd/Te Stacks in N2:

The ratio of thicknesses of Te and Cd needed to produce CdTe was calculated assuming that elements deposited in

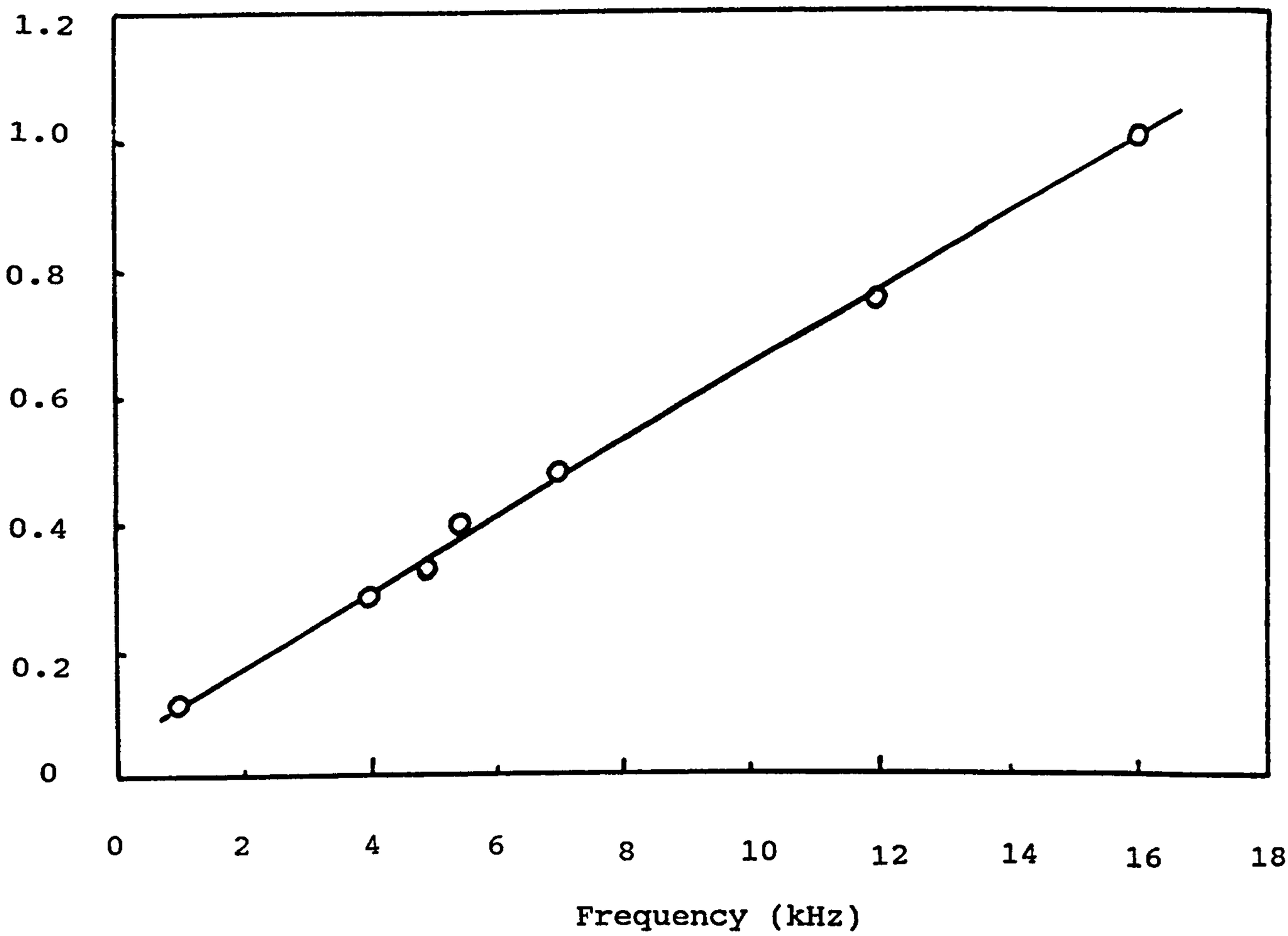


Figure 5.14 The Variation of Measured Cadmium Thickness Versus Frequency of Oscillation of the Quartz Crystal. (T_{sub}=16°C and T_{Cd}=135°C)

uniform homogeneous thin films throughout the evaporation. This calculation is given in appendix(A). The relative thicknesses of the Cd and Te films should be 5:6 to produce stoichiometric CdTe. The layers were deposited with thicknesses in this ratio using unheated substrates, a Te source temperature 273°C and a Cd source temperature, 160°C, such that the deposition rates for both the Cd and Te was < 10 A°/ Sec. The vacuum pressure was typically 10^{-5} - 10^{-6}Torr during the evaporations. For most of the work Corning 7059 glass substrates were used and hence a Te layer was deposited first.

Following the deposition of the stacked layers the samples were removed from the deposition chamber and placed in the annealing chamber described in section 4.2. The samples were then annealed in an inert environment - nitrogen or vacuum by heating the samples at 50 °C intervals in the range 50 to 550 °C for 15 minutes at each temperature. The variation of transmittance versus wavelength was measured after each anneal using the Cary 17-D spectrophotometer (described in section 4.4). Initial attempts to synthesize the CdTe used Cd thicknesses ≈ 2000 A° and Te thicknesses ≈ 1800 A°.

These layers cracked and peeled off the substrate for annealing temperatures in the range 200°C - 250°C. It was speculated that at such a temperature it was possible that reevaporation of the Cd and / or Te from the layers could be weakening the adherence of the stacks from the glass slide or that the heat released from the exothermic reaction between the Cd and Te could be causing a

difference in expansion between the CdTe formed and the neighbouring Cd and Te layers or between the bottom Te layer and the glass slide.

It was hence decided to deposit thinner layers of Cd and Te (< 1400A° thick) and to maintain the CdTe thickness by using a larger number of layers.

This approach was found to be successful and it was now possible to heat the stacks upto 550°C without encountering this adherence problem.

A typical result for a six layer stack consisting of three layers of Te, each 700 A° thick and, three layers of Cd each 600 A° thick, and annealed in nitrogen at 50 °C intervals for temperatures up to 550 °C is given in fig.5.15. Before annealing the sample was almost opaque with transmittance < 5 % for wavelengths 800 - 2000 nm. After annealing the transmittances progressively increased for λ > 825 nm and a steep absorption edge observed at a wavelength of 815 nm i.e. at a wavelength corresponding to the energy bandgap of CdTe. The transmittance of the sample could be increased to > 80% for photon energies less than the energy bandgap. It is evident from fig.5.14 that an annealing temperature > 450°C was necessary to fully synthesize the CdTe.

Reflectance versus wavelength measurements for the sample are given in fig.5.16. These measurements were used in conjuction with the transmittance measurements to calculate the absorption coefficient, α , for different wavelengths using the formula [4] :-

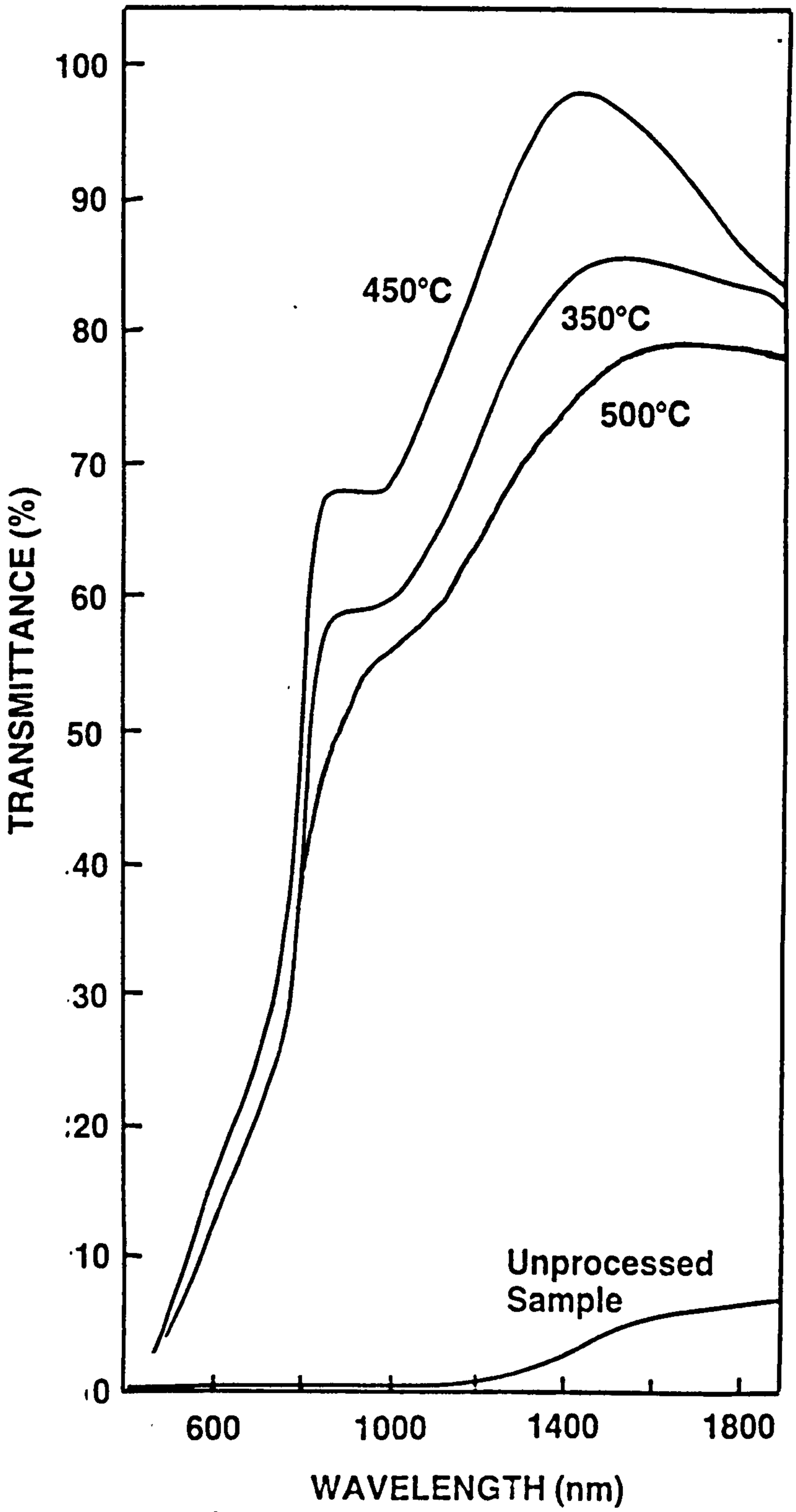


Figure 5.15 Transmittance Versus Wavelength for an Unannealed Stack and for the Stack Annealed in Nitrogen at 350°C, 450°C and 500°C.

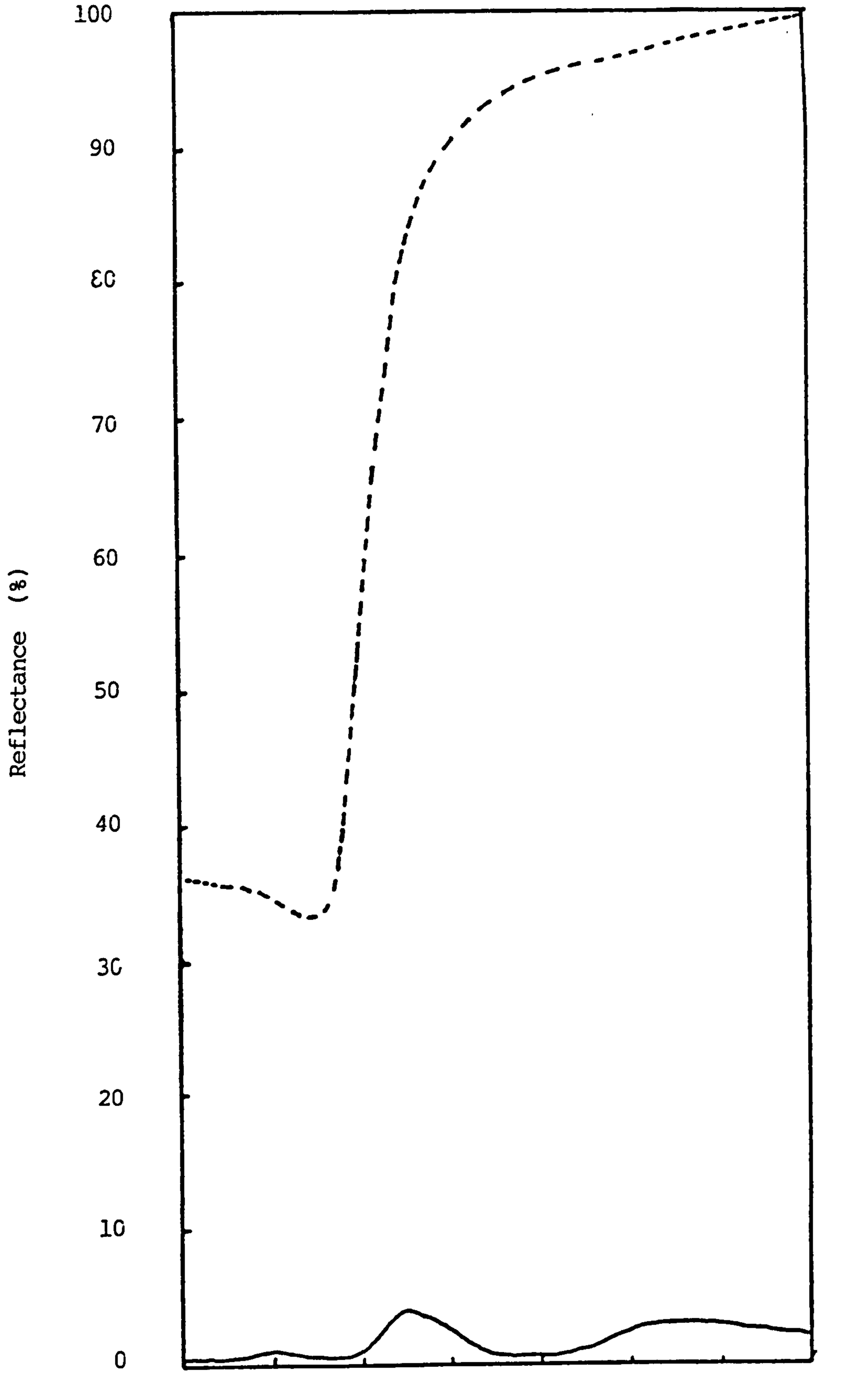


Figure 5.16 The Variation of the Reflectance of a CdTe Thin Film Versus Wavelength

$$\alpha = (-1/d)\ \ln\ \{(T/(1-R)^2\} \qquad 5.3$$

where d is the film thickness.

A plot α versus λ is given in fig.5.17. The variation is very similar to that observed for the electrodeposited CdTe layers produced by Basol [21], which were used to produce 10 % efficient CdS/CdTe solar cells.

For a direct bandgap semiconductor such CdTe, α is related to hv by the relation [3,8]:-

$$\alpha = (C/hv)\{E_g - hv\}^{1/2} \qquad 5.4$$

and hence a plot of $(\alpha hv)^2$ versus hv should be straight line with an intercept on the hv axis equal to E_g. Such a plot is given in fig.5.18 for the samples used to present the previous data. The plot is indeed a straight line and an extrapolation to the hv axis yields a value of E_g = 1.56 eV which is consistent that expected for a successfully synthesized CdTe thin film [22,23].

It was consistently found that if the annealing temperature for synthesizing the CdTe was increased to > 450°C the transmittance and absorption coefficient versus wavelength curves were found to " degrade " i.e. the absorption edge became less steep and the transmittance for the photons with energies < E_g was reduced as shown in fig.5.15. An annealing temperature of 450°C was thus considered to be optimum for synthesising the CdTe.

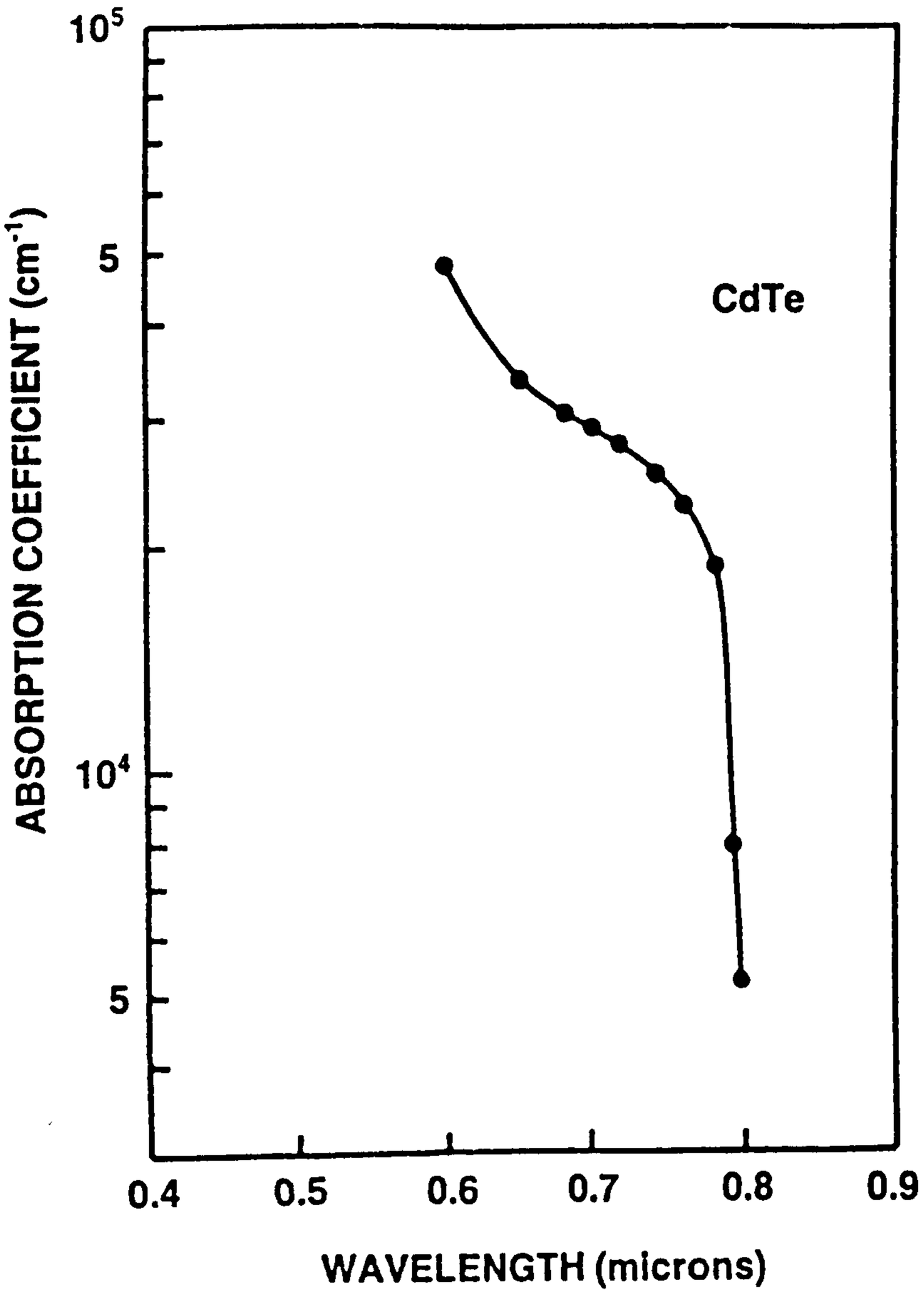


Figure 5.17 α Versus hv for a Cd/Te Sample Produced by Annealing a Cd/Te Stack at 450°C in Nitrogen.

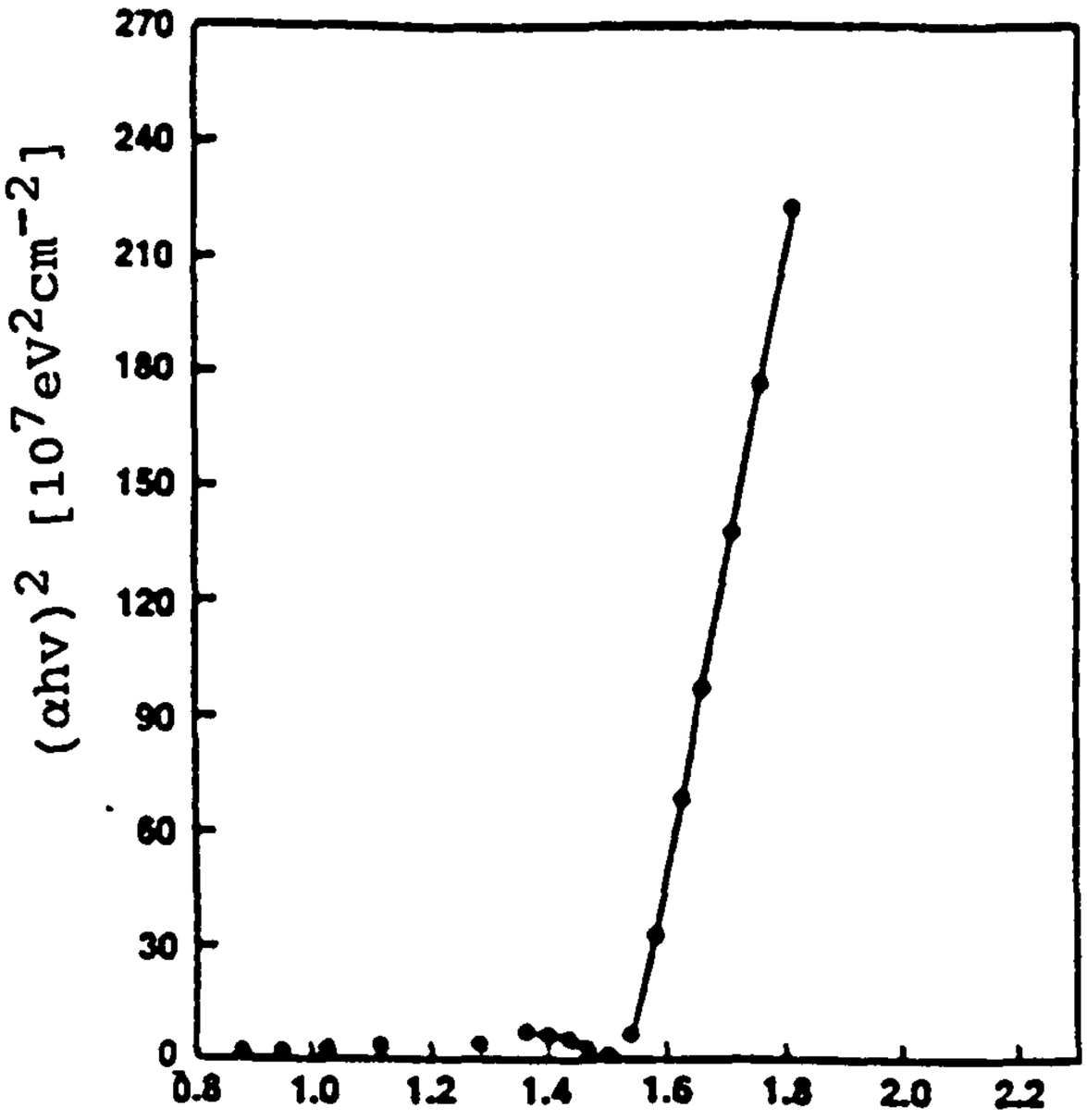


Figure 5.18 $(\alpha hv)^2$ Versus hv for a Cd/Te Sample Produced by Annealing a CdTe Stack at 450°C in Nitrogen

A secondary electron micrograph of one of the layers produced is given in fig.5.19. As shown in the figure the layers were found to consist of small randomly oriented grains which were tightly packed together ; the grains were typically ≈ 0.1 μm in diameter.

Increasing the thickness of the CdTe to > 1μm by increasing the number of stacks did not result in an increase in grain size ; the layers were again found to consist of small, randomly orientated grains similar to those observed in fig.5.20.

X-ray diffraction data obtained using the apparatus described in section 4.8 is given in fig.5.21 for a sample of CdTe, 0.56 μm thick, obtained by annealing a six layer stack in nitrogen at 450 $^{\circ}$C for 15 minutes. A comparison of the Bragg peaks obtained with those expected for CdTe shown in fig.5.22(a) indicates that CdTe had indeed been formed. The samples had the sphalerite (cubic) crystal structure and were preferentially orientated in the [111] direction. The small diffraction peak, at $2\theta = 43.3^{\circ}$, was not however expected for CdTe and it could be interpreted as due to the presence of excess tellurium in the layers, because at $2\theta = 43.3^{\circ}$ such a reflection is expected from the (111) planes within hexagonal tellurium (see fig.5.22(b)).

Excess tellurium as a second phase has been observed by many workers, including refs. [24,25]. Birkmire et al [25] have reported that the excess tellurium found present in the CdTe samples they produced using thermal

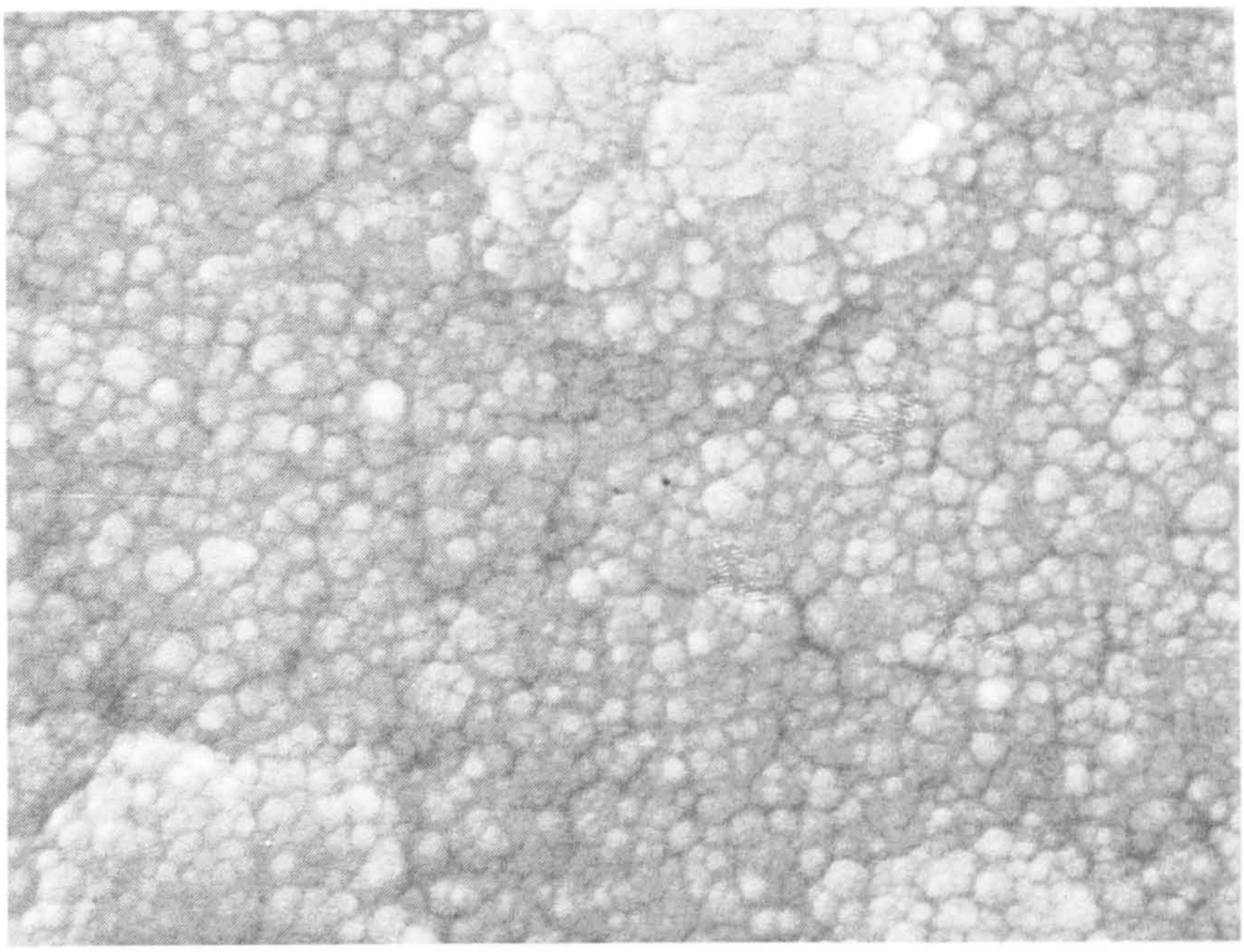


Figure 5.19 Secondary electron micrograph of a CdTe layer produced by annealing a Cd/Te stack at 450°C in nitrogen

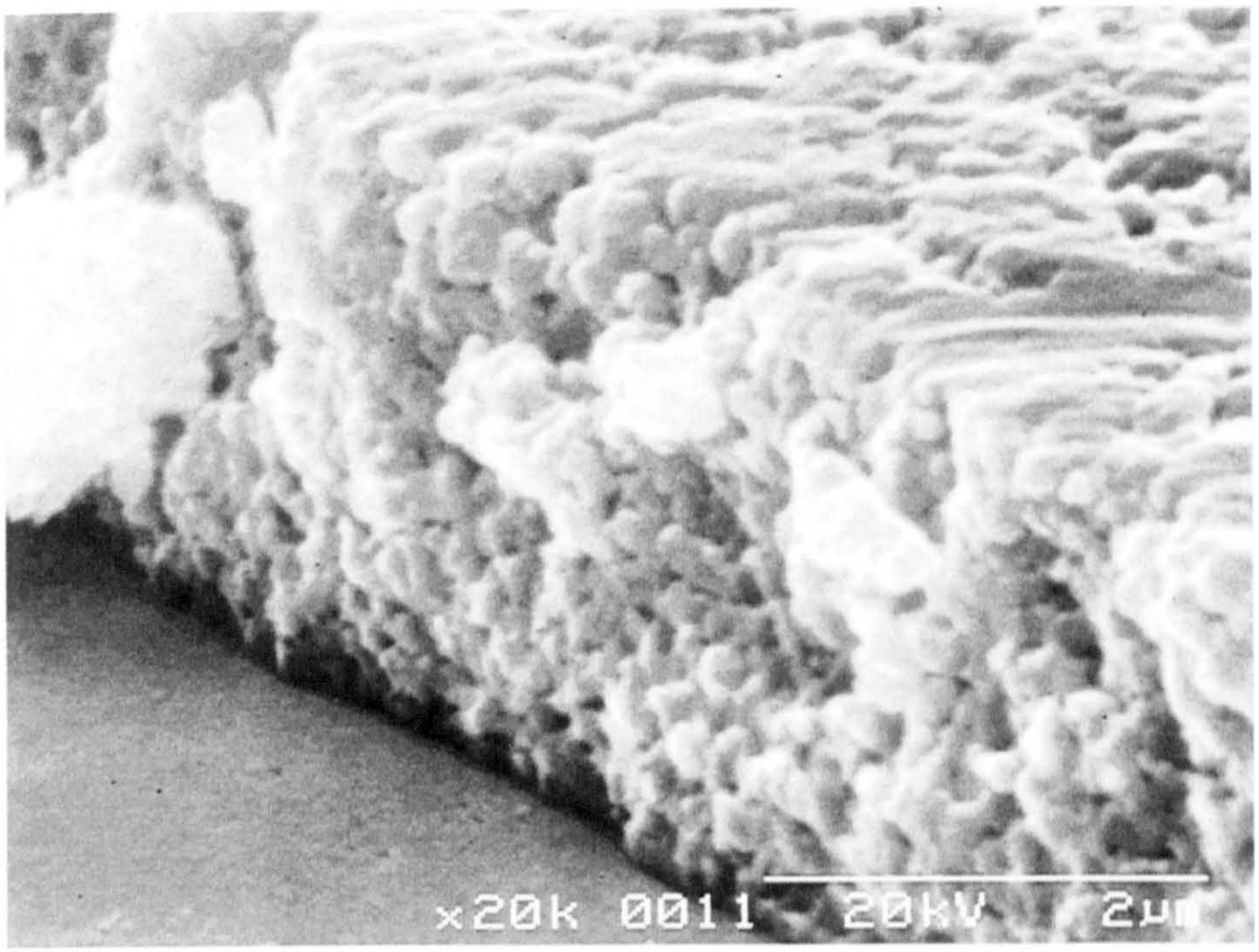


Figure 5.20 Secondary electron micrograph of (Thickness> 1 micron) CdTe layer produced by annealing a Cd/Te stack at 450°C in nitrogen

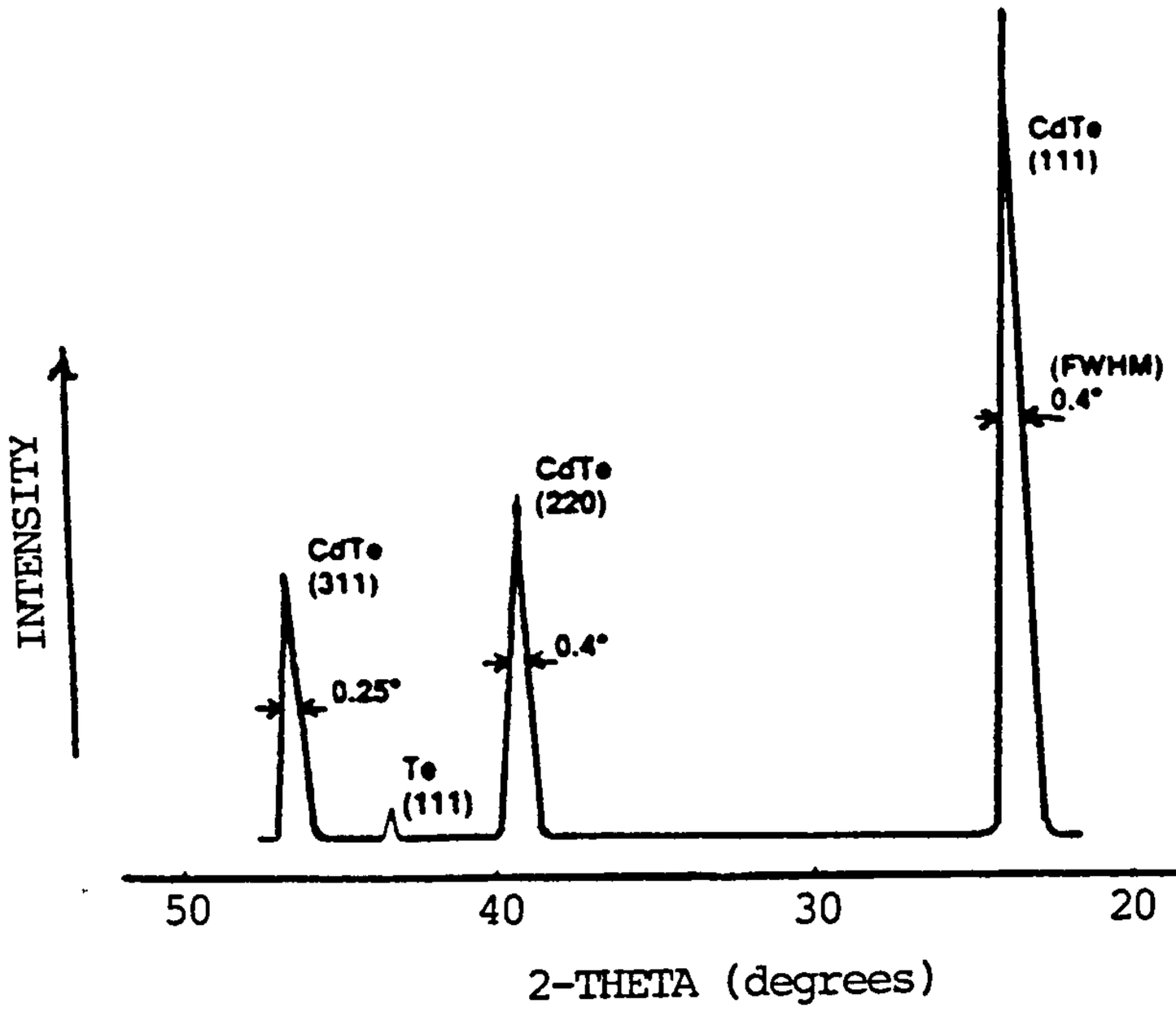


Figure 5.21 X-ray Diffraction Data for CdTe Produced by Annealing a Cd/Te Stack at 450°C in Nitrogen.

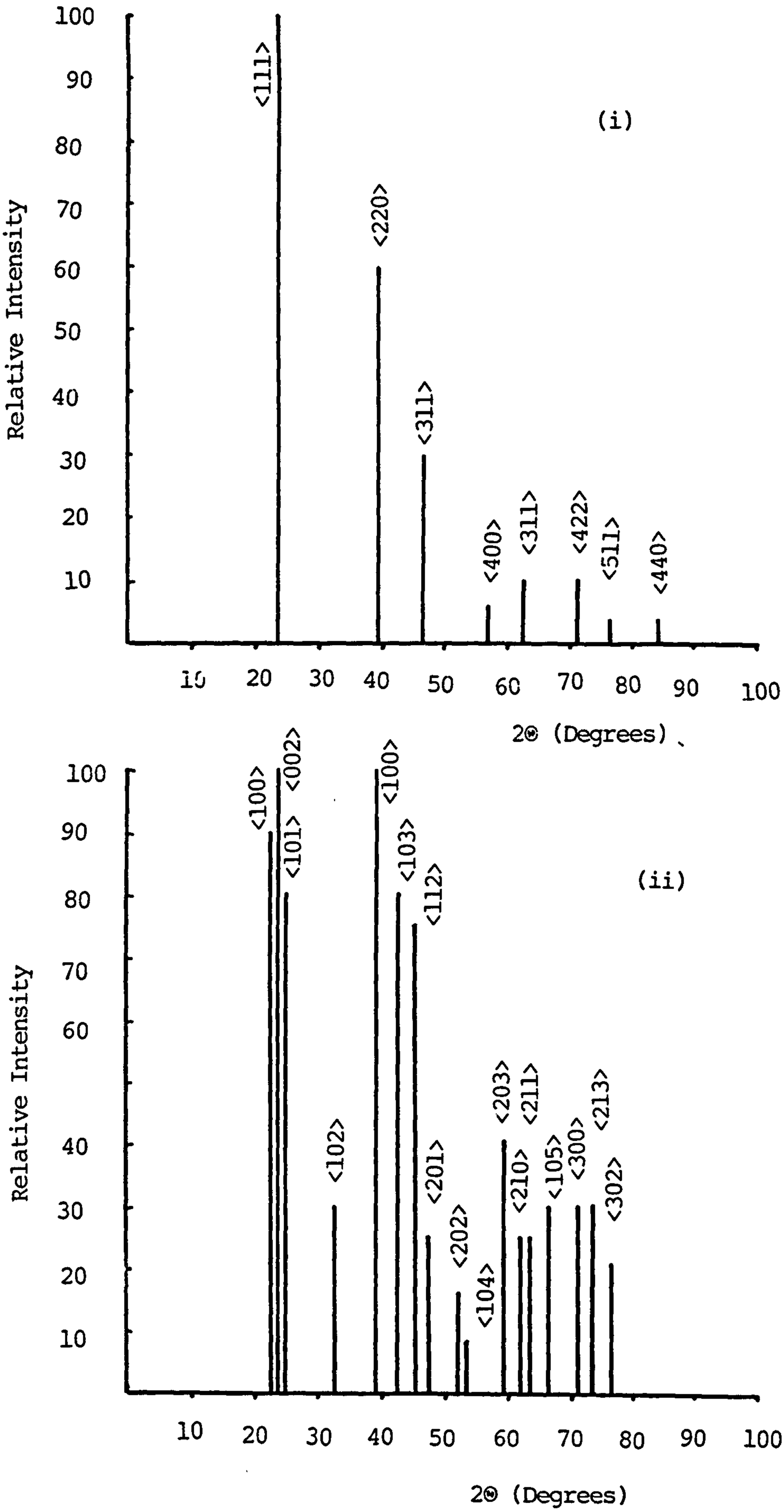


Figure 5.22(a) X-ray Diffraction Pattern of (i) Cubic CdTe
(ii) Hexagonal CdTe.

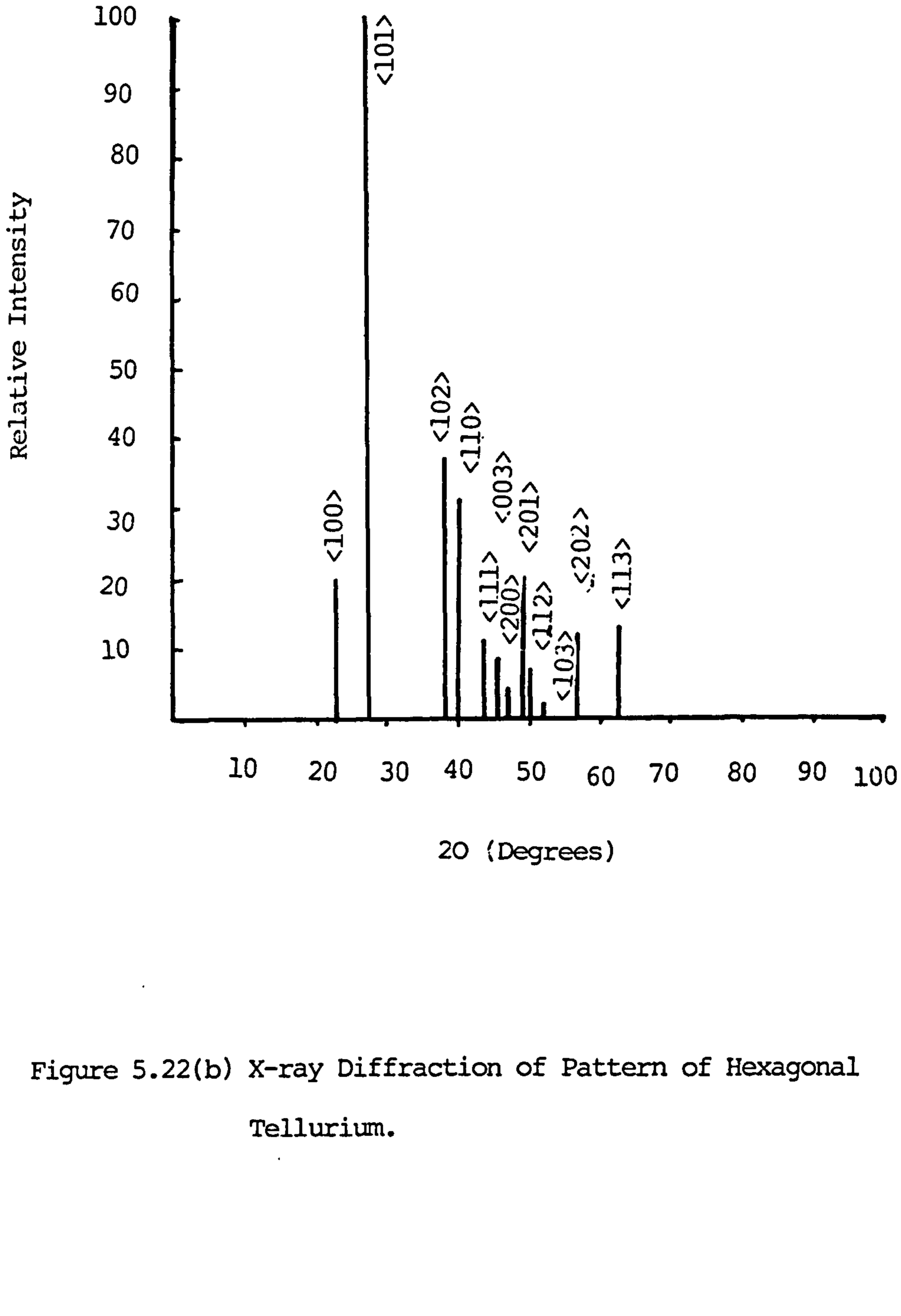


Figure 5.22(b) X-ray Diffraction of Pattern of Hexagonal Tellurium.

evaporation could be eliminated by coevaporating Cd with the CdTe during film growth. It was therefore decided that such an extra phase observed in S.E.L processed CdTe could be eliminated by adjusting the relative thicknesses of the Cd and Te layers in the stack more precisely towards as excess of cadmium. This approach proved to be successful; the peak at $2\theta = 43.4^{\circ}$ was eliminated when the layers contained excess cadmium. For such layers the ' full width half maximum ' (FWHM) of the (111) CdTe peak was found to be 0.42°. Using the expression given by [26]:-

$$L = C\backslash/B \ Cos\theta \qquad 5.5$$

where L = crystallite dimension perpendicular to the diffracting plane,

λ = X-ray wavelength.

θ = Diffraction angle.

B = Broadening on 2θ scale expressed in radians, due to crystallite size,

and C = A constant which depends on broadening measurement.

The F.W.H.M. corresponds to a crystal size $\approx 215A^{\circ}$ which is smaller than the grain size observed in the S.E.M.

All the layers synthesized in nitrogen had high resistivities $> 10^6$ Ωcm and were found to be slightly n-type as determined using the hot probe method [8,27,28] which is based on the fact that thermoelectric power is negative for p-type semiconductors and positive for n-type semiconductors.

5.8 Formation of CdTe by Annealing the Cd/Te Stacks in Vacuum and Air:

It was decided to synthesize CdTe by annealing the Cd/Te stacks in vacuum and air to compare the results with those obtained when layers were synthesized in nitrogen. The anneal in air was thought to have the most potential because various workers have reported that oxygen plays a significant role in improving the properties of CdTe for producing high efficiency solar cells [21,29-31].

The highest efficiency CdTe solar cells produced to date were made using the closed spaced sublimation (C.S.S.) method [32] and during the process a controlled amount of oxygen present during the sublimation of the CdTe has been found to be essential to produce such high efficiency cells. The " Monosolar process " developed by Basol [32,33] and currently used by B.P. Solar International [34,35] also involves an anneal with oxygen present. The electrodeposited films are found to be n-type with high resistivities and an anneal in air is found to convert the layers to p-type and to lower the resistivity. Basol [21] refers to this process as the TCJF i.e. the "type converted junction formation process.

The CdTe was produced using 11 layer stacks and the stacks annealed at 450°C for 15 minutes in nitrogen, vacuum and air environments to synthesize the material.

S.E.M. micrographs of the layers produced are given in fig.5.23(a) and (b). It is apparent that the surface morphology and grain size for the layers produced by

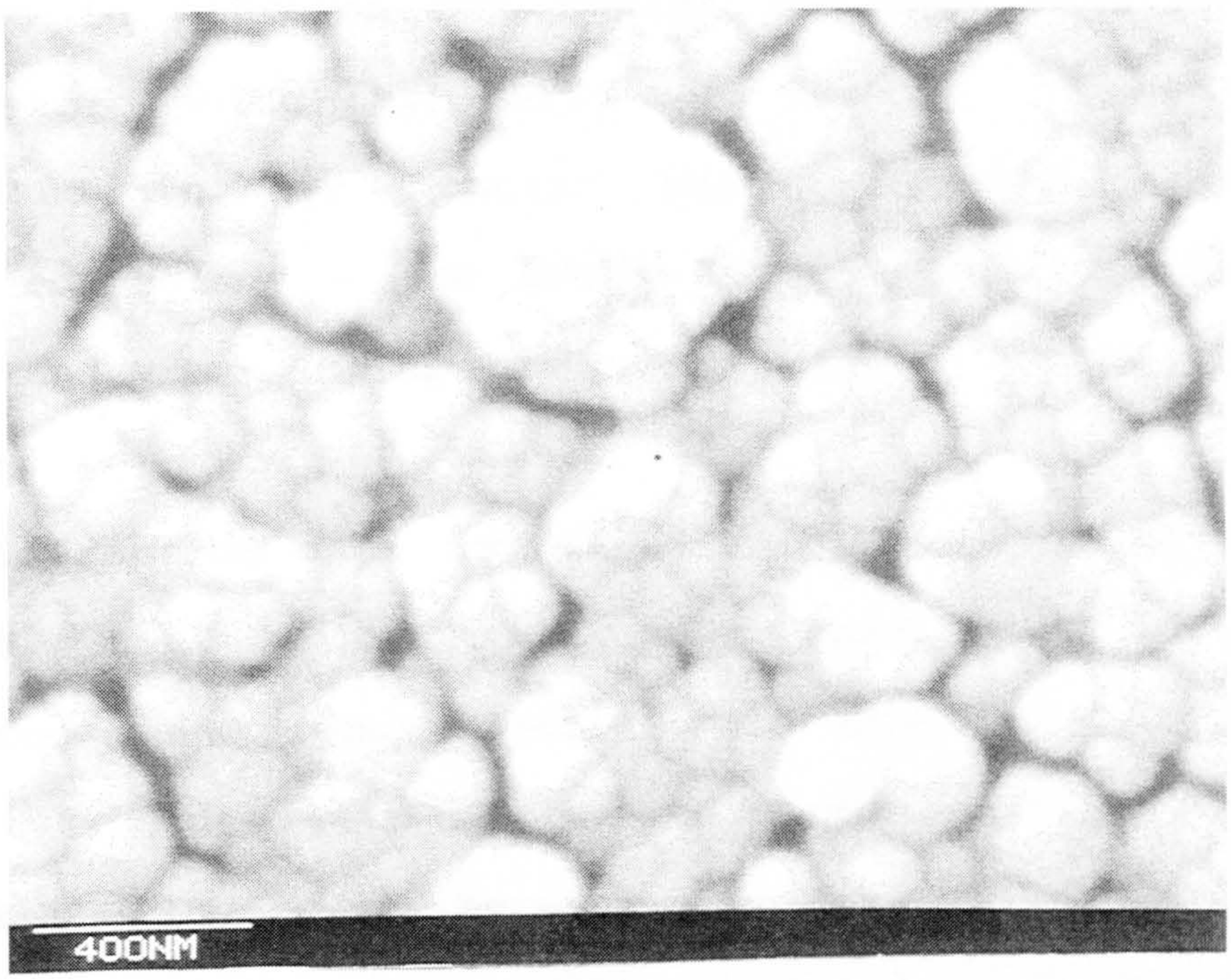


Fig.5.23(a) Secondary electron micrograph of a CdTe layer produced by annealing a Cd/Te stack at 450°C in vacuum

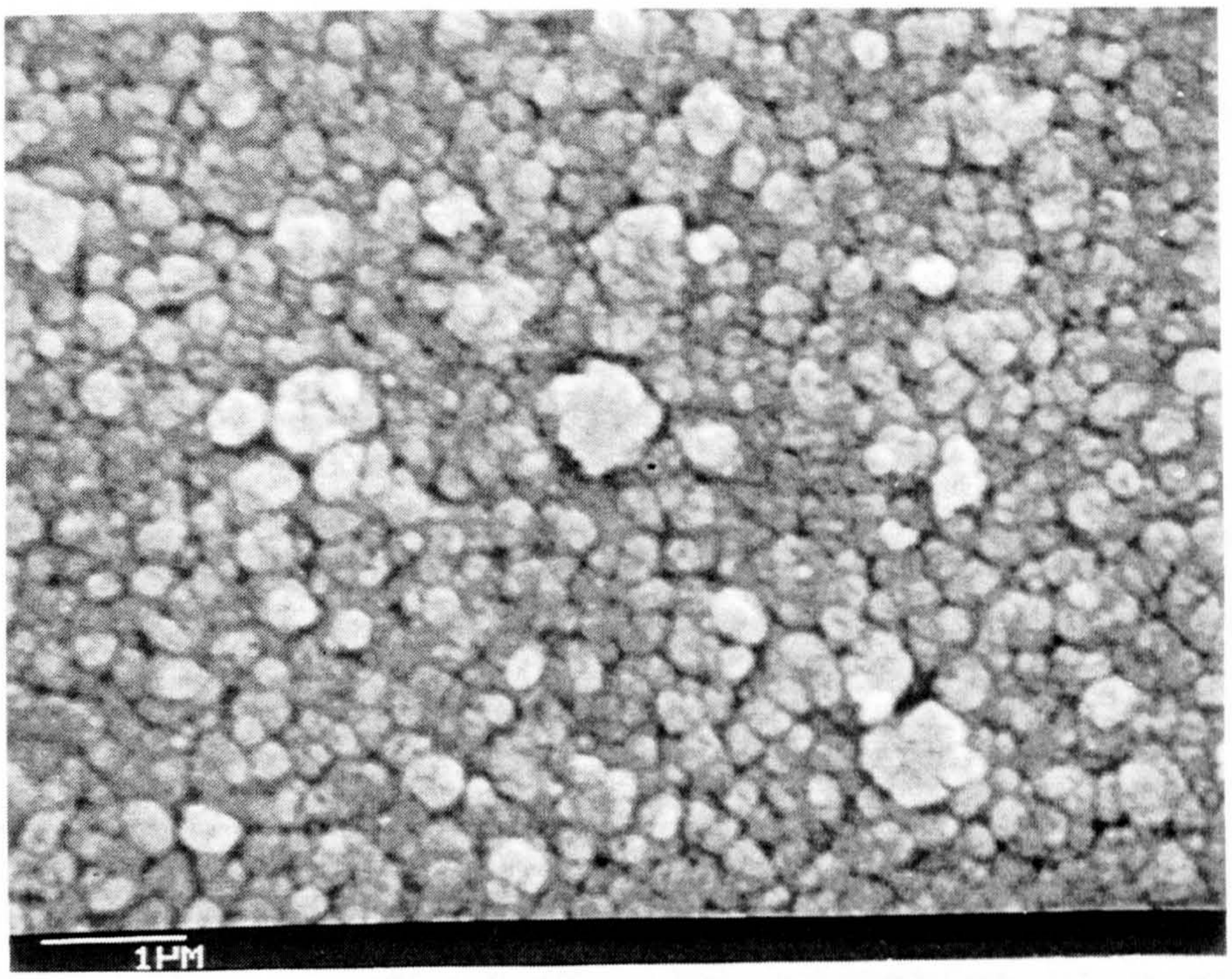


Fig.5.23(b) Secondary electron micrograph of a CdTe layer produced by annealing a Cd/Te stack at 450°C in air

annealing in nitrogen and vacuum are very similar the grain size being typically ≈ 1000A°. The layers synthesized in air however have slightly different surface morphology - the grains are slightly larger on average and some grains are very large , up to 1μm in diameter.

X-ray diffraction data for the three layers is given in fig.5.24. It is apparent that the layers synthesized in the nitrogen and vacuum environments have the sphalerite crystal structure with no second phase material present where as the layers synthesized in air give rise to extra diffraction peaks corresponding to reflection from the (20-2), (10-3), and (221) planes respectively of $CdTeO_3$. The formation of $CdTeO_3$ when annealing CdTe in air has in fact been observed by various workers [36] indicating that the interpretation of the data made here is reasonable.

The F.W.H.M. of the (111) reflection is significantly smaller for the layers synthesized by annealing in air than for the layers synthesized by annealing in the nitrogen or vacuum environments, consistent with the S.E.M. observations that the grain size is lower for the former anneals. The F.W.H.M. for the layers synthesized in vacuum was 0.41° i.e. similar that using the nitrogen anneal and correspond to a grain size ≈ 220A° calculated using the Scherrer formula.

Transmittance versus wavelength data for the three samples is given in fig.5.25 , the variation of α versus λ , derived from the transmittance data in conjuction

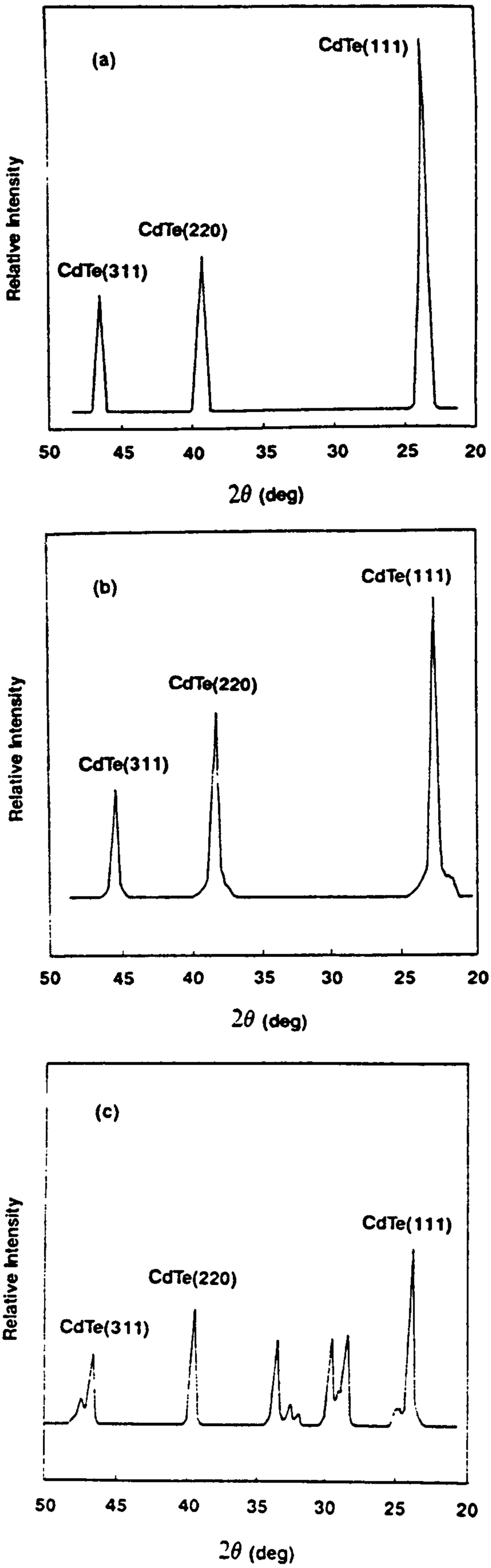


Figure 5.24 X-ray Diffraction Data for CdTe Produced by Annealing Repeated Stacks in (a) Nitrogen, (b) Vacuum, and air (F.W.H.M. of (111) Peak: (a) 0.42° (b) 0.47° (c) 0.29°)

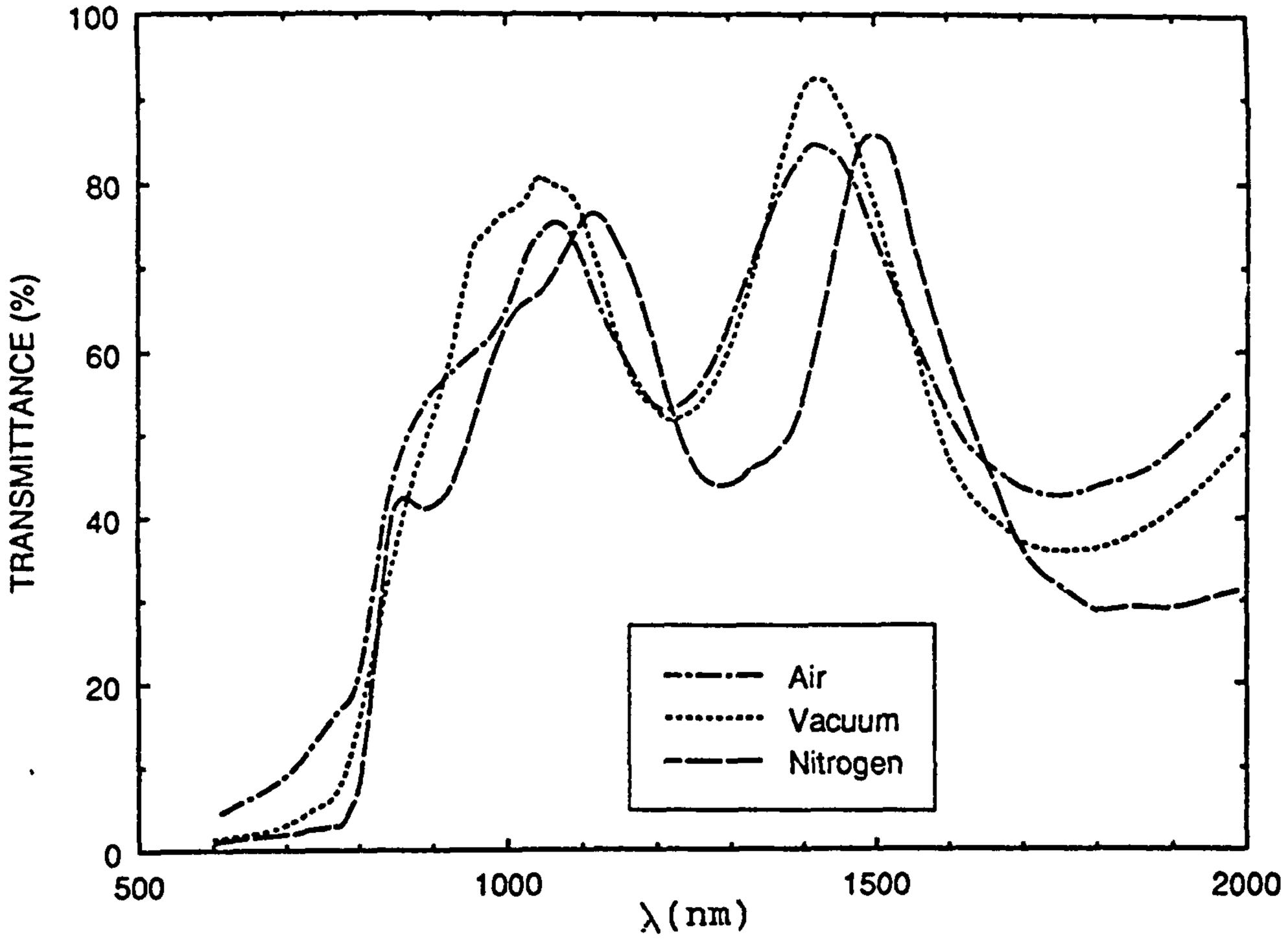


Figure 5.25 Transmittance Versus Wavelength for CdTe Produced by Annealing Cd/Te Stacks (a) in Nitrogen, (b) in Vacuum and (c) in air

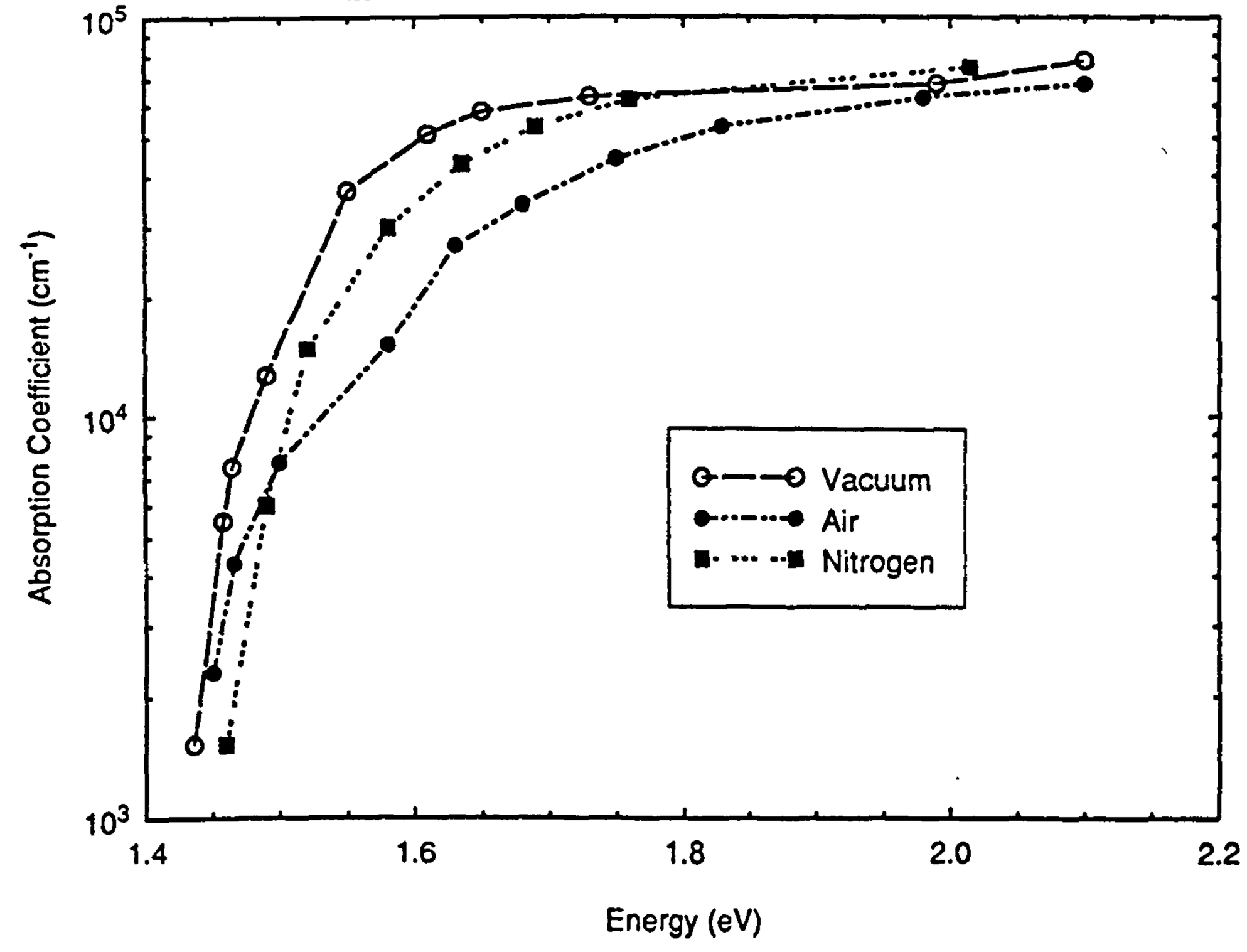


Figure 5.26 α Versus hv for the CdTe Produced by Annealing Repeated Te/Cd Stacks (a) in Nitrogen, (b) in Vacuum and (c) in air

with reflection data in fig.5.26, and plots of $(\alpha hv)^2$ versus hv in fig.5.27. It is apparent from the data that CdTe was successfully synthesized using the three different environments.

5.9 Properties of the CdTe Produced by the Co-evaporation of Cd With Te:

Thin films of CdTe were also produced by coevaporating Cd with Te onto heated substrates. Adherent thin films, free from pinholes were obtained using a substrate temperature of 200 °C and deposition rates of 12 A°/ sec (15-18 Hz) for both of the elements. The tellurium source temperature used was 273°C and the cadmium source temperature, 160°C. The source temperatures were adjusted manually to keep the deposition rate as constant as possible during the deposition. Film thicknesses > 1.5μm were obtained for deposition times of 20 minutes.

Transmittance versus wavelength data is given in fig.5.28, a plot of α versus hv in fig.5.29., and a plot of $(\alpha hv)^2$ versus hv in fig.5.30. The steep absorption edge at $\lambda \approx 850$ nm (1.5eV) confirm that CdTe was successfully synthesized using this method.

When the CdTe was heated to 450 °C after dipping in a solution of $CdCl_2$ in methanol (10g/l) the absorption edge was shifted to higher value of wavelength, as shown in fig.5.31 and the energy bandgap reduced to 1.47 eV as shown in fig.5.32 and fig.5.33. Such a reduction in energy bandgap due the $CdCl_2$/methanol heat treatment has been observed by the other workers [40] and is attributed

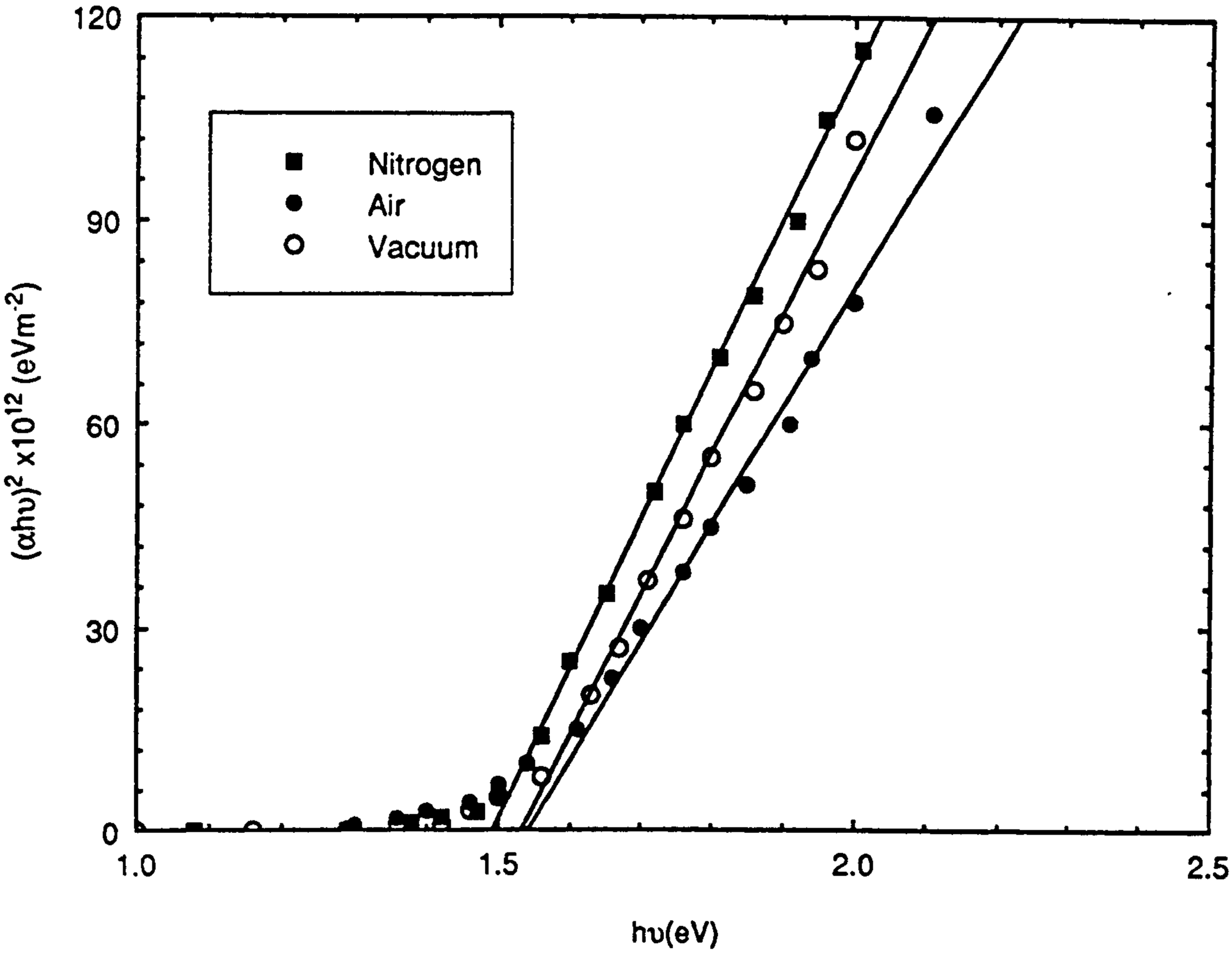


Figure 5.27 $(\alpha hv)^2$ Versus hv for the CdTe Produced by Annealing Repeated Te/Cd Stacks (a) in Nitrogen, (b) in Vacuum and (c) in air

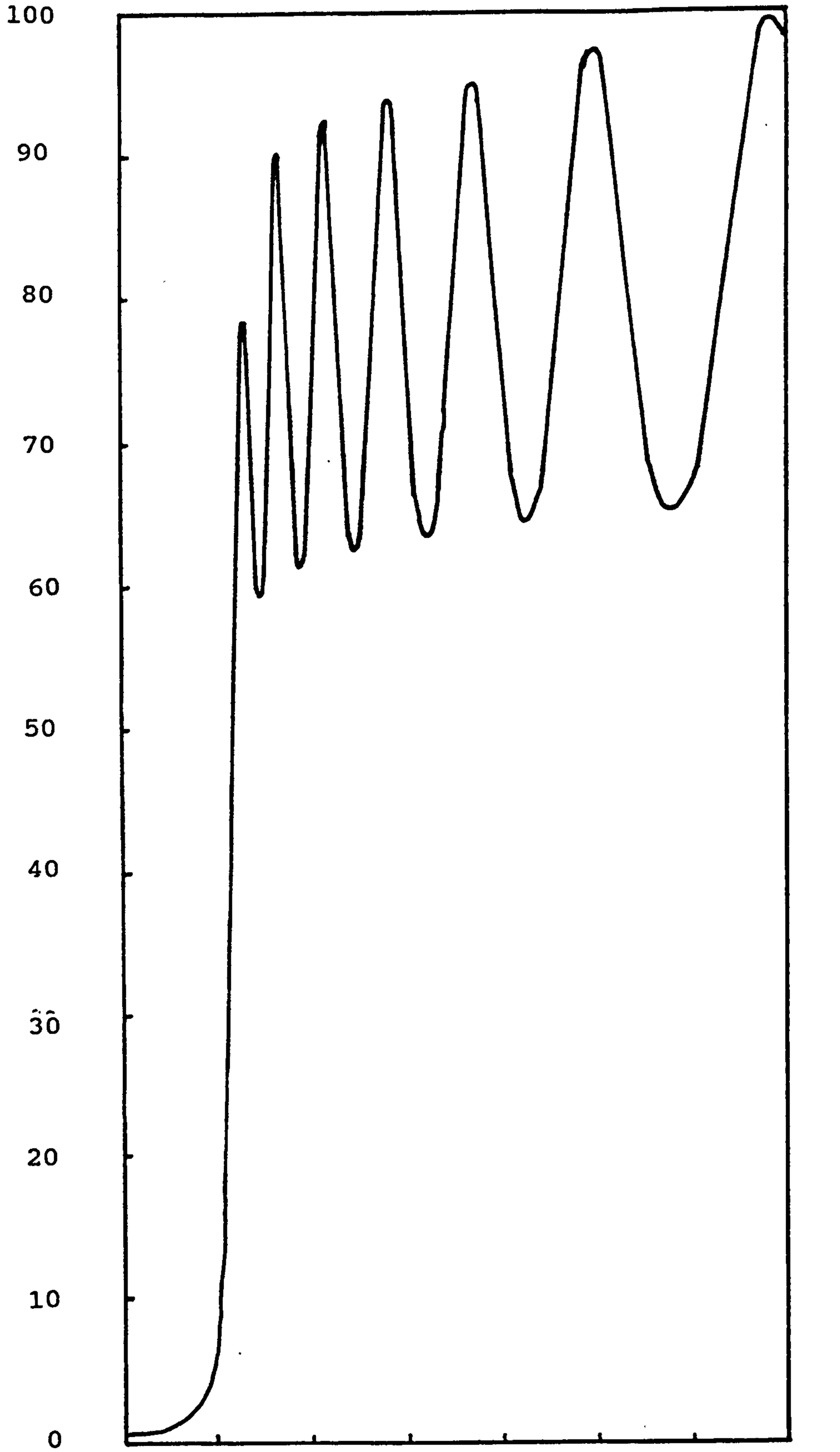


Figure 5.28 The Variation of Transmittance Versus Wavelength for a CdTe Thin Film Produced Using Co-evaporation.

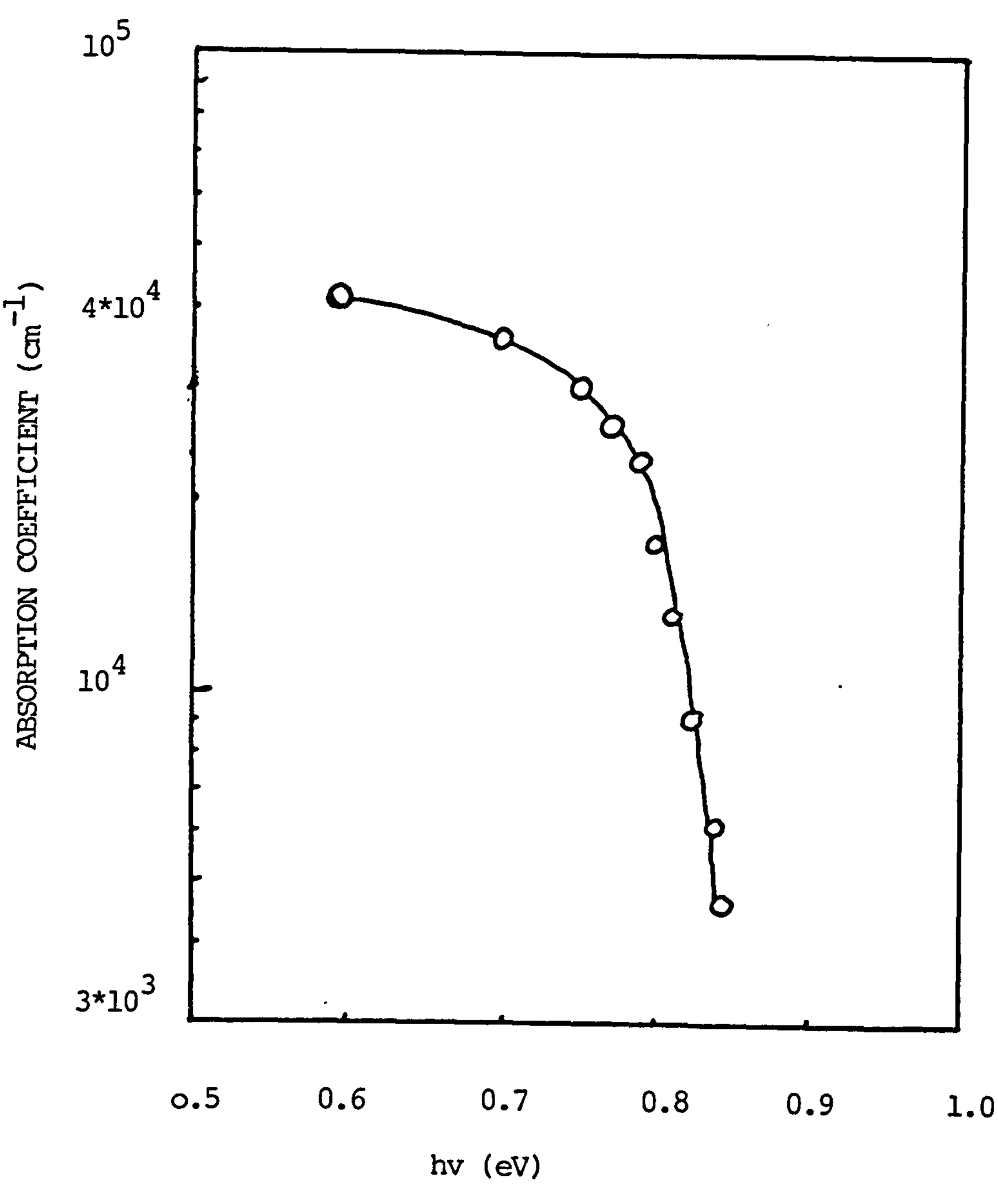


Figure 5.29 α Versus hv for the CdTe Produced by Co-evaporation

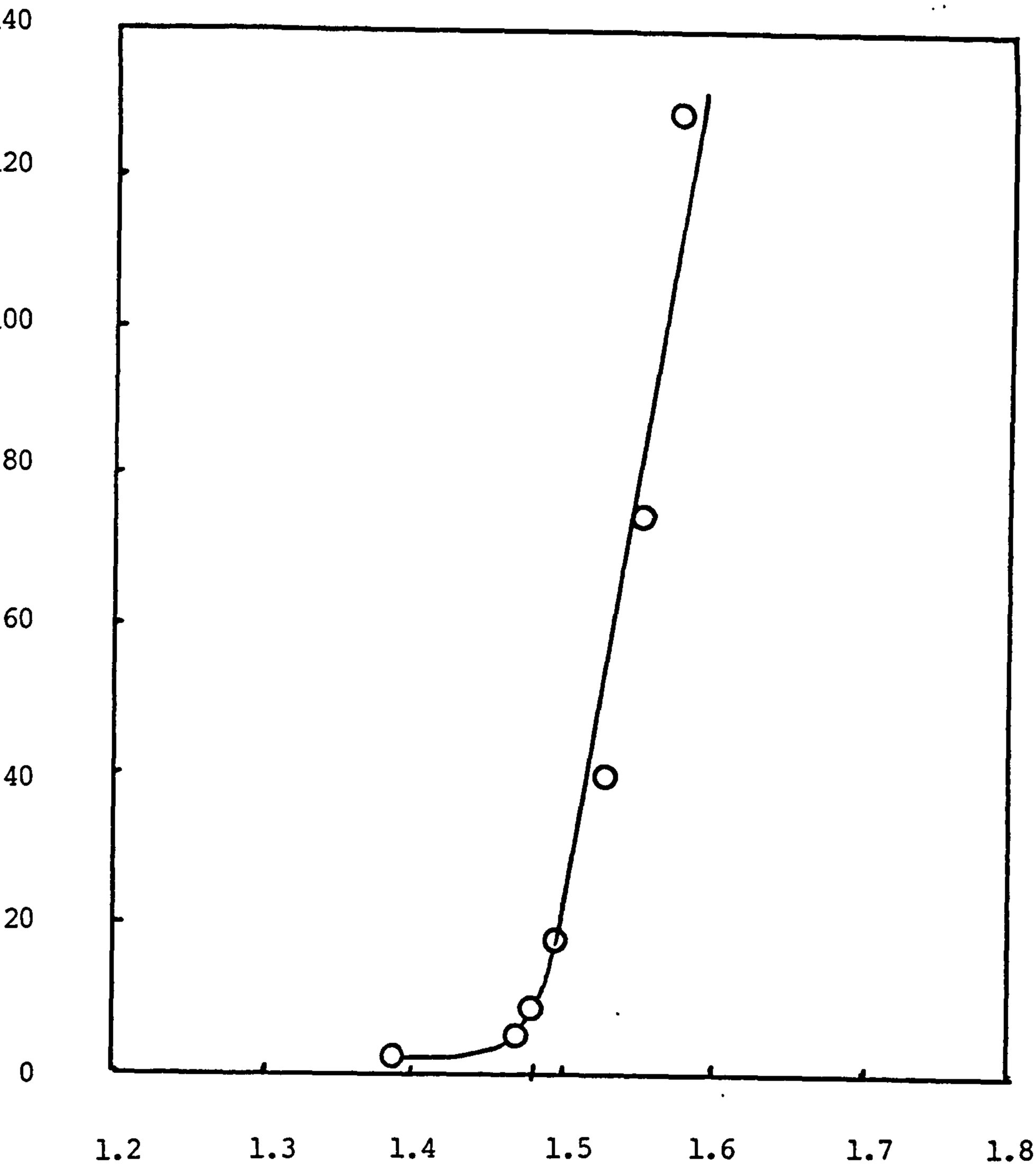


Figure 5.30 Variation of $(\alpha hv)^2$ Versus (hv) for the Co-evaporated Cadmium Telluride

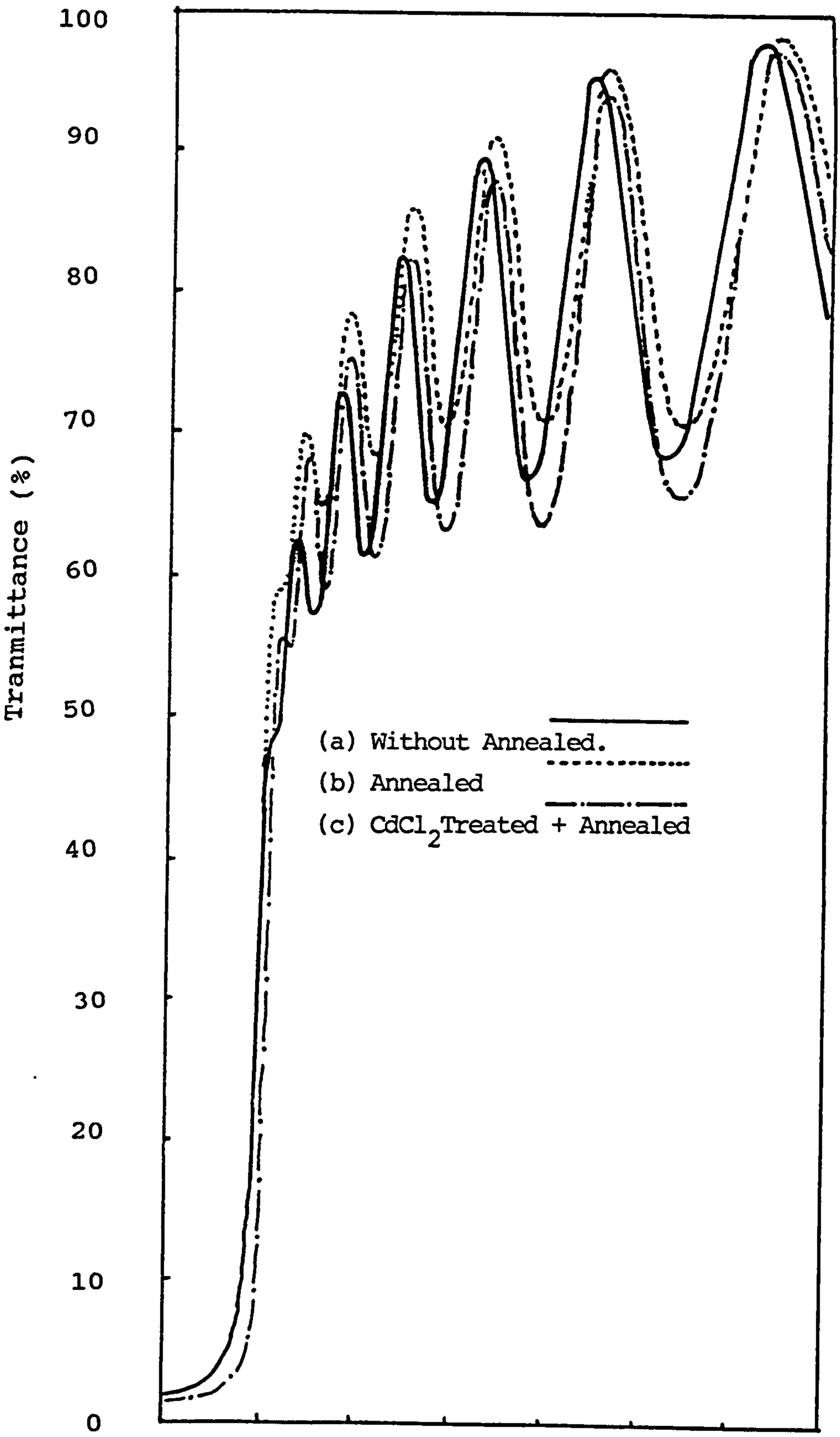


Figure 5.31 Transmittance Versus Wavelength for a CdTe Thin Film Produced Using Co-evaporation (a) for as-grown Sample (b) for an Unannealed Sample Treated With $CdCl_2$/Methanol and Then Annealed.

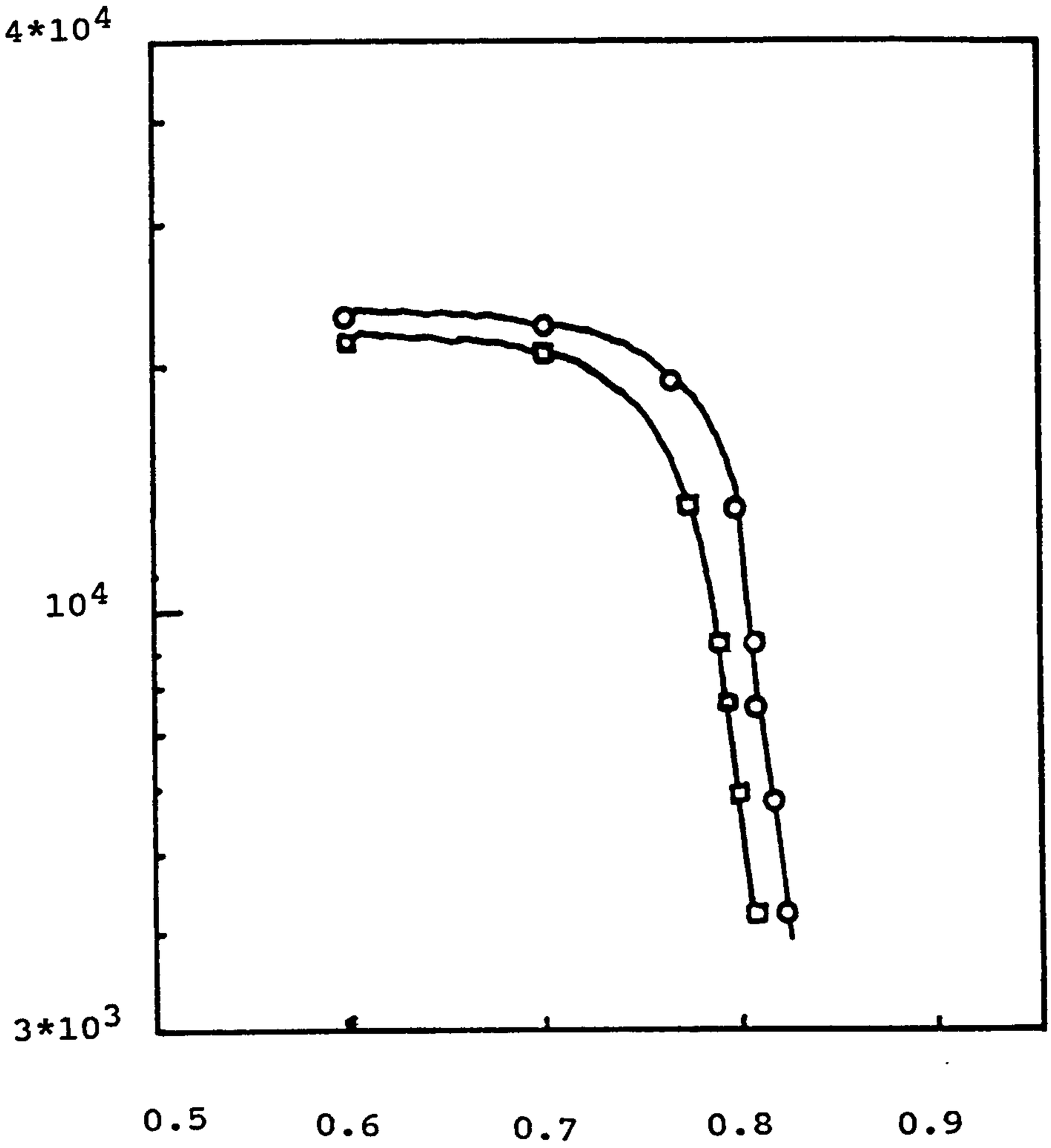


Figure 5.32 α Versus λ for a CdTe Thin Film Produced Using Coevaporation (a) Prior to the $CdCl_2$/Methanol Heat Treatment (b) After $CdCl_2$/Methanol Heat Treatment

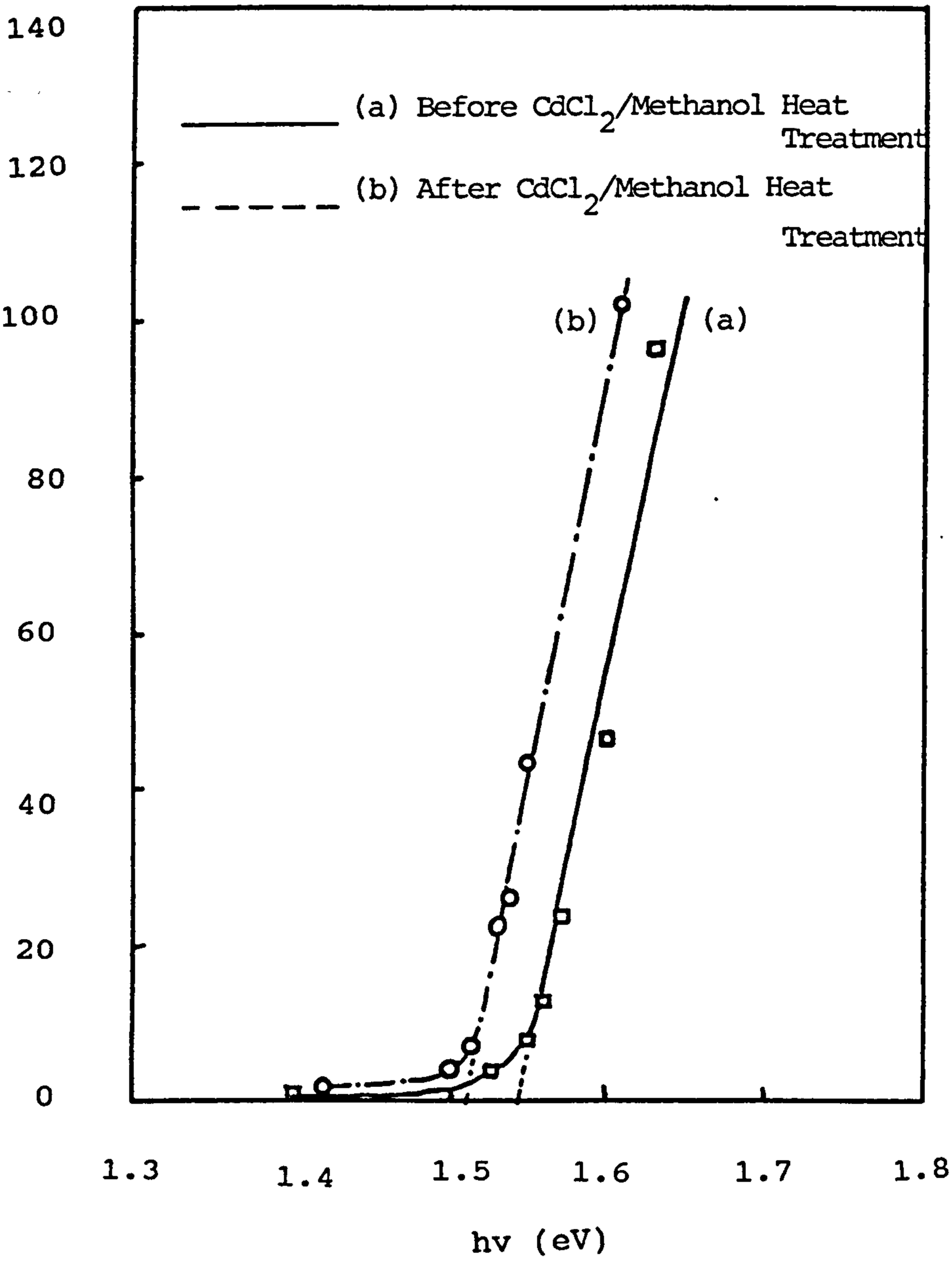


Figure 5.33 $(\alpha hv)^2$ Versus hv for CdTe Thin Film Produced Using Co-evaporation (a) Before $CdCl_2$/Methanol Heat Treatment (b) After the $CdCl_2$/Methanol Heat Treatment

to the $CdCl_2$/methanol heat treatment introducing shallow states into the energy bandgap reducing the effective bandgap of the material [37,38].

The refractive index, n, of the layers was calculated from the transmittance and reflectance data obtained using the method given by [39].

A plot of refractive index versus wavelength for a film produced using coevaporation and for a film produced using S.E.L. processing is given in fig.5.34 For these films (that were not heated with $CdCl_2$ in methanol solution) the refractive index is observed to be much higher for the films produced using coevaporation than for the films produced using S.E.L. processing.

X-ray diffraction data for a film produced using coevaporation is given in fig.5.35 It is evident that these films had the wurzite structure (hexagonal) crystal structure (see fig.5.22). The difference in refractive index of the CdTe layers produced using the different methods can thus be attributed to the different crystal structures that result from using these different methods of synthesis. Similar differences in the values of refractive indexes for cubic and hexagonal structure CdTe have been reported [3].

5.10 Cadmium Chloride Heat Treatment:

Although the CdTe synthesized by annealing the stacks in nitrogen, vacuum and air had good mechanical strength and good optical properties, the problems remained that columnor grain growth was not achieved during the

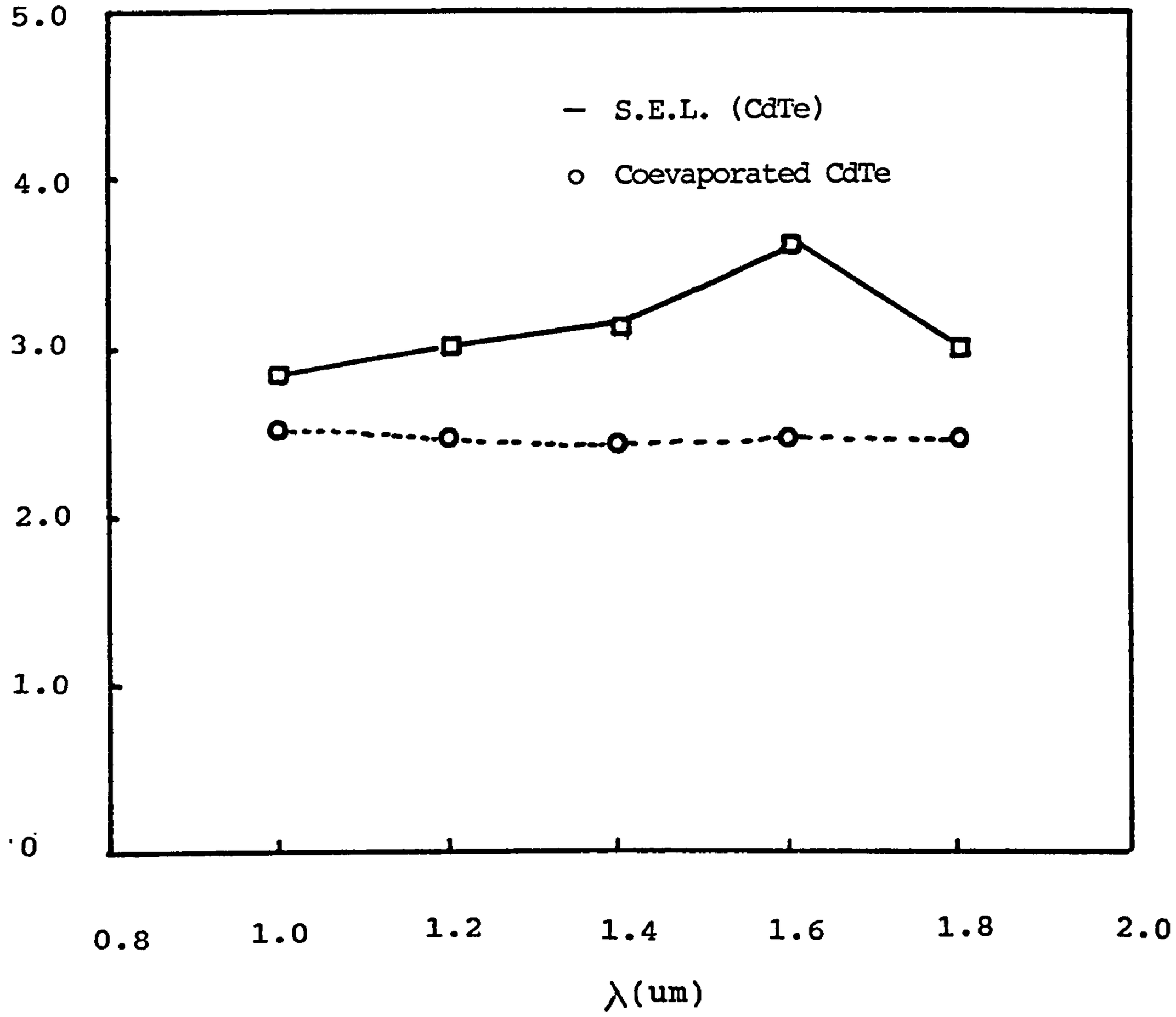


Fig.5.34 Variation of Refractive Index Versus Wavelength for the Cadmium Telluride Thin Films Produced Using S.E.L. Processing and Co-evaporation Method.

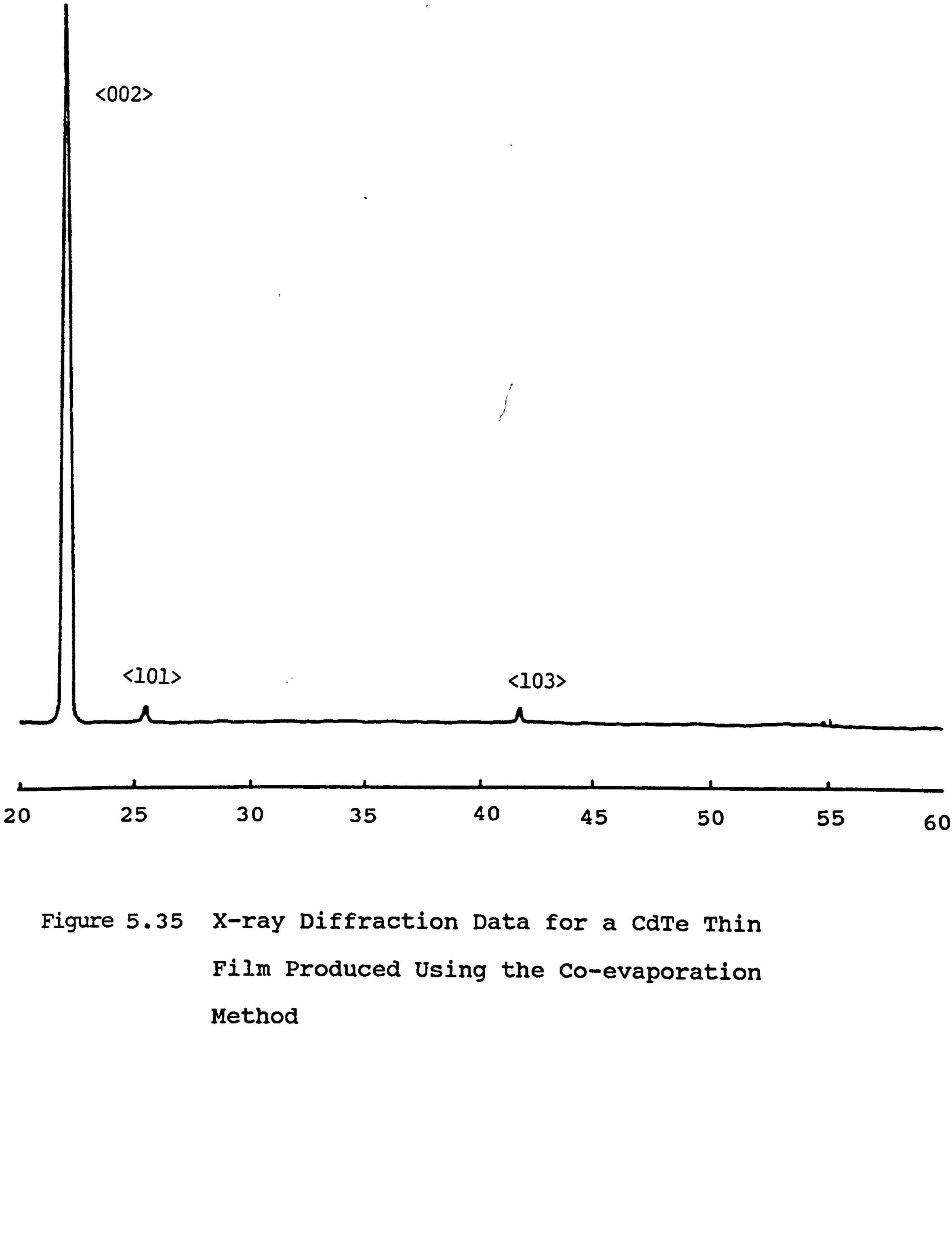


Figure 5.35 X-ray Diffraction Data for a CdTe Thin Film Produced Using the Co-evaporation Method

synthesis and the grain size remained small even for the synthesis in air. Further, p-type layers were only produced when the layers were synthesized in air, they had high resistivities and their production was not very reproducible as most of the layers formed were n-type. These layers also contained $CdTeO_3$ as a second phase material and its presence would probably be detremental to solar cell performance [36].

It had been reported by several workers, including Moon et al [41], Matsushita [44] and Burgleman et al [45,46] that the addition of $CdCl_2$ in the slurry used to make CdTe layers by screen printing significantly improved the efficiency of the solar cells produced using this material. The solar cells produced by Bonnet [42] in which the CdTe was produced using the C.S.S. process were similarly improved by adding $CdCl_2$ dissolved in methanol to the CdTe followed by heating the sample in air. It was hence decided to investigate the influence of heating the CdTe samples produced by SEL processing in the presence $CdCl_2$ to determine whether the layers could be improved.

Initial attempts involved using a solution of $CdCl_2$ in methanol (suggested by Bonnet [43]) mixed in a ratio 1 : 100 by mass. The $CdCl_2$ was dissolved in the methanol by heating the mixture to 80°C for 25 minutes and then allowing the solution to cool back to room temperature. Drops of solution were placed on the surface of the CdTe and the sample heated in air at 50 °C intervals upto 550 °C using an anneal time of 15 minutes at each temperature. An annealing temperature of 450 °C was

found to result in a significant change in the grain structure and in the size of the grains within the samples. The grain size was increased to > 5000°A over the entire surface area (see in fig.5.36(a) & (b)) and in some regions grains as large as 1μm in diameter were produced. Similar results were obtained for the CdTe previously synthesized by annealing the stacks in nitrogen, vacuum and air environments.

Uniformity of the grain growth across the entire sample area was found to be achieved by simply dipping the CdTe into the $CdCl_2$methanol solution prior to the anneal rather than placing drops onto the surface. The grain size was further improved by altering the ratio of $CdCl_2$: methanol and optimising the annealing temperature for each concentration of $CdCl_2$ in methanol used . Using such an approach it was found possible to produce samples with columnar grains > 1μm in diameter over the entire sample area, as shown in fig.5.37(a) & 5.37(b).

To achieve such grain growth the concentration of $CdCl_2$ in methanol had to be greater than 10 gm./l. If the solution had a concentration below this value the grains produced were not as large as those obtained with the 10g/l solution and they were also not well shaped or orientated (see fig.5.38). If the concentration of $CdCl_2$ in methanol was greater than this value then annealling in air at 450 °C resulted in a residue left on the surface of the samples which was possibly "unreacted" solute. Further it was found that when such layers were etched using a solution of bromine in methanol, pinholes

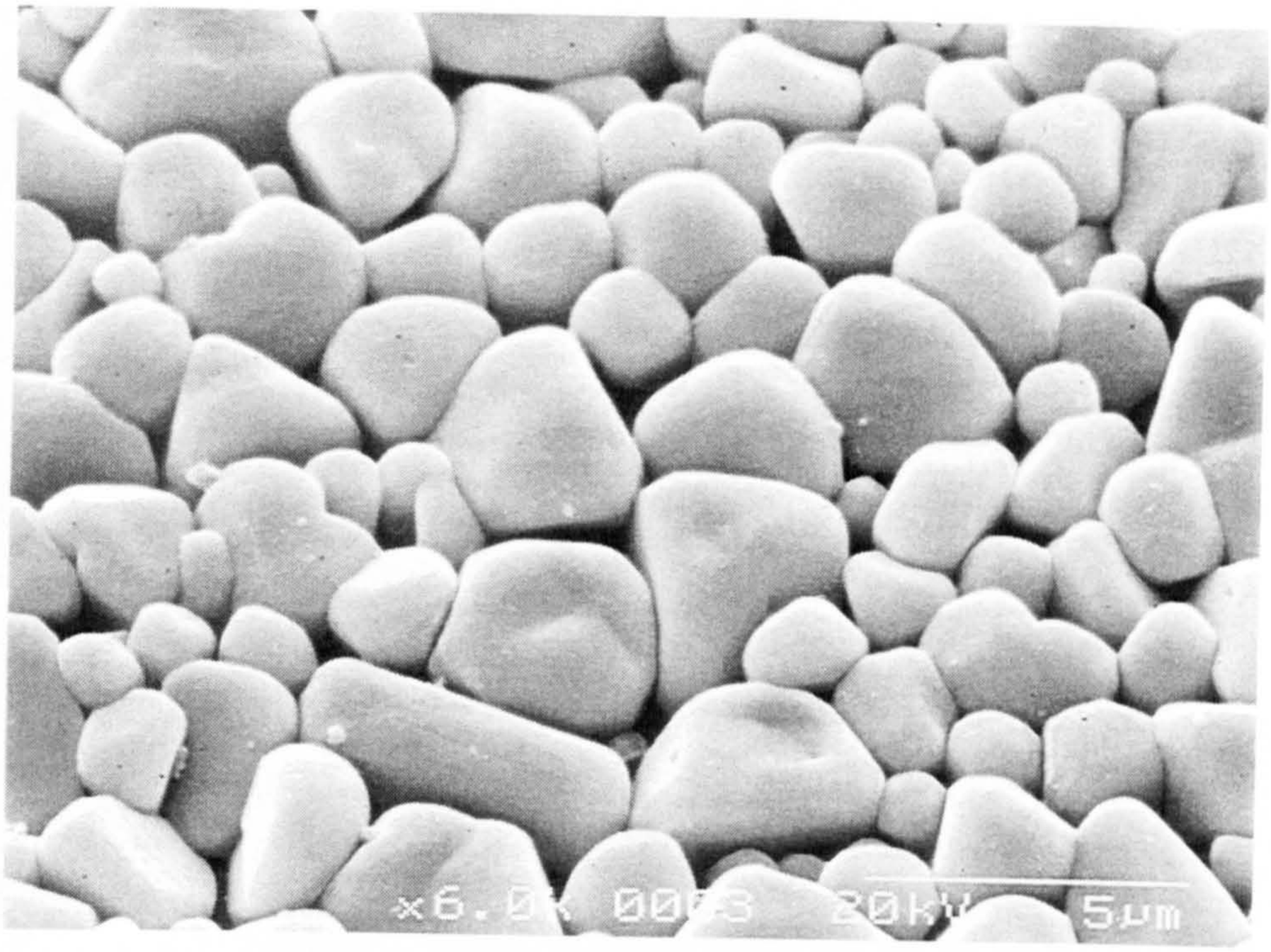


Figure 5.36 (a)SEM Micrograph of the Layer Produced by Annealing a Te/Cd Stack in Nitrogen Followed by $CdCl_2$/Methanol Heat Treatment -Plan View

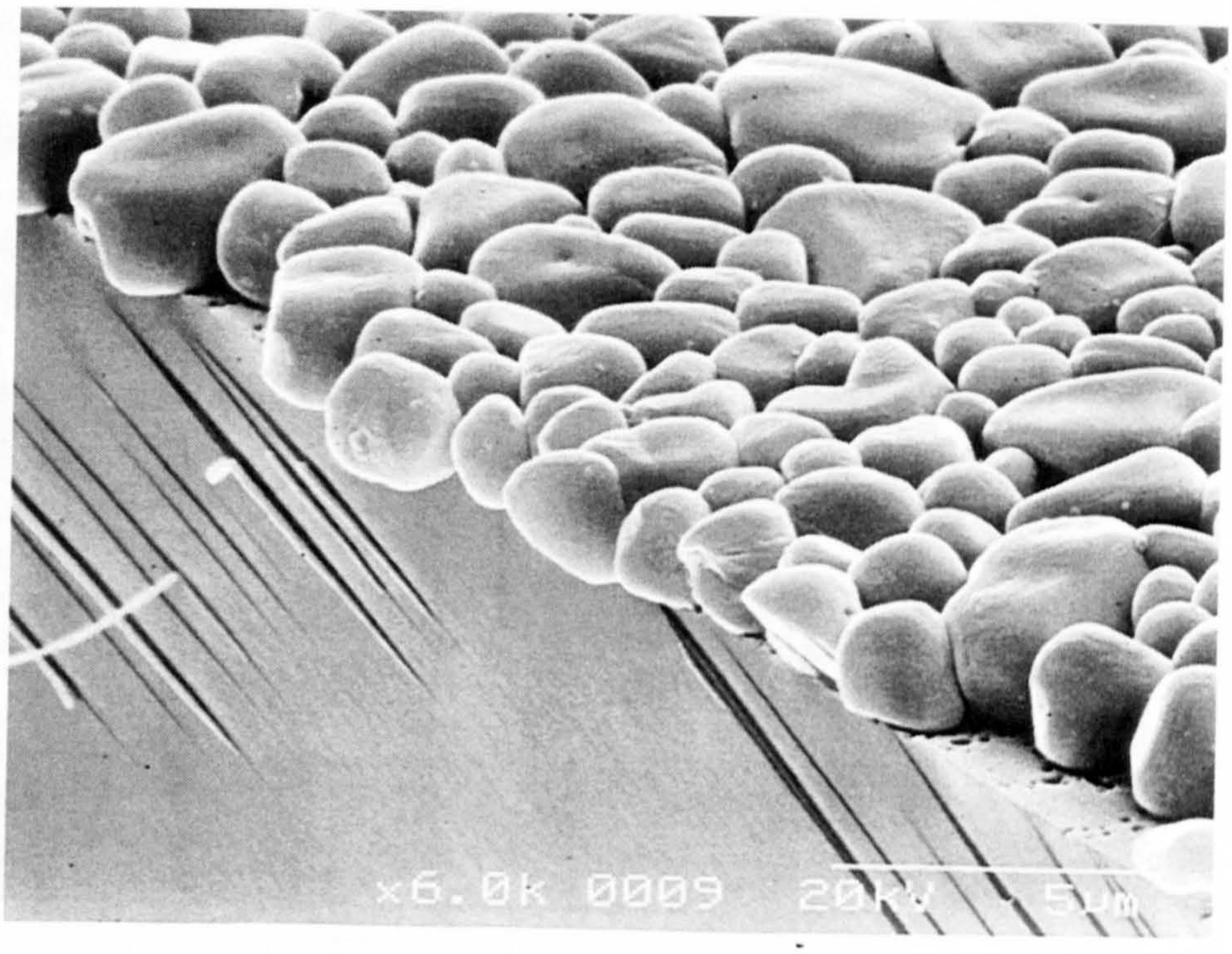


Figure 5.36 (b) SEM Micrograph of a Layer Produced by Annealing a Cd/Te Stack in Nitrogen Followed by $CdCl_2$/Methanol Heat Treatment - Side View

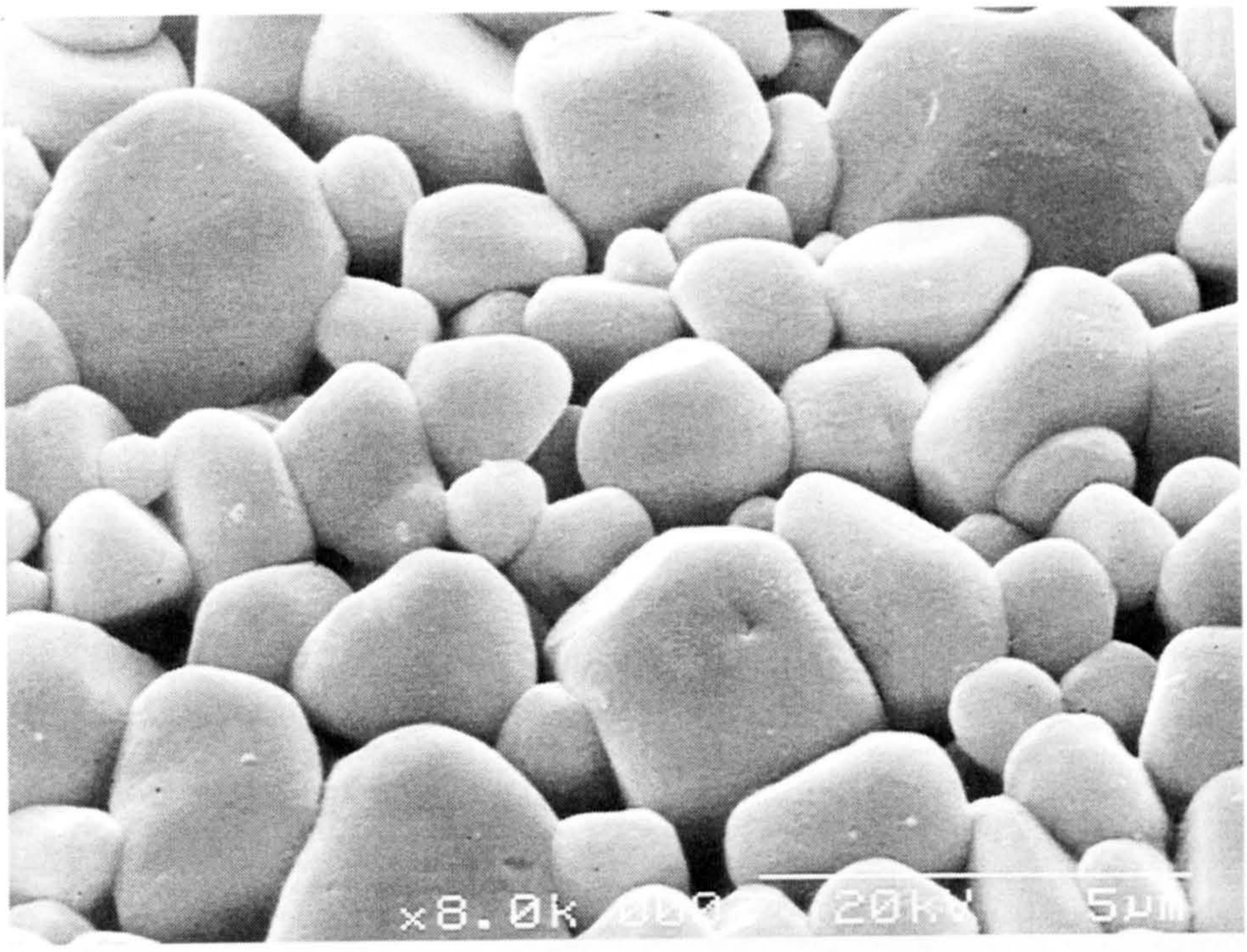


Figure 5.37 (a) SEM Micrograph of a Thin Film of CdTe - Plan View

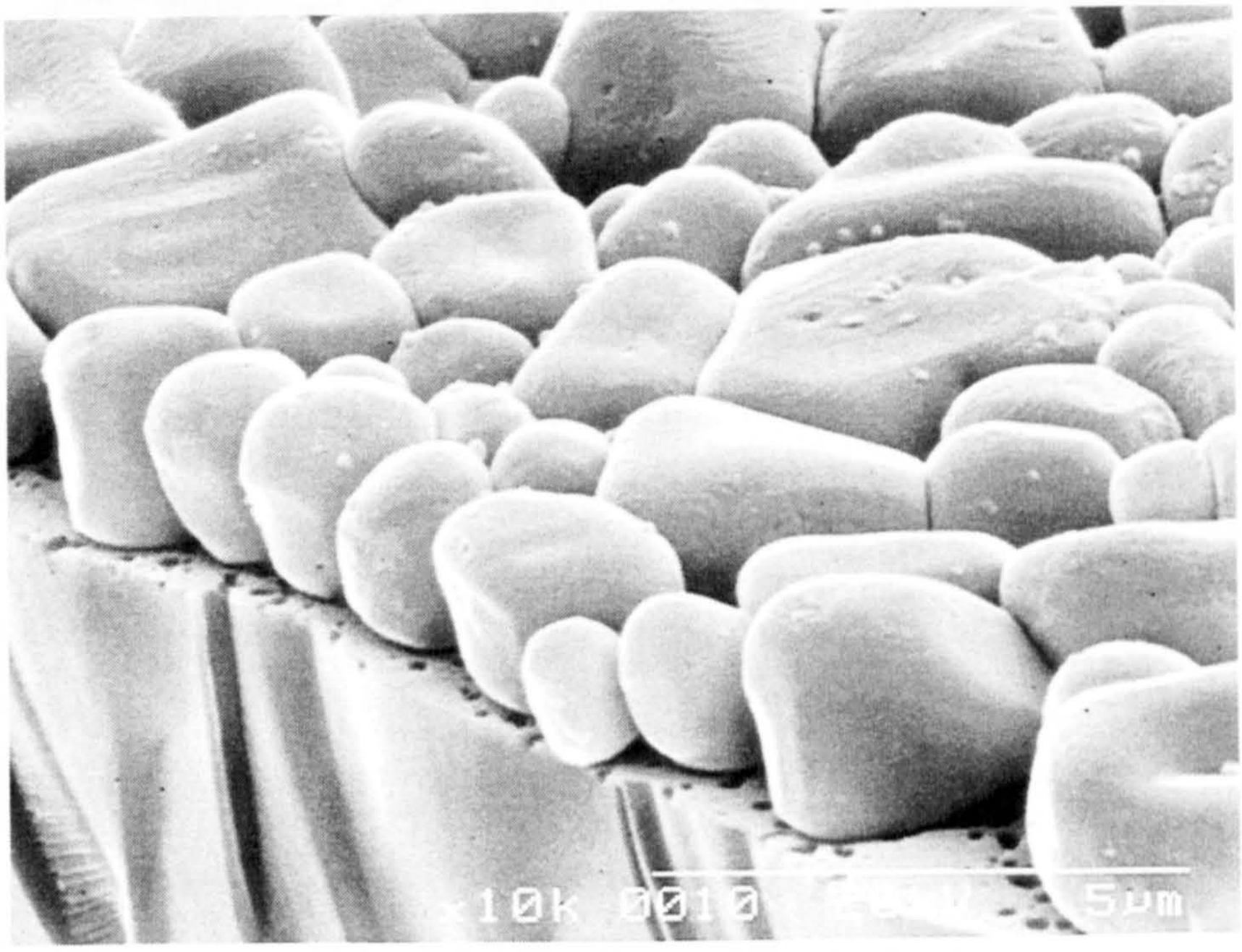


Figure 5.37 (b) SEM Micrograph of a Thin Film of CdTe -Side View

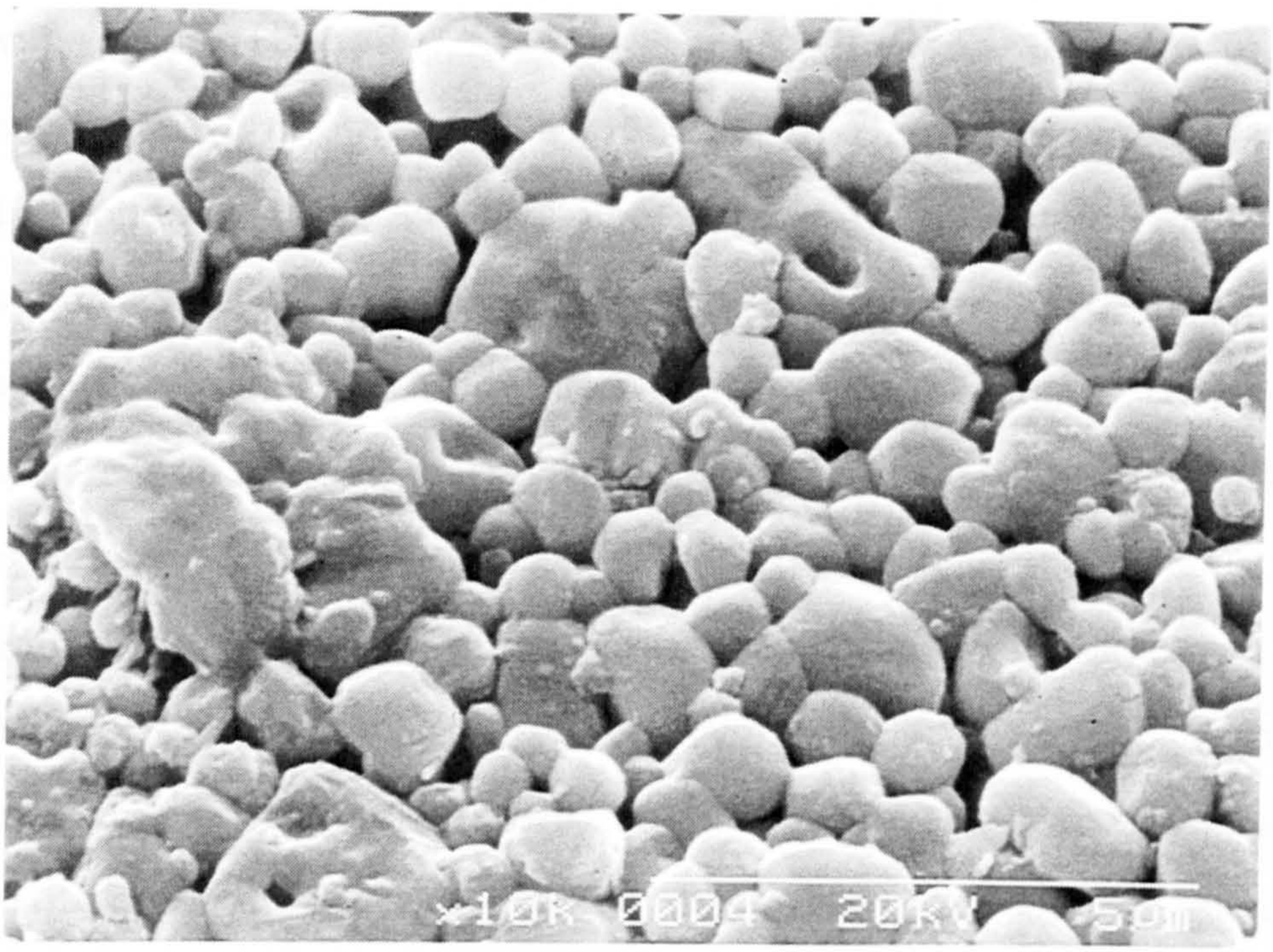


Figure 5.38 SEM Micrograph of Cadmium Telluride Heat Treated using 5.0gm/l Concentration of $CdCl_2$ in Methanol

were produced in the samples which were not present when the solute concentration was ≤ 10gm/l. A concentration of 10 gm/l was hence considered to be optimum to produce columnar grain growth without the above mentioned undesirable effects. X-ray diffraction data for a layer of CdTe previously synthesized by annealing the CdTe stacks in nitrogen followed such an optimum heat treatment is shown in fig.5.39. It is apparent that single phase CdTe with the sphalerite structure was produced. The F.W.H.M. of (111) peak was now 0.21° as opposed to the 0.4° obtained if the $CdCl_2$ heat treatment was not used. Using the Scherrer formula the F.W.H.M. corresponds to a grain size ≈ 430 A°.

It should be noted that similar results were obtained for the layers that were previously synthesized in vacuum. For the layers synthesized in the air environment X-ray diffraction data is given in fig.5.24(c). It is evident that the second phase $CdTeO_3$ is still present and hence such layers were probably not as useful for solar cell applications as those synthesized in nitrogen. Although such an annealing strategy was successful further experiments were performed to investigate the possibility of improving the process further. One approach involved thermally evaporating a layer of $CdCl_2$, with a thickness in the range 0.05-1μm directly onto the top of a Cd/Te stack followed by an anneal in nitrogen to synthesize the CdTe. A $CdCl_2$ source temperature ≈ 370°C was used. Single phase CdTe was produced and an increase in grain

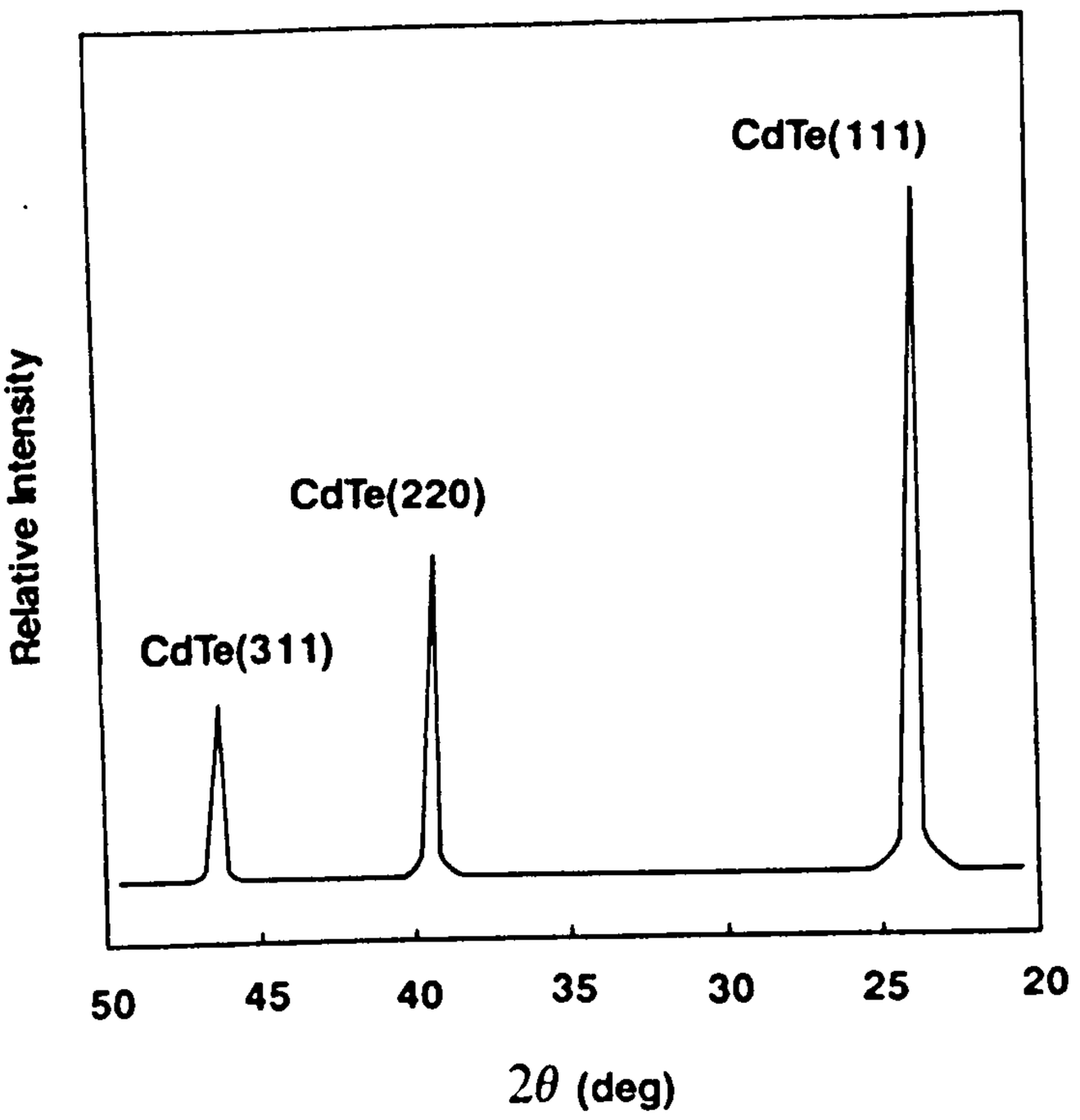


Figure 5.39 X-ray Diffraction for a CdTe Thin Film Produced Using S.E.L. Processing and Given the Optimum $CdCl_2$/ Methanol Heat Treatment.

size to ≈ 347A° achieved. The F.W.H.M. of the (111) peak in this case was reduced to 0.26°.

It was also possible to deposit alternate layers of Te with $CdCl_2$ mixed with Cd followed by an anneal of the structure at 450 °C for 15 minutes. Some grain growth was again achieved and the F.W.H.M of the (111) peak in this case reduced to 0.35°.

Yet another strategy involved dipping the repeated Cd/Te stacks into the solution of $CdCl_2$ in methanol solution [10g/l] followed by an anneal at 450 °C for 15 minutes. This process proved to be unsuccessful as the layers produced were not adherent to the substrate.

A summary of the results of these experiments is given in table 5.1. The samples dipped into the $CdCl_2$/methanol solution and then annealed at 450 °C in either air, vacuum or nitrogen were found to be p-type using the hot-probe method.

Fig.5.40 shows how the thermoelectric e.m.f. varied for a sample that had been synthesized in nitrogen and then annealed at various temperatures in air. It is evident that the thermoelectric e.m.f. changes sign from positive to negative at a temperature of 400°C, corresponding to a change in the samples from n-type to p-type. This temperature is close to that at which the $CdCl_2$ interacts with the CdTe to change the grain structure of the material.

It is evident that the $CdCl_2$ heat treatment does not only enhance grain growth but it also plays an important role in converting the samples from n-type to p-type.

TABLE 5.1

Sr. No.	Stacks + Annealing Environments	Anneling		SEM Studies Grain Size(A°)	X-ray Studies		Brief Comments
		Temp(C°)	Time(mins)		FWHM <111>	Grain-Size,A°	
1	Te/Cd/Te..stack + synthesised in N_2.	450	15	1000	0.42	215	Cubic structure
2	Te/Cd/Te..stack + synthesised in vacuum.	450	15	1000	0.41	220	Cubic structure
3	Te/Cd/Te..stack + synthesised in air.	450	15	5000	0.286	316	Cubic structure + $CdTeO_3$
4	Te/$CdCl_2$/Te.. stack + synthesised in N_2.	450	15	2000	0.35	258	Cubic structure
5	Te/Cd/Te..stack + Synthesised in N_2+ $CdCl_2$ evaporated + annealed in N_2	450	15	-----	0.26	347	Cubic structure
6	Te/Cd/Te... stack synthesised in N_2+ annealed in air	450	15	> 5000 Max. 30000	0.2	430	Cubic structure

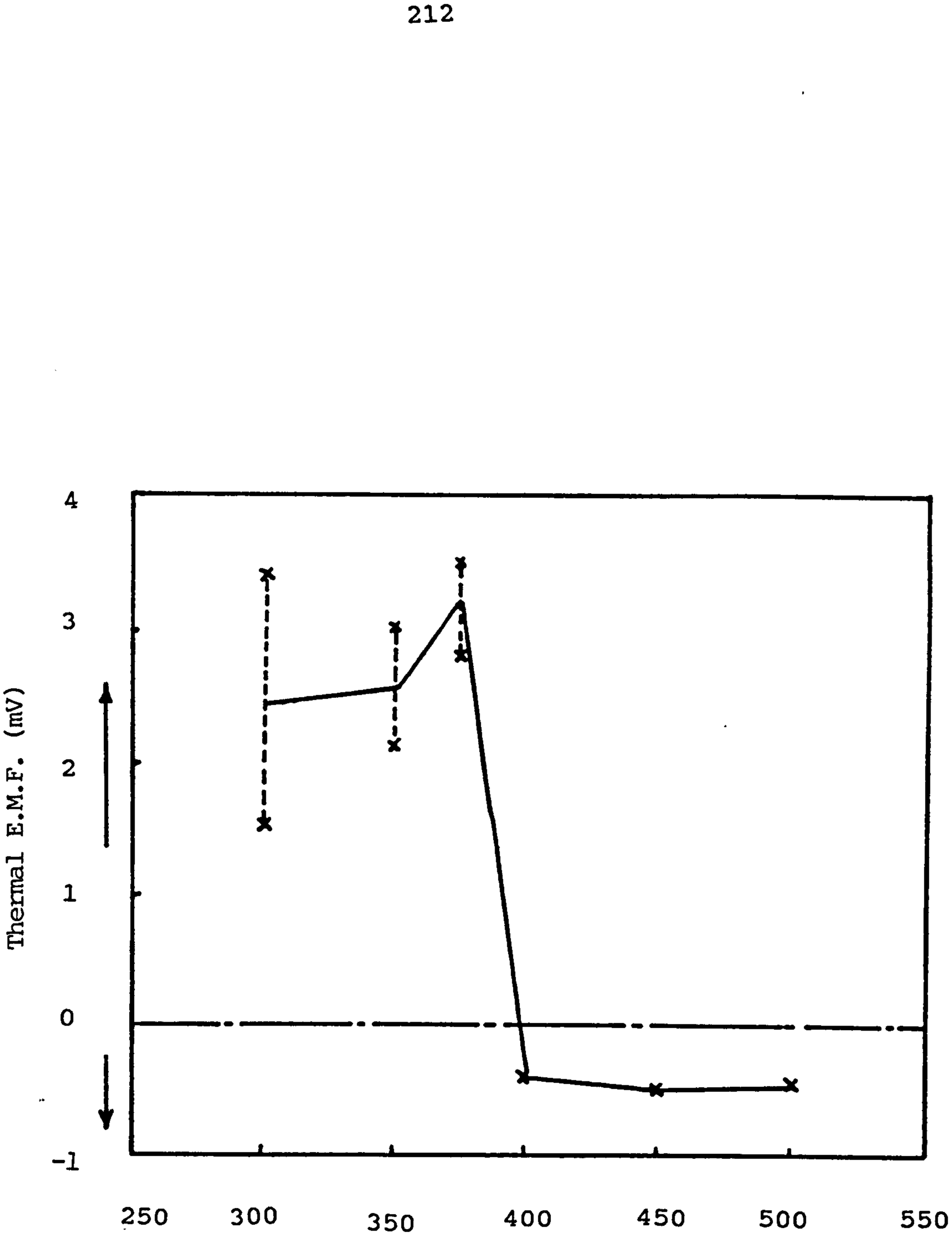


Figure 5.40 The Variation of Thermal e.m.f. Versus Annealing Temperature After the Sample had Been Given the $CdCl_2$ Heat Treatment

Etching the samples in a 0.1% solution of bromine in methanol for 30 seconds prior to making the hot probe measurements was found to increase the thermoelectric e.m.f. to a value in the range -60mV - -74mV (as opposed to -5 mV) which is the indication of relatively strong p-type behaviour compared to the unetched samples.

It is possible that this removed an insulating layer that had formed on the CdTe surface during the heat treatment in air. The resulting CdTe surface was also shiny indicative of a tellurium rich surfaces on the CdTe [47]. Such a tellurium rich surface is considered by several workers to be essential prior to making low resistance electrical contacts to p-type CdTe [48].

The role of $CdCl_2$ and oxygen in doping CdTe P-type is not fully understood [49,50]. The presence of both materials is considered to be essential to enhance the p-type character of polycrystalline CdTe films [29,52]. It is known that tellurium vacancies and cadmium interstitials should act as donors whereas cadmium vacancies and tellurium interstitials should act as acceptors [21]. Further chlorine is thought to act as an n-type dopant [51] whereas oxygen it thought to act as a p-type dopant [50]. Several workers believe that the $CdCl_2$ acts to permit easier incorporation of oxygen into CdTe by perhaps creating tellurium vacancies [40]. The most detailed study of the role of the $CdCl_2$ heat treatment on CdTe has been made by Rohatgi et al [52]. The photoluminescence spectra of the heat treated films had peaks at 7900 A° and 8400 A°. The broad band centred

around 8400 A° they attribute either to structural defects, native defects or to cadmium vacancy-chlorine complexes (based on [37,53]) whereas the peak at 7900 A° is attributed to cadmium vacancies (following [38]). Both the cadmium vacancy-chlorine complexes and cadmium vacancies have a p-type character. It could be that the incorporation of oxygen plays some rule in creating the cadmium vacancies. Alternatively the p-type character of the films may be the result of oxygen, cadmium vacancies and the cadmium vacancy-chlorine complexes doping the layers, the cadmium vacancies perhaps resulting from the loss of cadmium atoms during the anneal.

5.11 Electrical Properties of the CdTe Thin Films Produced:

The electrical properties of the thin films produced were investigated using the Van der pauw method and using thermoelectric power measurements as described in the section 4.6 and respectively.

For the former measurements electrical contacts had to be made to the CdTe thin films and these were formed at the corners of the square pieces of CdTe (which measured 1cm * 1cm). Following the experience of the other workers the following were used as contact materials : evaporated gold, conducting graphite paste, graphite paste mixed with $CuCl_2$ and graphite paste mixed with HgTe.

The samples produced using S.E.L. processing even after the $CdCl_2$/methanol heat treatment were found to be very resistive ; the resistance was so high in fact that a

measurable current flow was not achieved through the samples. Annealing the samples to temperatures > 400 °C to "diffuse" in the contact materials failed to overcome this problem.

It was only after etching the samples for 30 Secs using a solution of 0.1% bromine in methanol and then depositing the contacts that a measurable current flow was achieved. Such a surface treatment has been found by other workers to be an essential step for forming ohmic contacts to the CdTe produced using other methods [54,55]. This etch is considered to produce a tellurium rich surface on the CdTe [56].

The most promising samples were found to be produced by synthesizing the CdTe in nitrogen, following by dipping the samples in the 10g/l solution of $CdCl_2$ in methanol and then annealing in nitrogen at 450°C for 15 minutes. Etching using the bromine methanol solution followed by the use of gold contact or conducting graphite paste cotacts lead to reproducible values of resistivity. The resistivity were found to be in the range 500-1000 Ω-cm and the Hall constant in the range $1.86*10^{-3}$-$8.2*10^{-3}$ m^3c^{-1}.

These values corresponds to Hall mobilities in the range 16.4-18.6 $cm^2V^{-1}s^{-1}$ and hole concentration in the range $7.6*10^{14}$-$3.6*10^{16}$ cm^{-3} if the formulae $\mu_H=R_H/e$ and $p=1/R_He$ are used. These values are comparable to those obtained for the CdTe produced using the C.S.S. method; p ≈ $6*10^{14}$-$5*10^{16}cm^{-3}$, μ ≈ $40cm^2V^{-1}s^{-1}$ or < 10 $cm^2V^{-1}s^{-1}$,[57,59], the electrodeposition method; p ≈ $1.5*10^{16}$-

$5.9*10=16cm^{-3}$, [58,61], the screen printing method; p ≈ $2.3*10^{15}$-10^{13} cm^{-3},[41] and the R.F(sputtering) method ; p ≈ $10^{14}cm^{-3}$,[62].

It should be noted that performing the $CdCl_2$/methanol heat treatment in air rather than in nitrogen leads to pinholes being produced during bromine/methanol etch. The nitrogen used probably contained a small residual concentration of oxygen which was adequate to play a role in doping the layers. Using air the concentration of oxygen was much higher and it is possible that a surface oxide was formed during the $CdCl_2$/methanol anneal which was more difficult to remove with bromine methanol etchant. The samples producing by co-evaporating Cd and Te were found to be p-type with resistivities in the range 450-470Ωcm for the as grown samples, in the range 10^6-10^7Ωcm after the $CdCl_2$/methanol heat treatment and in the range 10^4-10^5Ωcm after bromine methanol etch.

Thermoelectric power measurements was made on the S.E.L. processed CdTe samples that had been given the CdTe heat treatment in nitrogen.

The thermoelectric power, α_T, is given by the slope of a graph of how thermoelectric e.m.f. varies with temperature difference between the hot and cold probes.

For the unetched samples the thermoelectric e.m.f. was small < 7.5mV and the data so scattered it was not possible with confidence to discern a trend and hence to determine α_T.

Etching the samples using 0.1% bromine in methanol and

then repeating the measurements however resulted in data such as that shown in fig.5.41.

For the data given in fig.5.41 α_T = 0.31mV/°C. The thermoelectric power was measured for the S.E.L. processed CdTe samples annealed in nitrogen at 450°C after dipping into $CdCl_2$/methanol solutions with different concentrations in the range 3.5-20g/l as shown in fig.5.42. It is evident the thermoelectric power is a maximum for a concentrations of $CdCl_2$ in methanol equal to 10 g/l. It is interesting that this value is the same as that established previously to ensure good , columnar growth of the CdTe layers.

It is possible to use the values of α_T obtained to deduce the hole concentration in the layer using the formula given by [63-66] :-

$$p = 4\pi m^* kT/\{h^3 \ln^{-1}[B \pm \alpha_T q/k]\} \qquad 5.6$$

To determine the value of p the "scattering constant", B, should however be known. From [67]

B = 0.5 or 1 for amorphous semiconductors.

B = 2 for acoustic phonon scattering.

B = 3 for polar optical phonon scattering,

and

B = 2.5 for neutral impurity scattering.

Using α_T = 0.31 mV/°C and taking extreme values for B i.e. B=1/2 and B=3 then $p \approx 3.2*10^{19} - 3.9*10^{20} cm^{-3}$.

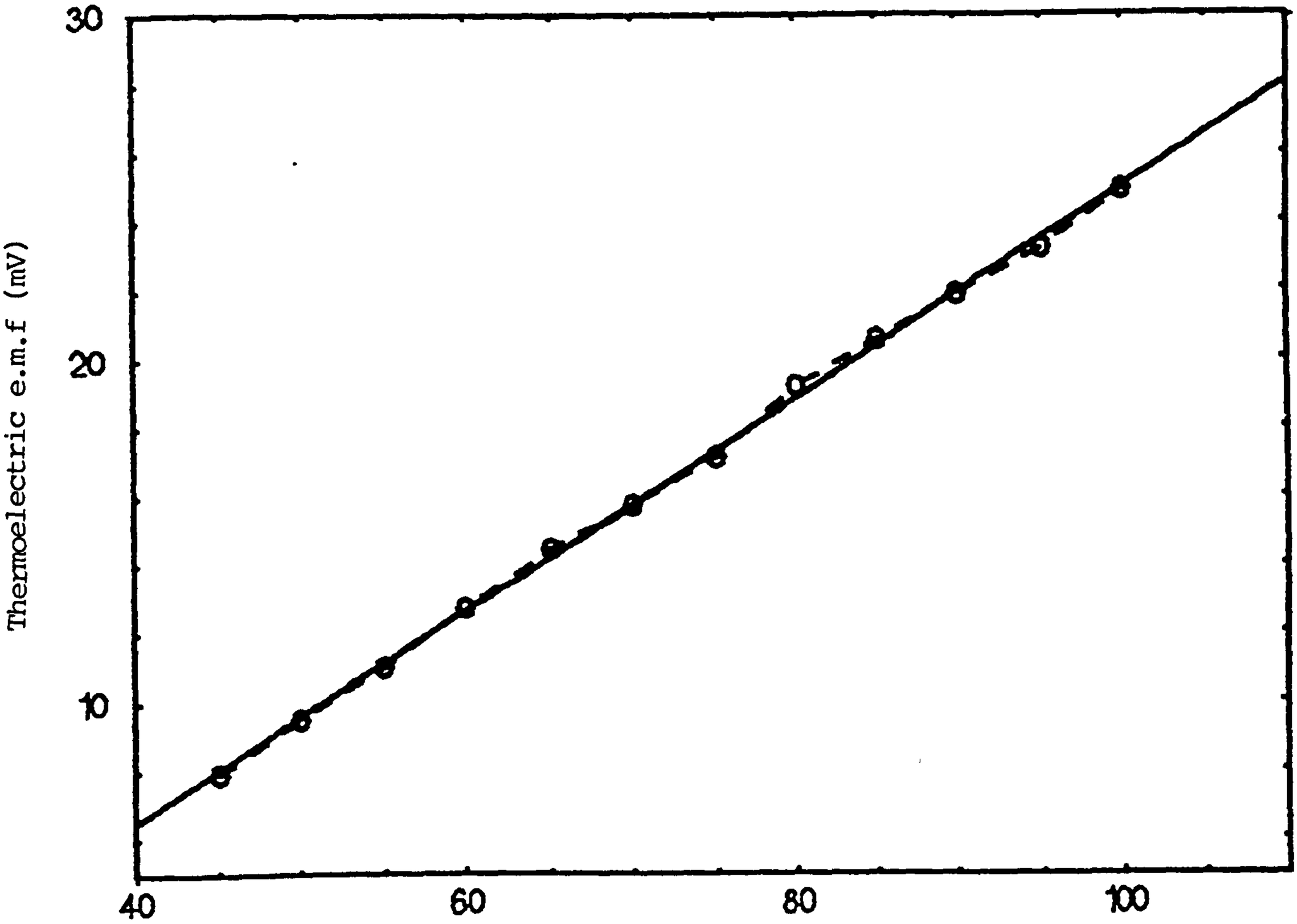


Figure 5.41 Thermoelectric Power Measurements of CdTe Produced by S.E.L. Method.

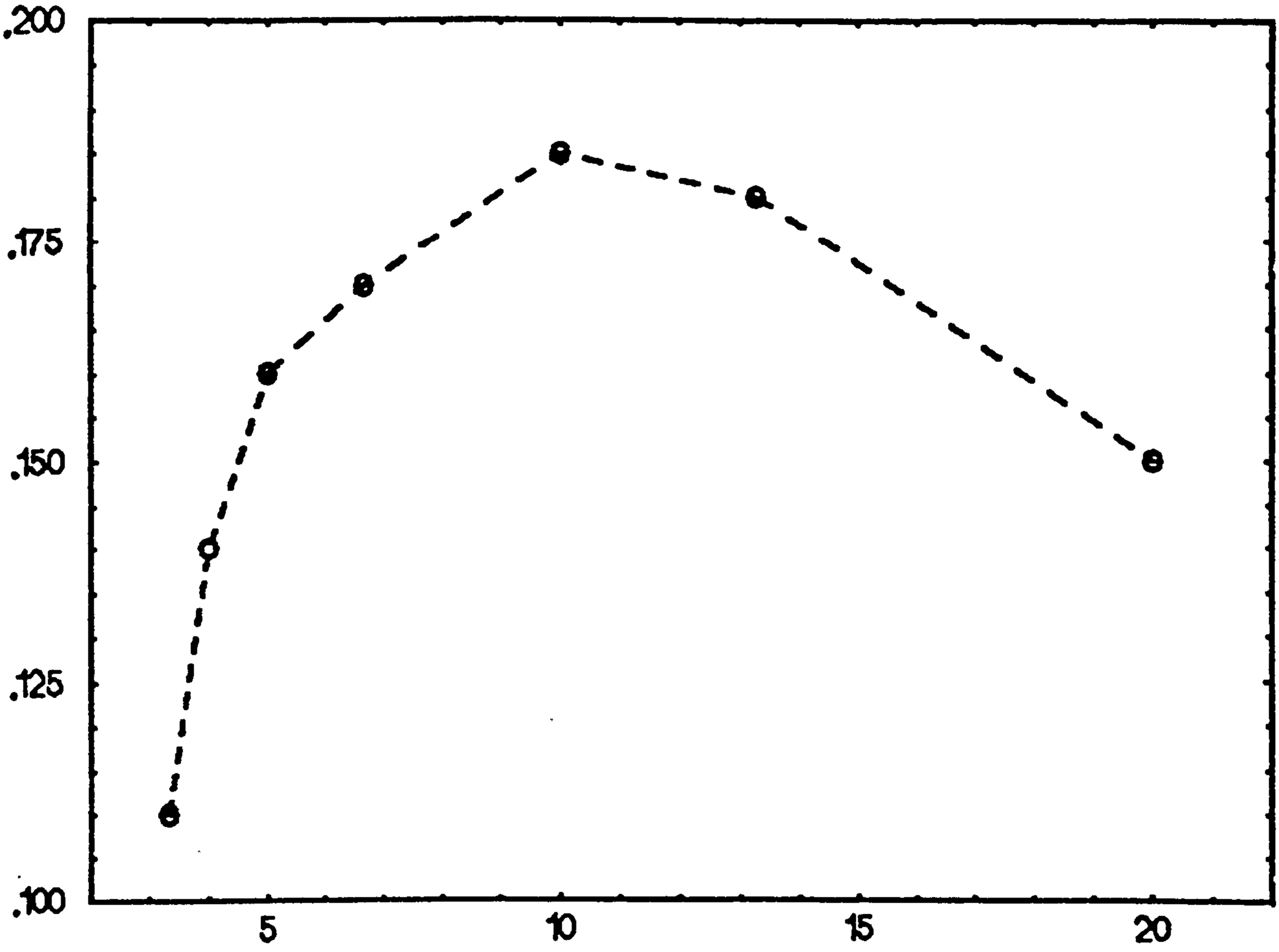


Figure 5.42 Effect of $CdCl_2$/Methanol Heat Treatment on Etched CdTe Thin Films

The values of p obtained are hence very much higher than those determined using the Van der Pauw method and much higher than the carrier concentrations usually observed in CdTe.

It is possible that the measurements are strongly influenced by tellurium rich surface of the CdTe which is much more conductive than the underlying CdTe.

5.12 The Production of Solar Cell Devices:

The substrates used for solar cell fabrication were indium tin oxide (I.T.O) coated glass slides with an I.T.O. thickness of 400 $^{\circ}$A and an I.T.O. resistivity of 8-10 Ωcm. On top of the I.T.O. layer, a thin layer of CdS, typically 1.5 - 2μm thick and with a resistivity of 50 - 100Ωcm was thermally evaporated using the procedure described in section 4.3.

The Cd and Te layers were deposited onto such CdS/I.T.O./glass substrates using the conditions described in section 4.1 and the entire device then annealed in nitrogen, vacuum or air to synthesis the CdTe. A back contact was then made to CdTe to complete the device.

The first device fabricated and then studied used CdTe layers, approximately 1.2 μm thick, and a thermally evaporated gold or copper back contact. Although the CdTe layers synthesized in nitrogen, vacuum or air were highly resistive and only some of the layers synthesized in air were p-type, it was possible that an anneal in air after the back contact was deposited could dope the CdTe p-type

by the incorporation of oxygen into the layer or by the indiffusion of gold or copper from the back contact extrinsically doping the material.

The devices fabricated were found to have low values of $J_{s.c.} < 100\mu A\ cm^{-2}$ and low values of $V_{o.c.} < 400$ mV even when the devices were annealed in air after the back contact was formed.

The key step to improve $V_{o.c.}$ and $J_{s.c.}$ significantly was to dip the devices into a solution of $CdCl_2$ in methanol, after the CdTe had been synthesized , and the device then annealed in air or nitrogen at a temperature > 400°C for 15 minutes.

Fig.5.43 shows how $V_{o.c.}$ and $I_{s.c.}$ vary with the concentration of $CdCl_2$ in methanol used if the samples are annealed at 450°C for 15 minutes in nitrogen. It is evident that the is an optimum concentration of $CdCl_2$ in methanol, of 10gm/littre to maximize both $V_{o.c.}$ and $J_{s.c.}$ for a given device. This concentration is exactly that needed to dope the CdTe strongly p-type and to ensure the good columnar growth (see section 5.10). The improvement of $V_{o.c.}$ and $J_{s.c.}$ may hence be attributed directly to the change from the material consisting of small, randomly oriented grains to material consisting of large columnar grains.

Fig.5.44 shows how $J_{s.c.}$ and $V_{o.c.}$ vary with time of annealing if the concentration of $CdCl_2$ in methanol is kept constant (10 gm/littre) and annealing temperature kept constant at 450°C. It is evident that there is an

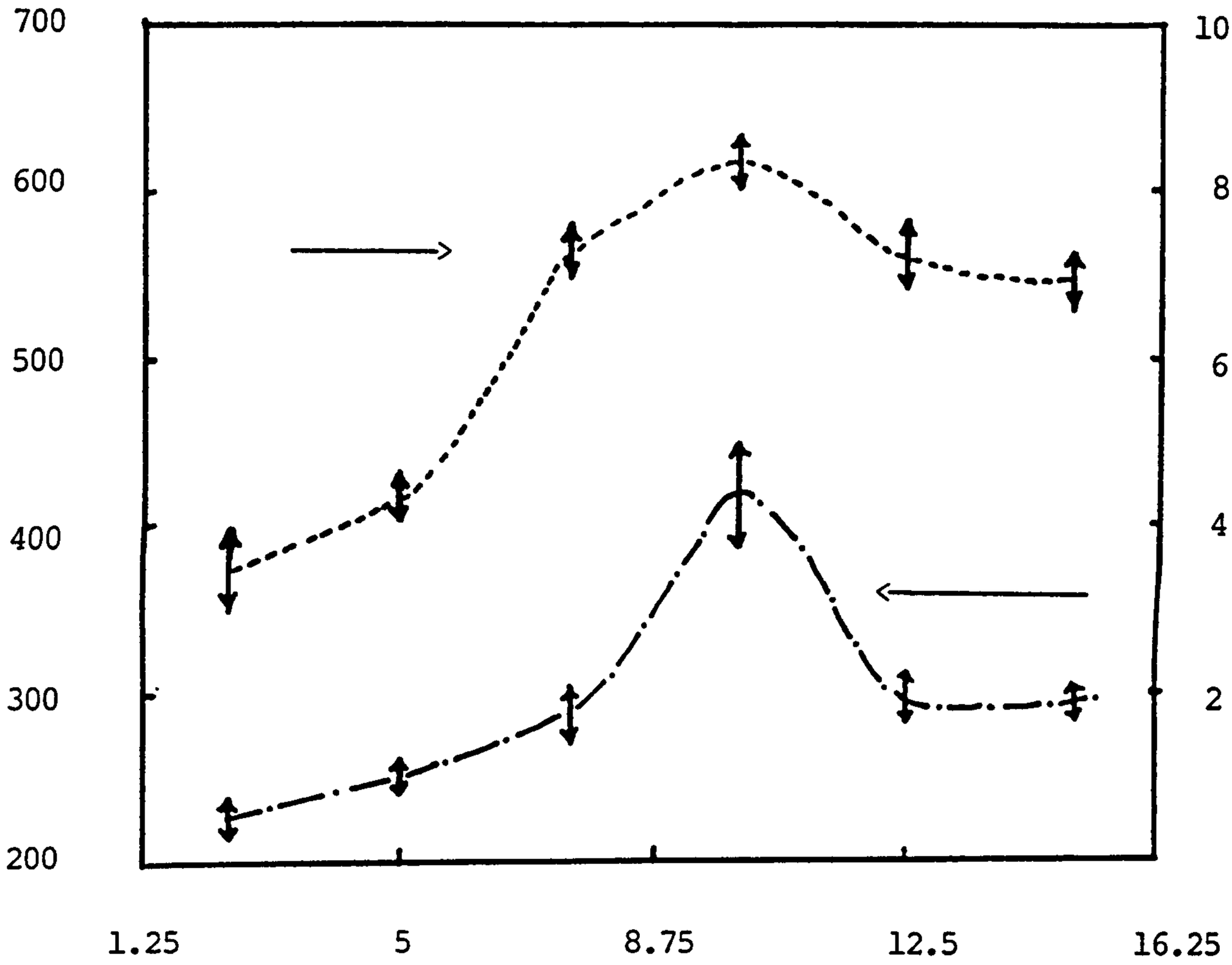


Figure 5.43 The Variation of $V_{o.c}$((a)) and $J_{s.c}$((b)) With the Concentration of $CdCl_2$ in Methanol Used in the Heat Treatment.

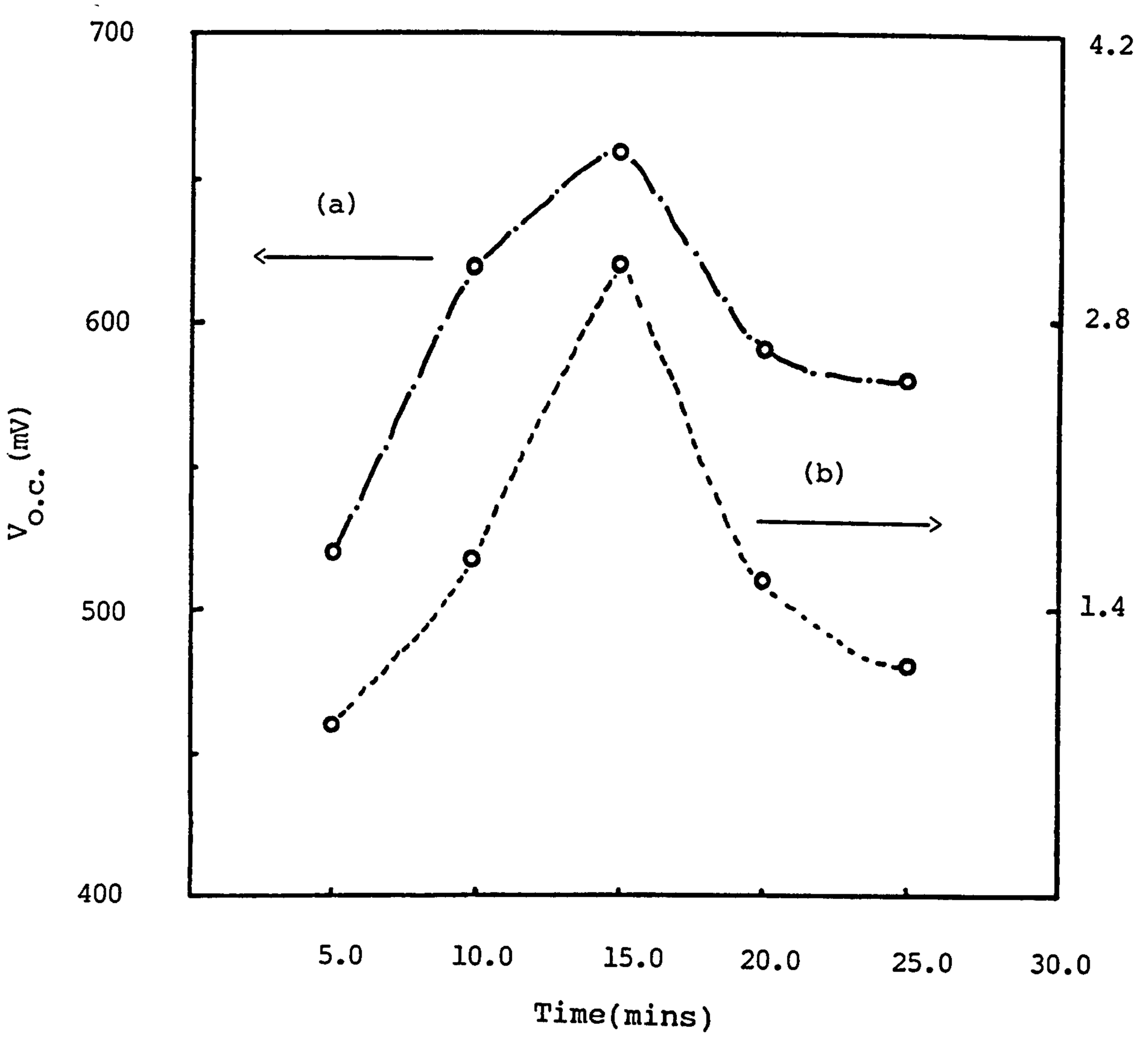


Fig.5.44 The Variation of $V_{o.c.}$((a)) and $J_{s.c.}$((b)) Versus Time of Annealing After the Samples Were Dipped in the $CdCl_2$/Methanol Solution

optimum time of annealing , 15 minutes, to maximise both $V_{o.c.}$ and $J_{s.c.}$.

When the devices were given the $CdCl_2$ heat treatment at 450°C for 15 minutes using 10gm/littre $CdCl_2$ in methanol the variation of $V_{o.c.}$ with the thickness of CdTe used in the device structure was determined as shown in fig.5.45. It was found that $V_{o.c.}$ increased with the thickness of CdTe used up to a CdTe thickness of 1.8μm ; beyond this thickness $V_{o.c.}$ was no longer improved. The increase in $V_{o.c.}$ can be attributed to either an increase in the grain size of the CdTe with increasing CdTe thickness or to the need to spatially separate the depletion region in the CdTe from the back contact. It is also possible that the CdTe needs to be sufficiently thick to minimise the shunting paths arising from the indiffusion of atoms from the back contact material along the grain boundaries in the CdTe.

However with increasing CdTe thickness, the grain size should continue to increase and it is not obvious why $V_{o.c.}$ should "saturate" for CdTe thickness > 1.6μm. Given that the depletion region width in the CdTe is estimated to be 1.6μm (see section 5.14) the isolation of the CdTe depletion region from the back contact is the most plausible explanation of this effect.

A $V_{o.c.}$= 680mV indicated that the CdTe/CdS interface was satisfactory and it was guessed that $J_{s.c.}$ could be

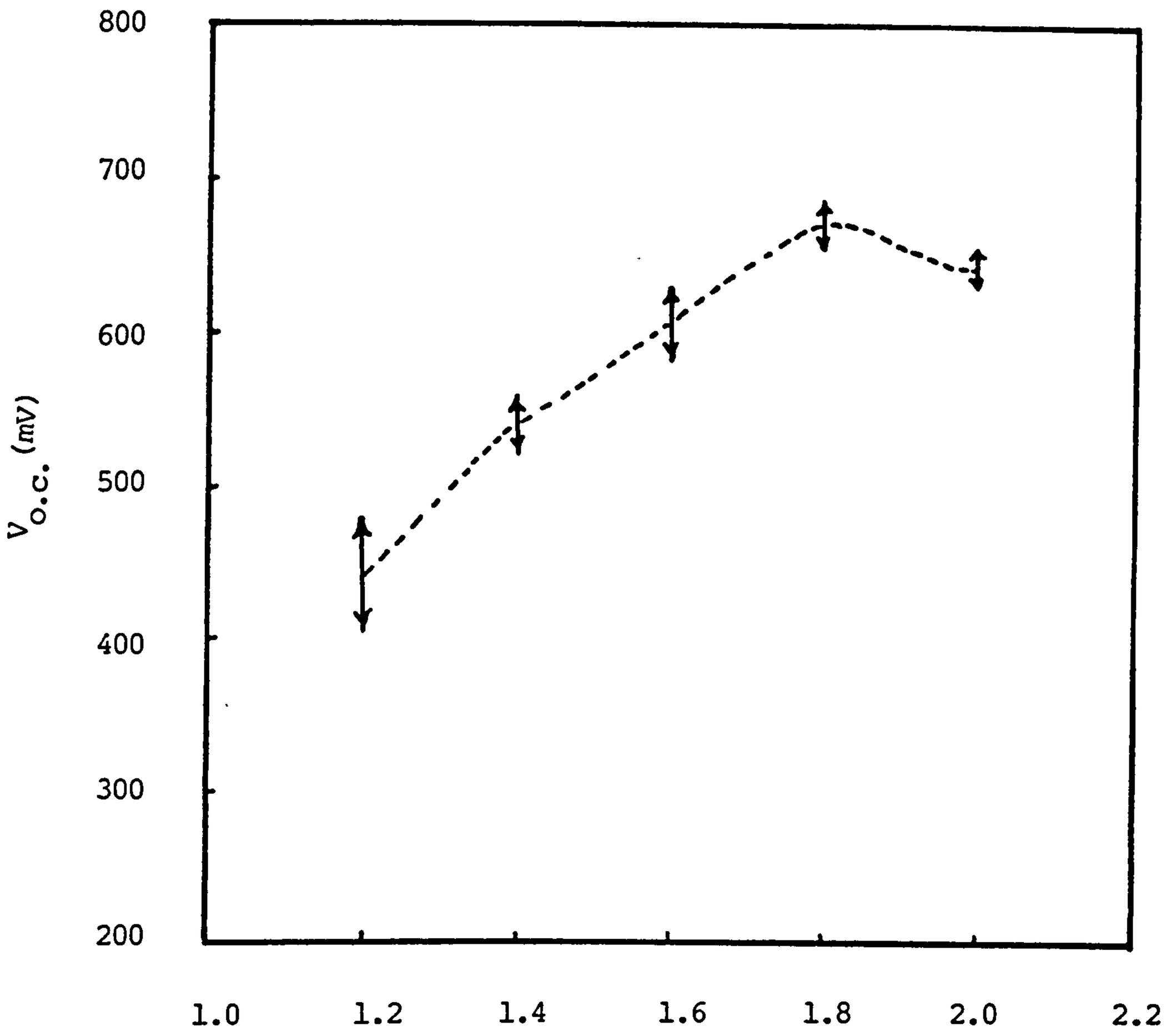


Figure 5.45 The Variation of $V_{o.c.}$ Versus the Thickness of CdTe Used in the Solar Cell Devices.

improved further by reducing the device series resistance.

Chu et al [68,69] reported that they had achieved the highest CdTe efficiency in the world using a similar device structure to that used in this work and further that the best back contact material to use was a copper doped graphite paste. Such a contact was applied to the CdTe after it had been given an etch in a solution of bromine methanol.

Following their approach i.e. dipping the samples into a 0.1 % solution of bromine methanol for 30 secs and then painting a copper doped graphite paste resulted in improvement of $J_{s.c.}$ by reducing the back contact resistance. It was also possible that annealing that back contact resulted in copper diffusing into the CdTe, and hence doping it . The copper may also have a more subtle role in improving the device efficiency by interacting with oxygen and cadmium chloride to some how reduce the concentration and/or effectiveness of recombination centres within the CdTe or at the CdTe/CdS interface [46].

It was found that $J_{s.c.}$ could be improved to $11mA/cm^{-2}$ for $V_{o.c.}$ = 680mV if the back contact was annealed at 450°C for 15 minutes. Annealing at higher temperature or for a longer period of time was found to improve $J_{s.c.}$ further, up to > $15mA/cm^{-2}$ but at the expense of degrading $V_{o.c.}$ to < 500mV. This latter observation is

consistent with what would be expected if copper was diffusing from the graphite paste into the CdTe.

5.13 I-V measurements:

The I-V characteristic under A.M.0. illumination of the most efficient CdS/CdTe solar cell produced in this work is given in fig 5.46.

For this device $V_{o.c.}$ = 680mV, $J_{s.c.}$= 11mA/cm^2, F.F=.35 and the efficiency, n = 2 %. This device was 0.07cm^2 in area.

This solar cell was produced using a CdTe layer 1.8μm thick. This layer was synthesized by annealing a 16 layer stack, in nitrogen at 450 °C for 15 minutes; each Cd layer was 1200 A° thick and each Te layer 1100 A° thick. The device was then dipped in the optimum $CdCl_2$in methanol solution, and annealed in nitrogen at 450 C° for 15 minutes. The CdTe surface was etched for 30 seconds in a 0.1% bromine in methanol solution, the copper doped graphite paste painted onto the surface and the entire device then reannealed at 450°C in nitrogen for 15 minutes.

The shape of the I-V characteristic under illumination is that expected for a device with a rectifying back contact [70,71].

If the slope of the characteristic where it cuts the voltage axis is, $1/R_S$, [72] then the series resistance, R_S, of this device is 40Ω and the shunt resistance, R_{SH},

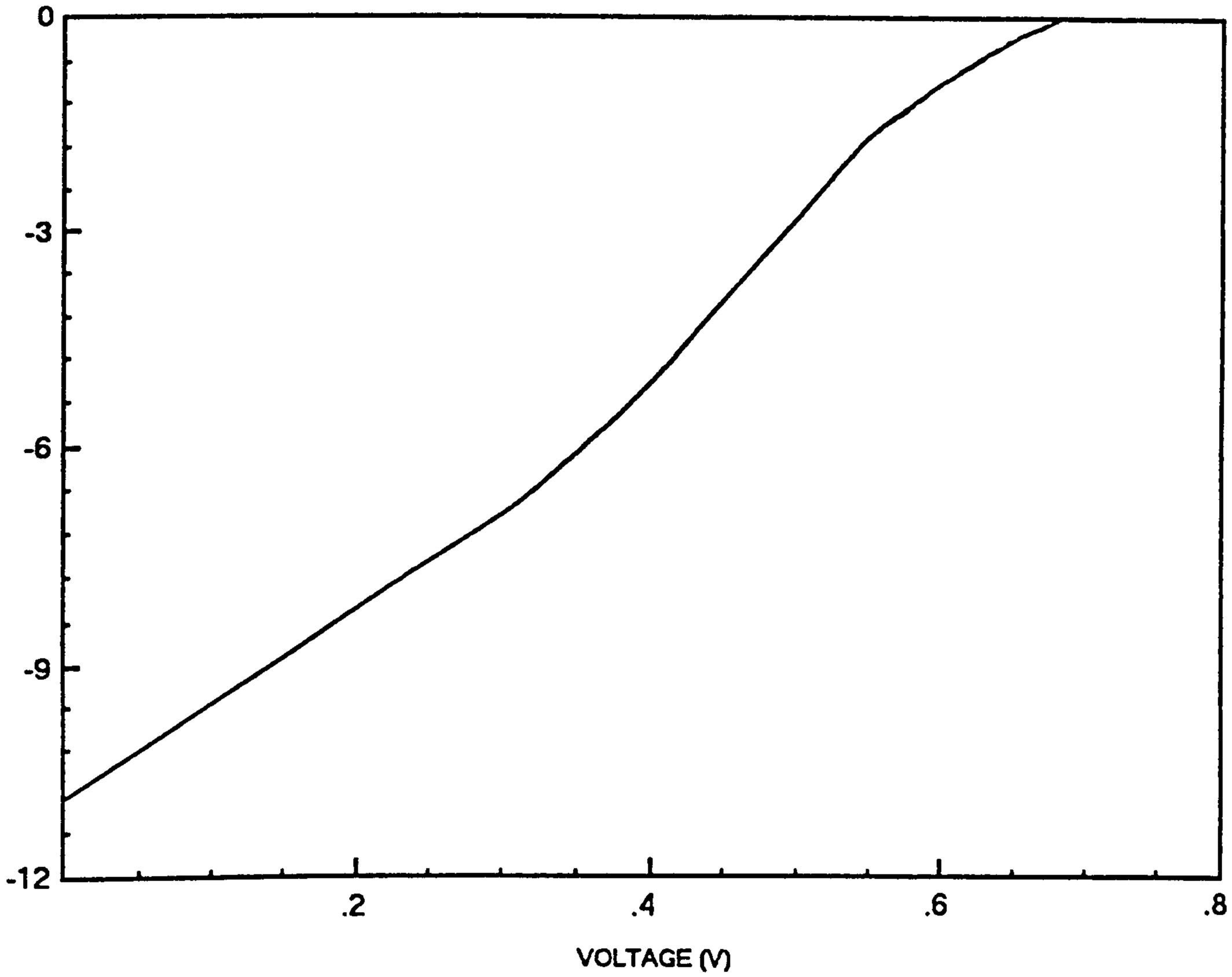


Figure 5.46 I-V characteristics Under Illumination of a CdS/CdTe Solar Cell

is 90Ω, if the slope of the characteritic where it cuts the current axis is $1/R_{SH}$.

The dark current flowing for forward biases < 0.4 Volts was found to be too small to measure because of the high series resistance. To obtain further information about the device the I-V characteristic was measured under different intensities of illumination and the following formula was used [73,74] :-

$$V_{o.c.} = (AkT/q)\ln(J_{s.c.}/J_0) \qquad 5.7$$

This formula is derived by considering the point of the illuminated I-V characteristic where J=0 ($V = V_{o.c.}$) and hence the drop voltage across the series resistance is zero.

A plot of $\ln(J_{s.c.})$ versus $V_{o.c.}$ for the device is given in fig.5.47. The slope gives a value for A = 0.6 and the intercept a value for $J_0 = 8*10^{-9}$ Acm^{-2}. It should be noted that such a low value for A was obtained with this one device; for all the other devices studied A was in the range 1.2 - 2.0. A value of ideality factor , A < 1 is possible if the back contact is rectifying in which case the ideality factor measured will be the difference of the ideality factors of the CdS/CdTe junction and the contact junction [71].

The value of J_0 obtained was obtained in the other devices fabricated; it was typically in the range 10^{-8}-10^{-9} Acm^{-2}.

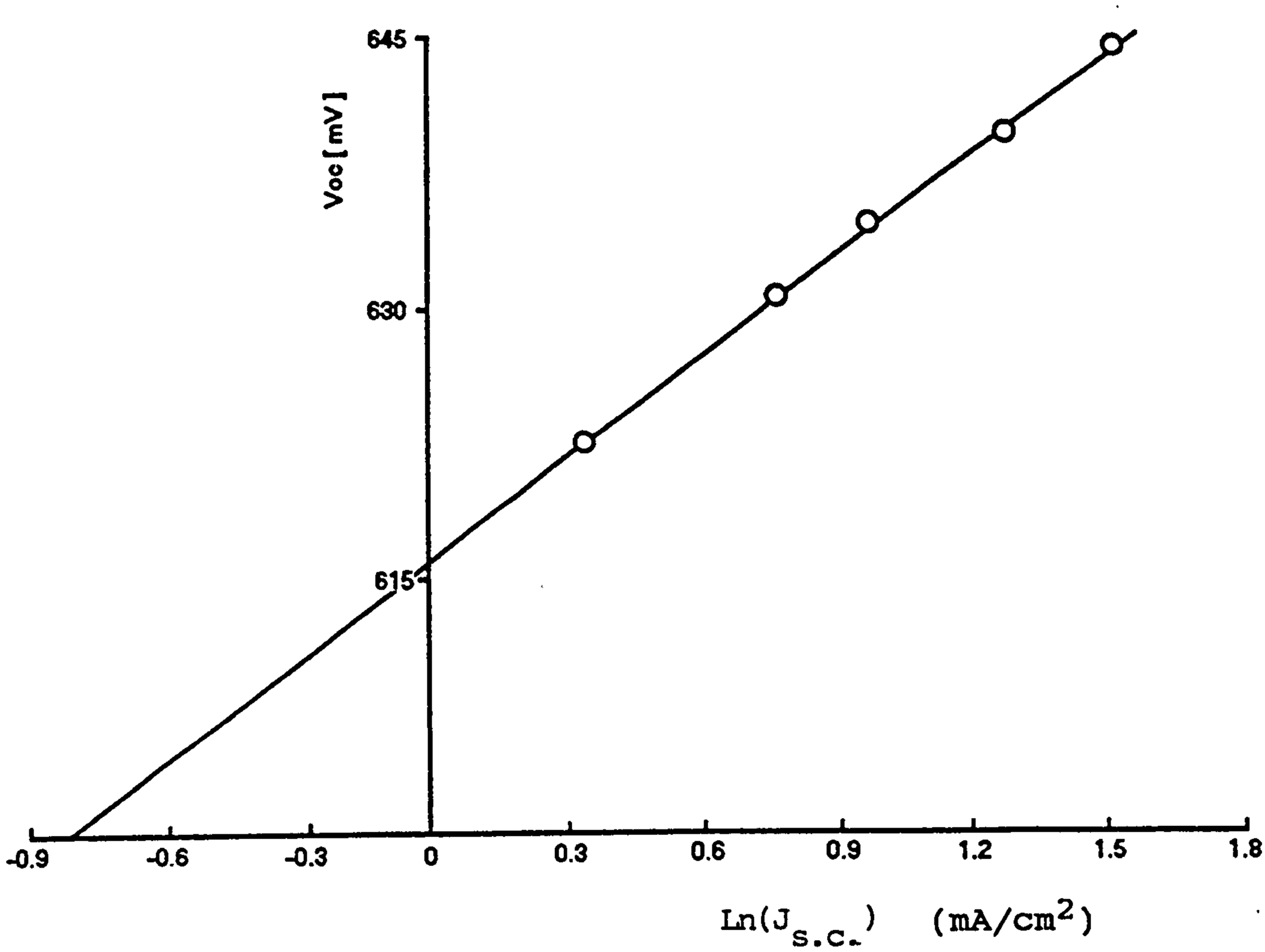


Figure 5.47 A Plot of $V_{o.c.}$ Versus $\ln(J_{s.c.})$.

Fig.5.48. shows that the variation of $\ln(J_{s.c.})$ versus $V_{o.c.}$ obtained in the more typical devices.
The temperature variation of the plots is also given in figs.5.49. show how the values of J_0 and A derived from these plots vary with temperature. As shown in fig.5.50 the ideality factor, A, decreases with an increase in temperature . This behaviour is consistent with that observed in the CdS/CdTe solar cells produced using other techniques [58,75,76]. If the forward current is given by [77] :-

$$J = J_o\exp(qV/AkT) = J_{oo}\exp(-\varphi/kT)\exp(qV/AkT) \qquad 5.8$$

then a plot of $\ln(J_0)$ versus 1/T should be a straight line and the slope will yield the activation energy,φ.
As observed in fig.5.51 such a plot is indeed a straight line and φ=0.66eV for the device shown for T > 333K°. The behaviour is in fact very similar to that observed in the CdS/CdTe solar cells produced using electrodeposition [58], C.S.S.[78], and using Single Crystal CdTe [79]. The change in the slope of the $\ln J_0$ versus 1/T plot for $10^3/T$ > 3(i.e. T<333k°) is also observed in other devices and the observed dependence of J_0 on T has led to the suggestion that tunnelling is dominating the current transport for T < 340k°[61].
An alternate way to determine, φ, is shown in fig.5.52. For $V=V_{o.c.}$, J=0 and the equation may be rearranged to :-

$$V_{o.c.} = A\varphi-(AkT/q)\ln[J_L/J_{oo}] \qquad 5.9$$

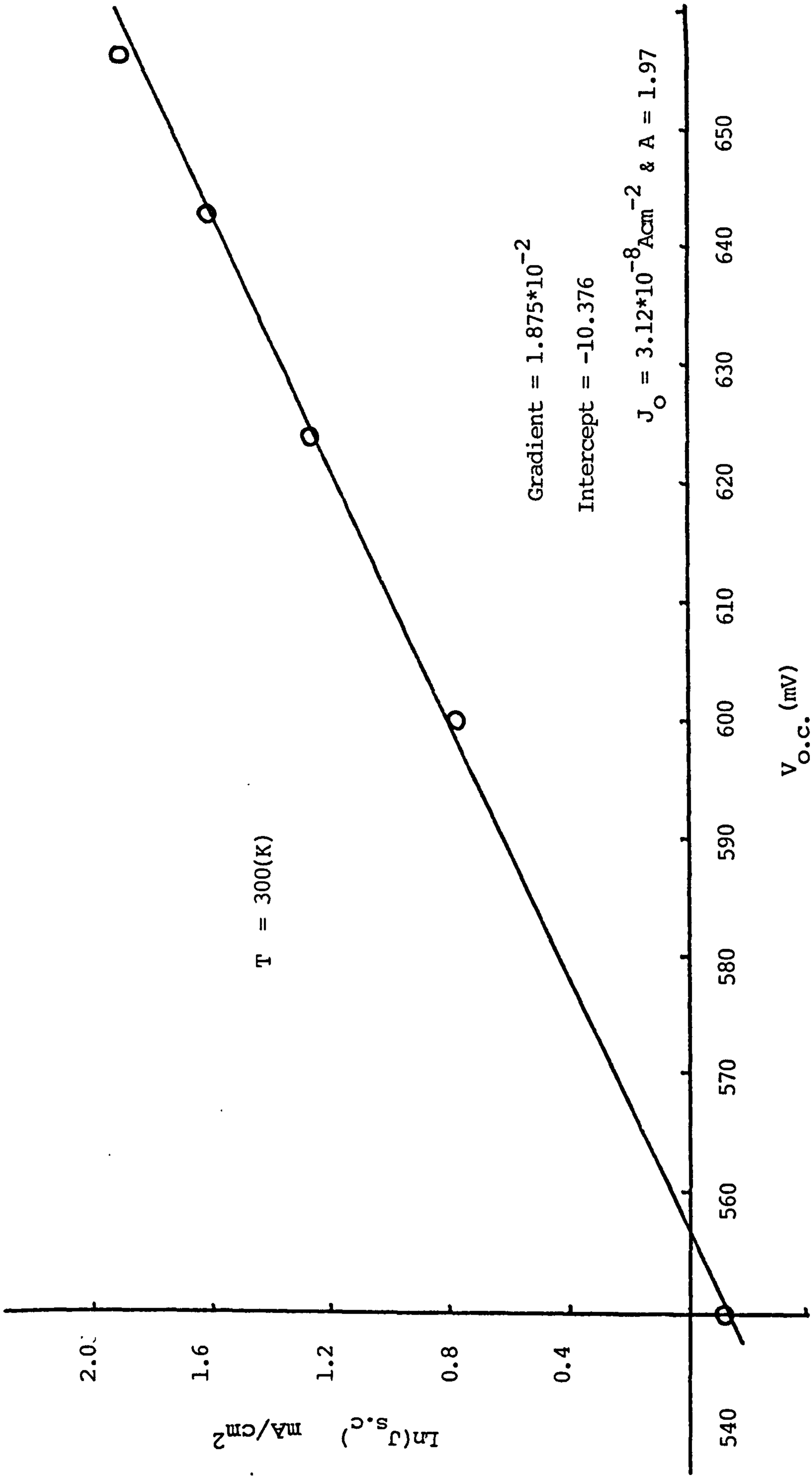


Figure 5.48 Ln $J_{s.c.}$ Versus $V_{o.c.}$ Under Different Illuminations of CdTe Solar Cell.

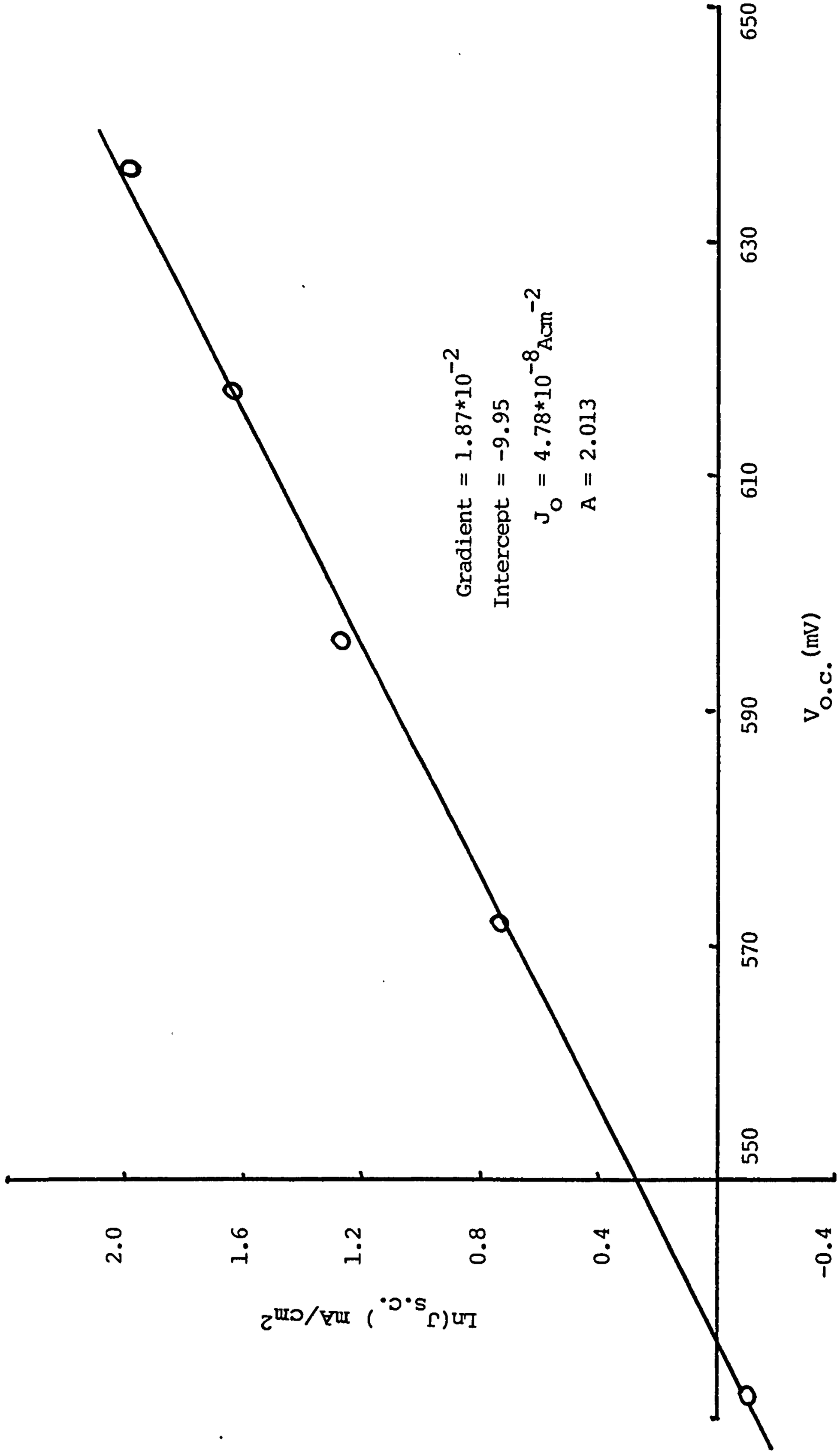


Figure 5.49 (a) Ln ($J_{s.c.}$) Versus $V_{o.c.}$ at 313(K)

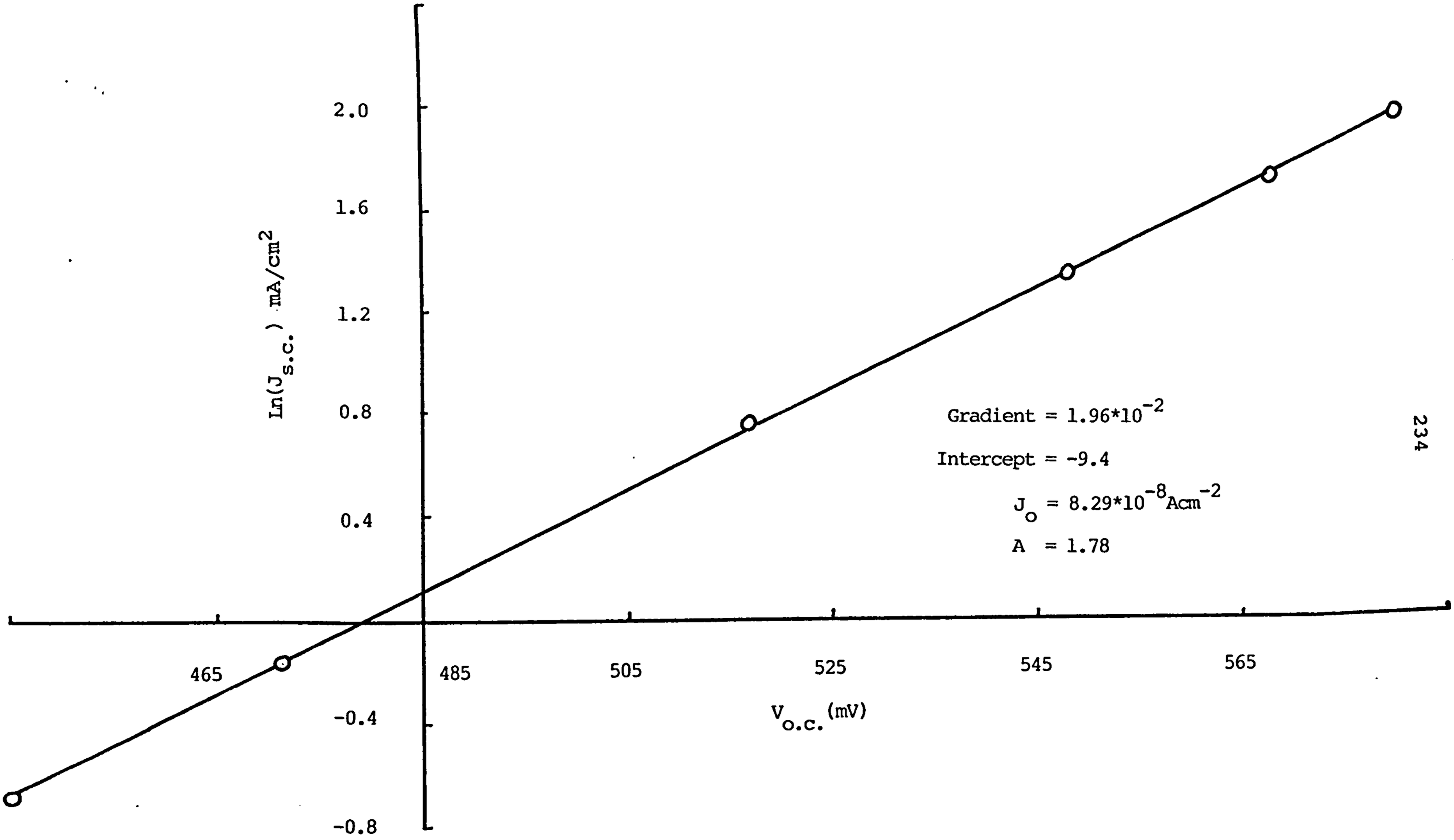


Figure 5.49(b) $Ln(J_{s.c})$ Versus $V_{o.c.}$ at 333(K).

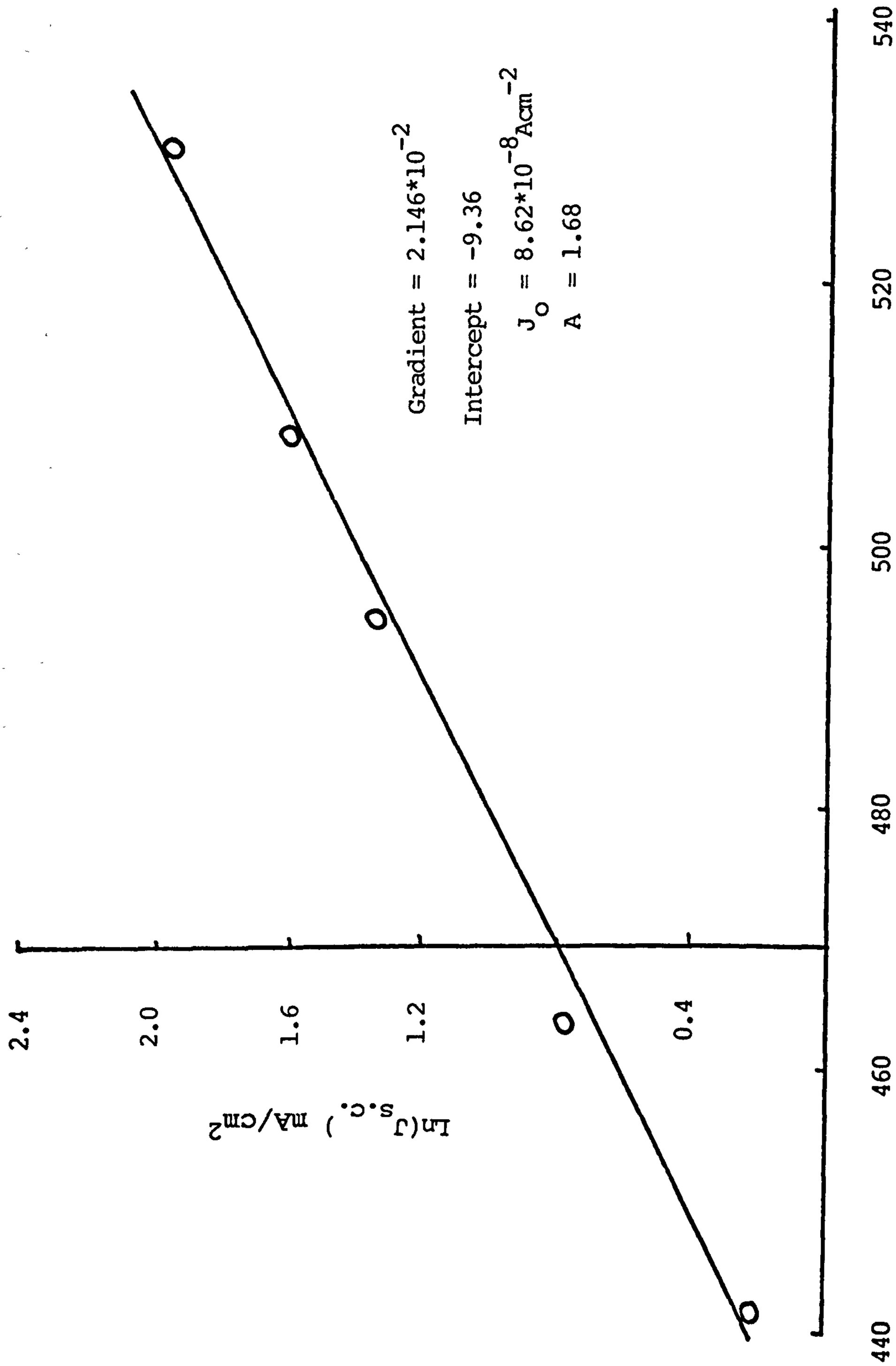


Figure 5.49(c) $Ln(J_{s.c.})$ Versus $V_{o.c.}$ at 353(K)

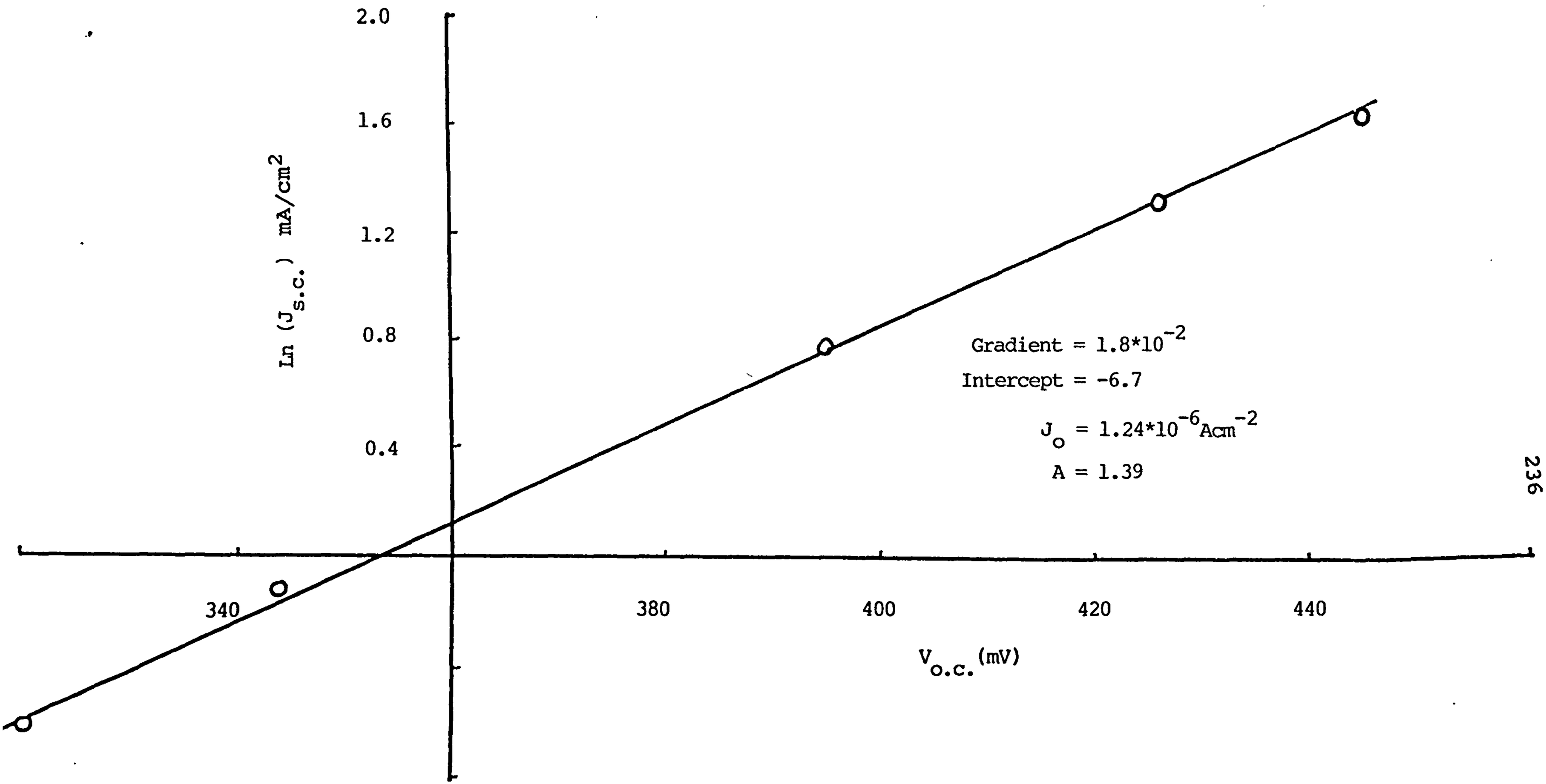


Figure 5.49(d) Ln($J_{s.c.}$) Versus $V_{o.c.}$ at 373(K)

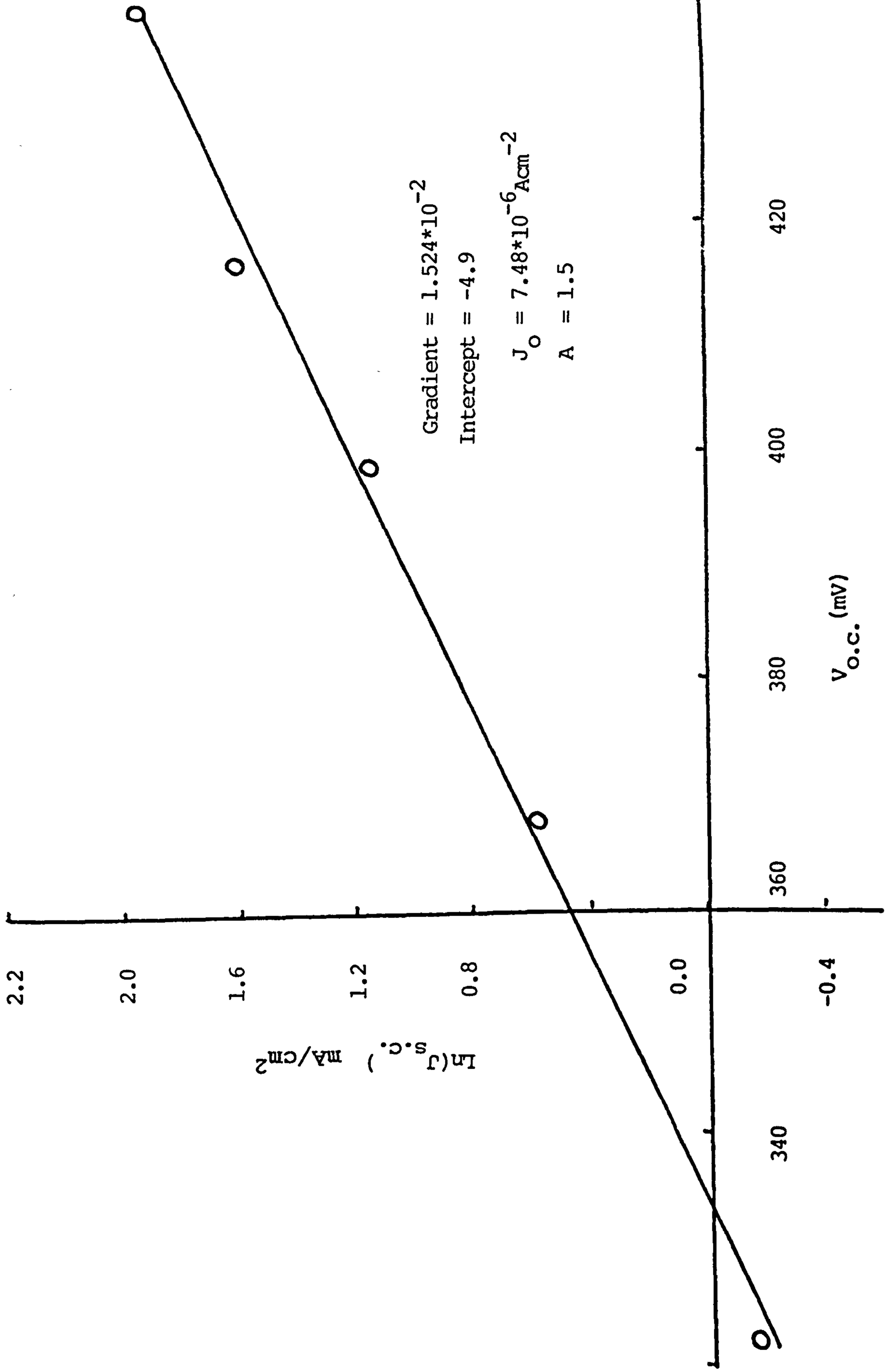


Figure 5.49(e) Ln($J_{s.c.}$) Versus $V_{o.c.}$ at 393(K).

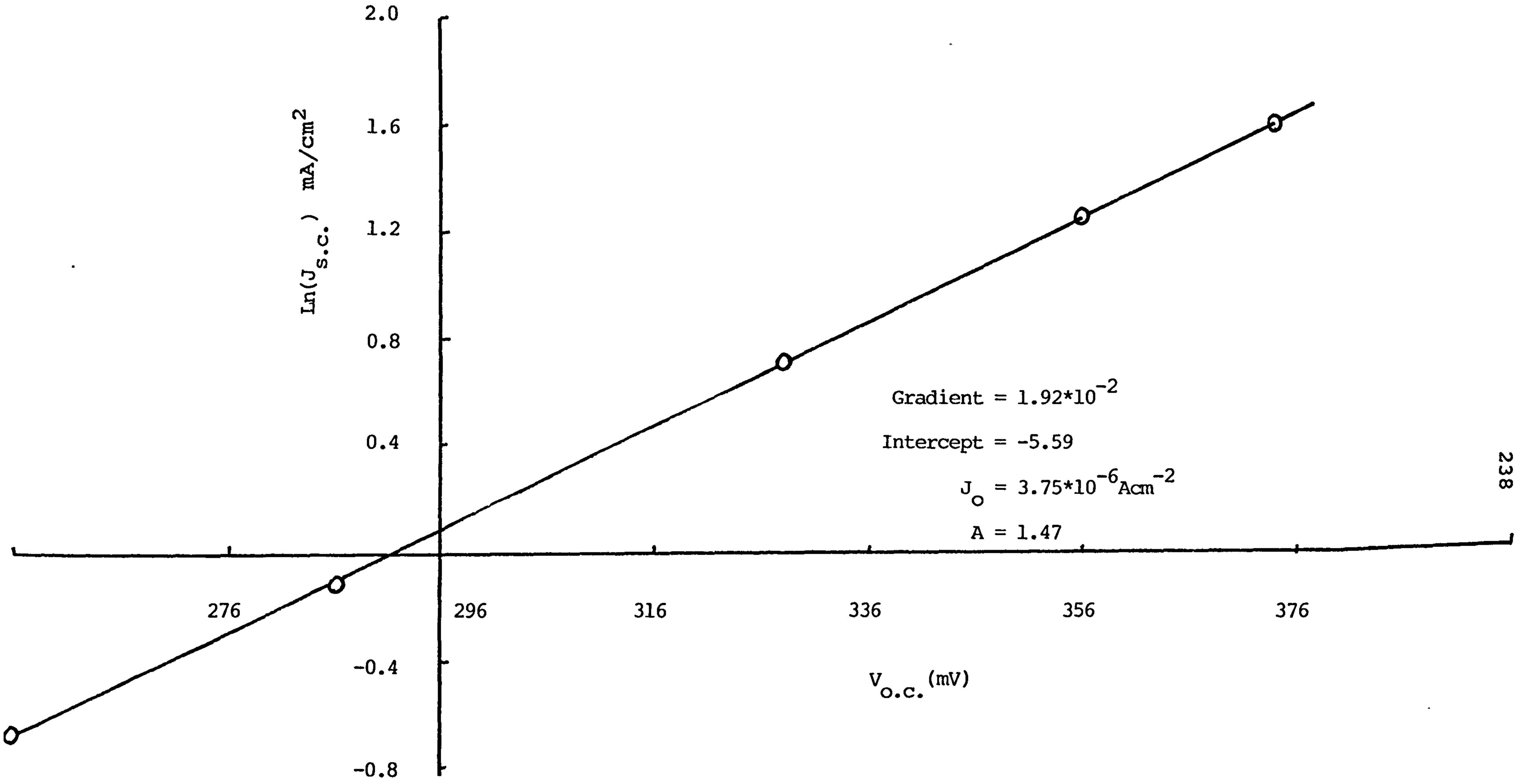


Figure 5.49(f) Ln($J_{s.c.}$) Versus $V_{o.c.}$ at 413(K)

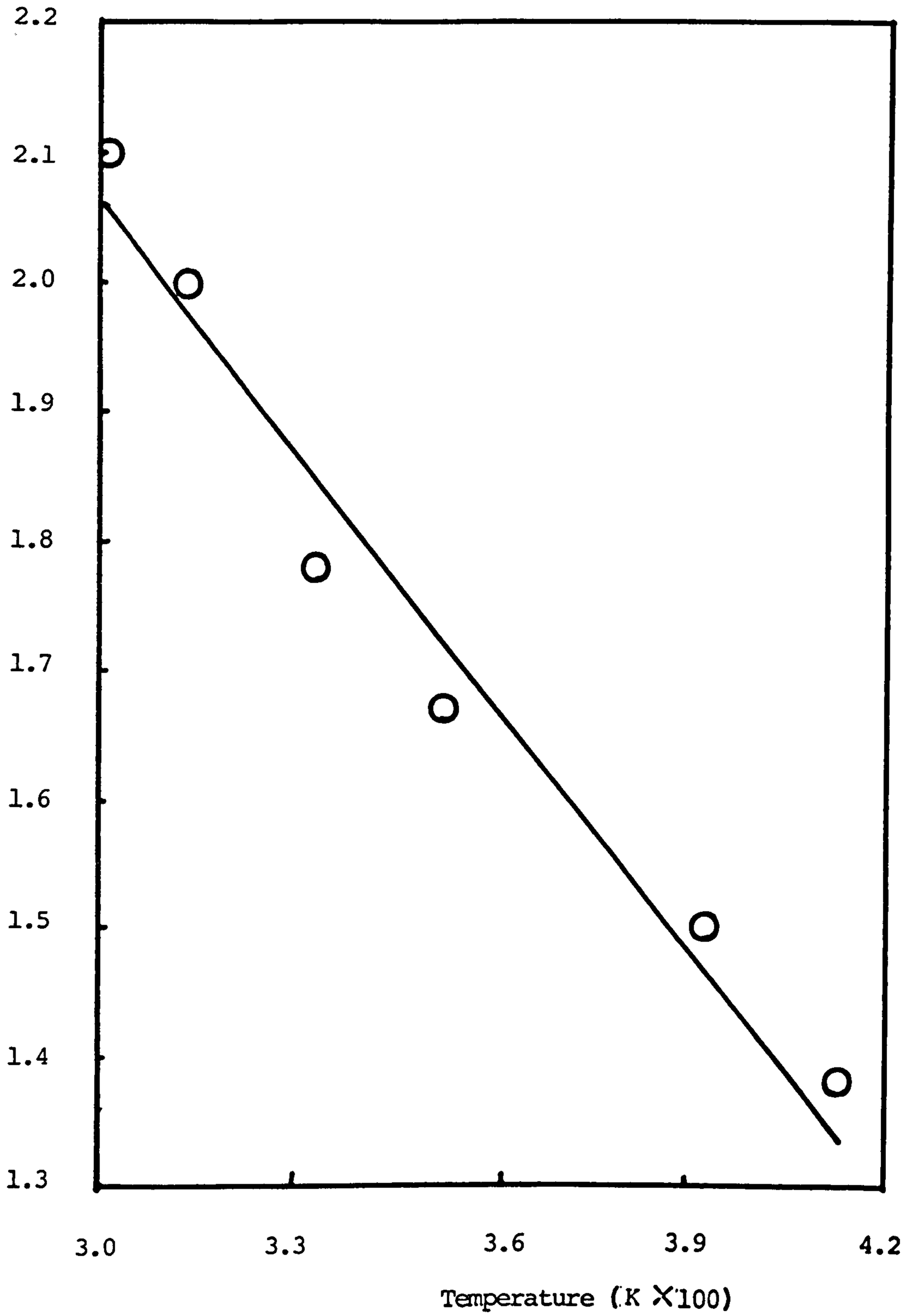


Figure 5.50 Variation of Ideality Factor Versus Temperature for a CdS/CdTe Solar Cell.

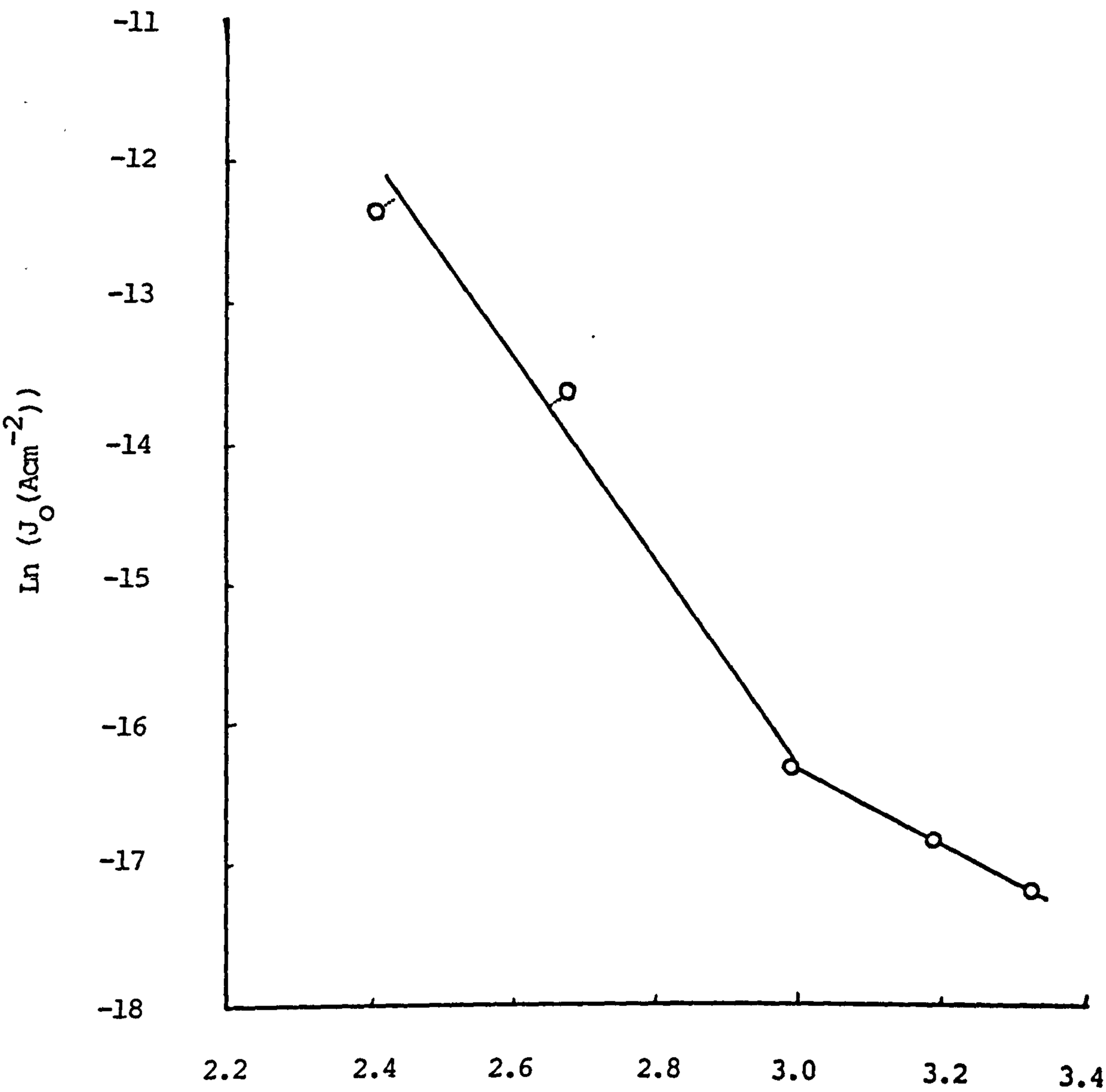


Figure 5.51 Variation of J_o Versus $10^3/T$ for a CdS/CdTe Solar Cell.

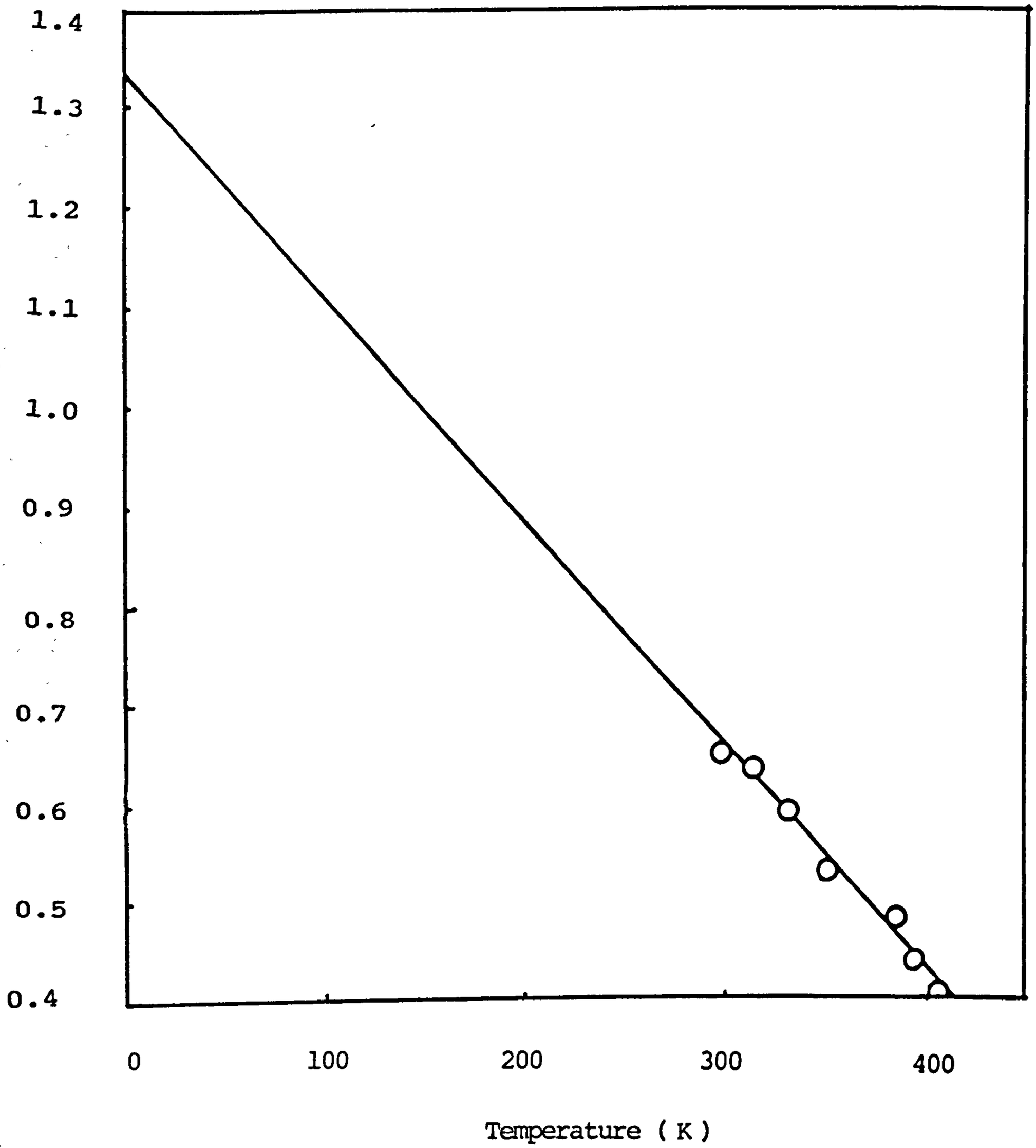


Figure 5.52 Variation of $V_{o.c.}$ Versus Temperature for CdS/CdTe Solar Cell

Hence a plot of $V_{o.c.}$ versus T will be a straight line with an intercept, for T=0, equal to $A\varphi$. From the graph, $A\varphi$ = 1.35eV and because A = 2.0 then φ = 0.67eV.

Table 5.2 gives the value of J_0, φ, A and J_{00} (obtained from the plots of $\ln(J_0)$ versus 1/T) obtained in this work and those quoted in the literature.

The values obtained in this work are hence comparable to those observed in the CdS/CdTe solar cells produced using other techniques [80,81].

The current transport model considered by most workers to be dominant for T > 300°C, (where the barrier height is ≈ 0.5 - 0.7eV) is the tunnelling recombination model of Donnelly and Milnes [82]. If this model is applicable then the forward current, J should be given by :-

$$J = qS_iN_B\exp(-\varphi/kT)\exp(qV/AkT) \qquad 5.10$$

where the interface recombination velocity, S_i, is given by :-

$$S_i = N_i\delta_iV_{th} \qquad 5.11$$

N_i is the density of interface states, δ_i there capture cross-section and v_{th} is the "thermal velocity".

The value of J_{oo} is determined to be ≈ 800 Acm^{-2}. Taking N_B ≈ $10^{16}cm^{-3}$ then S_i ≈ $5*10^5$ cms^{-1} which corresponds well with the value determined by Loferski [77] for the CdS/CdTe solar cells he studied which were produced using the Bridgman method.

TABLE 5.2

Sr. No	Method of Deposition	J_o(mA/cm^2)	J_{oo}(mA/cm^2)	ø(eV)	Idea. Fact(A)	Ref.
1	Vacuum Deposition	$3*10^{-9}$	------	0.67	1.89	55
2	Close Space Vapor Transport (CSVT)	$8*10^{-8}$	-------	0.59	----	55
3	Electrodeposition	10^{-10}	-------	0.67 0.58	1.5	58
4	Electrodeposition	10^{-8}	-------	0.52 0.71	1.88	61
5	Close Space Vapor Transport (CSVT)	10^{-9}	-------	0.72	1.6-1.7	45
6	Vacuum Evaporation	-----	10^7mA/cm^2	0.65	1.7-1.9	
7	Close-Spaced Sublimation (CSS)	$5.4*10^{-10}$	-------	----	1.78	60
8	Screen Printing (SP)	$1.79*10^{-10}$	-------	----	1.83	45

If $V_{th} \approx 1.2*10^{7}cms^{-1}$ then $N_i\delta_i \approx 0.04$. N_i may be estimated using the formula used by Donnelly and Milnes [82] :-

$$N_i = \blacktriangle a/a^3 \qquad 5.12$$

where a is the average lattice constant in the plane of the junction and ▲a the difference of the lattice constants of the CdTe and CdS.

In this work, $a_{CdS} = 6.7A^{\circ}$ and $a_{CdTe} = 6.452A^{\circ}$ for sphalerite structure CdTe and $a_{CdTe} = 7.5\ A^{\circ}$ for wurtzite structure CdTe (as determined from the X-ray diffraction data).

For sphalerite CdTe/CdS devices, $N_i \approx 7*10^{12}cm^{-2}$ and for wurzite CdTe/CdS devices, $N_i \approx 2.2*10^{13}cm^{-2}$.

Using the values and $N_i\sigma_i \approx 0.04$ results in a capture cross-section, $\sigma_i \approx 6*10^{-15}cm^2$ for sphlerite CdTe/CdS devices and $\sigma_i = 2*10^{-15}cm^{-2}$ for hexagonal devices.

It should noted that the D.L.T.S. (deep level transient spectrscopy) studies of the CdS/CdTe solar cells produced using the MBE [83] have indicated the presence of deep acceptor states at Ev + 0.64 eV and that this level is attributed to cadmium vacancies or cadmium-vacancies-chlorine complexes introduced during the $CdCl_2$ anneal. A trap density of $8.8*10^{13}\ cm^{-3}$ with a capture cross-section $\approx 8.2*10^{-16}cm^2$ were determined in this study. Depletion layer recombination is considered to occur via this E_v + 0.64 eV level.

It is possible to estimate trap density in this work using the formula :-

$$N_t \approx 1/(\sigma_n \Gamma_n V_{th}) \qquad 5.13$$

where Γ_n is the minority carrier lifetime which is expected to be 10^{-9}s in p-type, polycrystalline CdTe [84].

For sphalrite CdTe/CdS devices, taking $\sigma_i \approx 6*10^{-15}cm^2$, $V_{th} \approx 1.2*10^7$ cms^{-1} then $N_t \approx 1.4*10^{16}$ cm^{-3} if $\Gamma_n \approx 10^{-9}$ s.

For hexagonal structure CdTe/CdS devices, taking $\sigma_i = 1.8*10^{-15}cm^2$ and $V_{th} \approx 1.2*10^7$ cms^{-1} then $N_t \approx 4.6*10^{16}cm^{-3}$ for $\Gamma_n \approx 10^{-9}$s.

These values of N_t are similar to those determined by Collins and Mc Gill [85] in their CdS/CdTe devices produced using single crystal CdTe. They report N_t is in the range 10^{15}-$10^{16}cm^{-3}$ and $\sigma_i \approx 5*10^{-14}cm^2$.

5.14 Capacitance-Voltage Measurements

The capacitance of the solar cells produced was measured for different biases applied across the device and for different measurement frequencies. Plots of C^{-2} versus V using different measurement frequencies are given in fig.5.53 for a typical device.

The device capacitance is observed to decrease with increasing frequency. If the difference between the capacitance measured at high frequencies and that measured at low frequencies is assumed due to charged interface states being unable to respond to the high

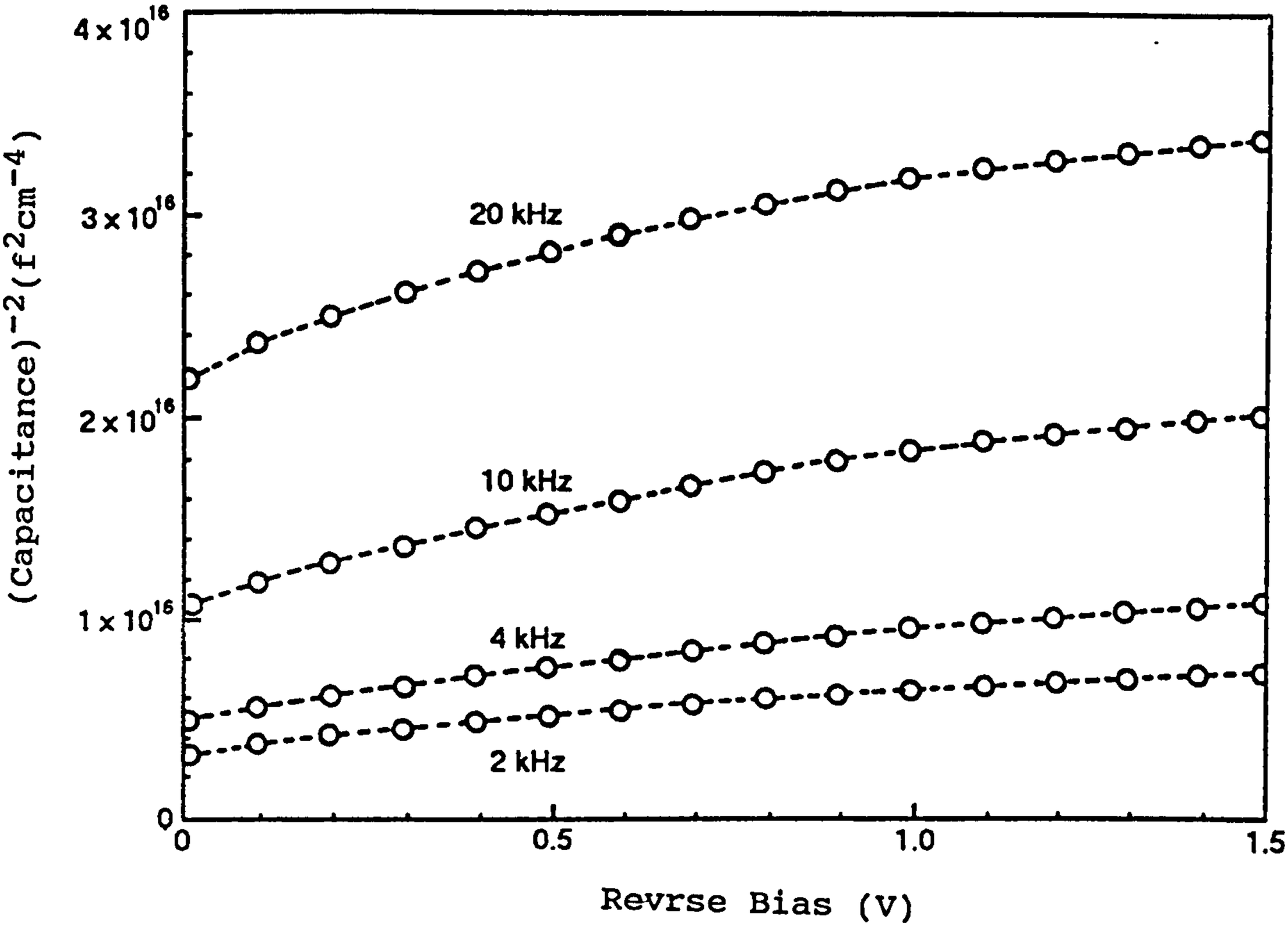


Figure 5.53 Variation of Capacitance Versus Reverse Bias Voltage for a CdS/CdTe Solar Cell

frequencies signals then the interface states density, N_i , is given by [86] :-

$$N_i=(C_{LF} - C_{HF})/q \qquad 5.14$$

where C_{LF} and C_{HF} are the lower and higher frequencies respectively.

"The variation of N_i" with applied bias is given in fig.5.54 and the behaviour is similar to that observed by [58].

For zero applied bias , the interface states, $N_I \approx 8.2*10^9$ $cm^{-2}eV^{-1}$ which is one order of magnitude smaller than the value obtained by Das, $6.4*10^{10}$ $cm^{-2}eV^{-1}$, with electrodeposited CdS/CdTe solar cells [58].

The plots of C^{-2} versus reverse bias voltage, V, are not straight lines implying that the doping of the CdTe is not uniform throughout its thickness. If the devices are assumed to be n^+-p then the doping concentration is proportional to $1/d(C^{-2})/dV$ and the plots indicate that the doping is lowest nearest to the CdS/CdTe interface and increases towards the back contact. At the interface if $d(C^{-2})/dV = 7.5*10^{15}$-$3.0*10^{15}$ then $N_A \approx 10^{15}$-10^{16} cm^{-3} for all the different measurement frequencies used. The data taken at the highest frequencies where the effect of the charged interface states are minimised will more accurately reflect the value of N_A; for f=20kHz, the highest measured frequency used, $N_A=9.8*10^{15}$ cm^{-3}. Fig.5.55 shows how N_A varies with distance from the CdS/CdTe interface, taking the data from the variation of C with V at f=20kHz. Such non uniform doping could arise

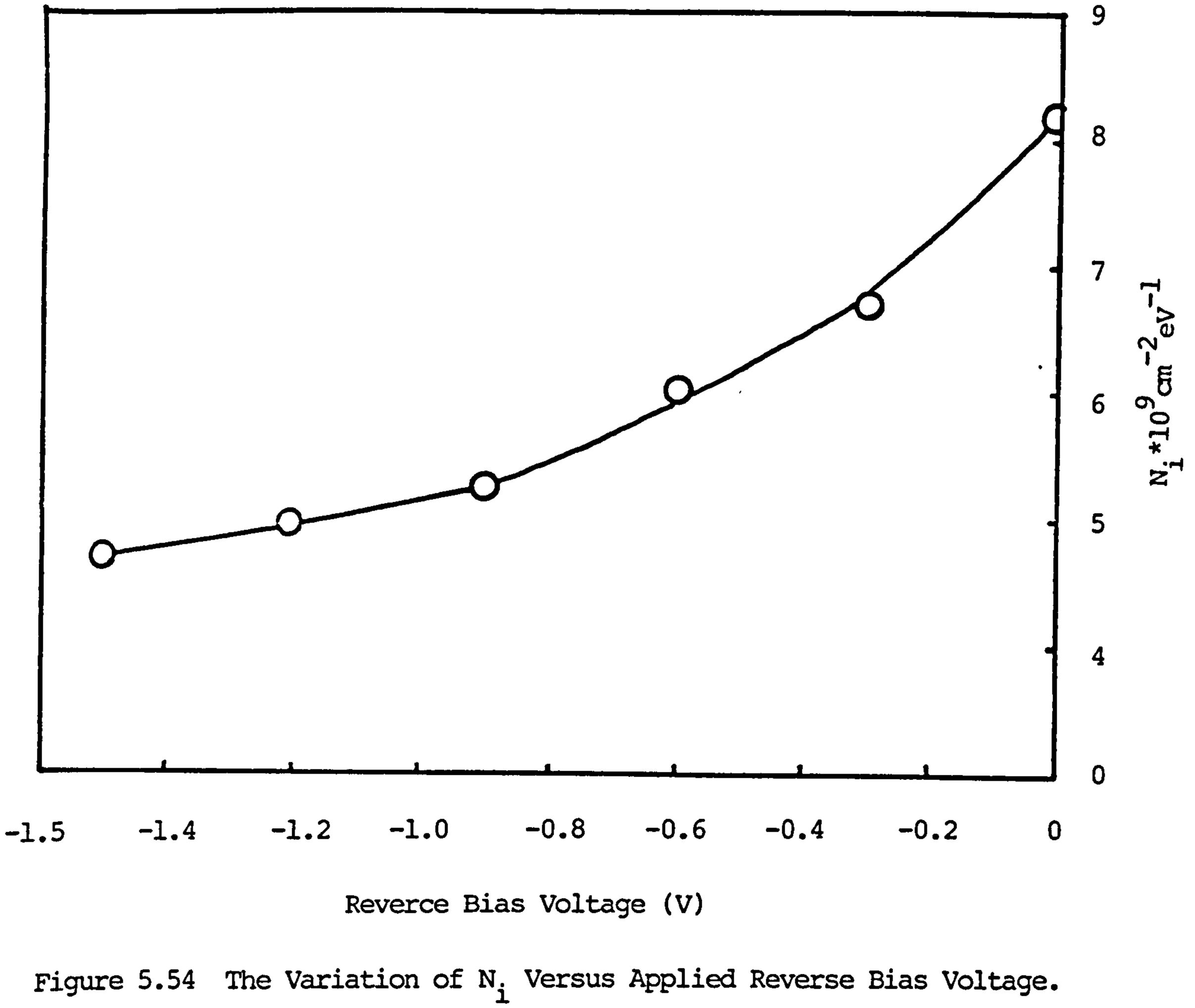


Figure 5.54 The Variation of N_i Versus Applied Reverse Bias Voltage.

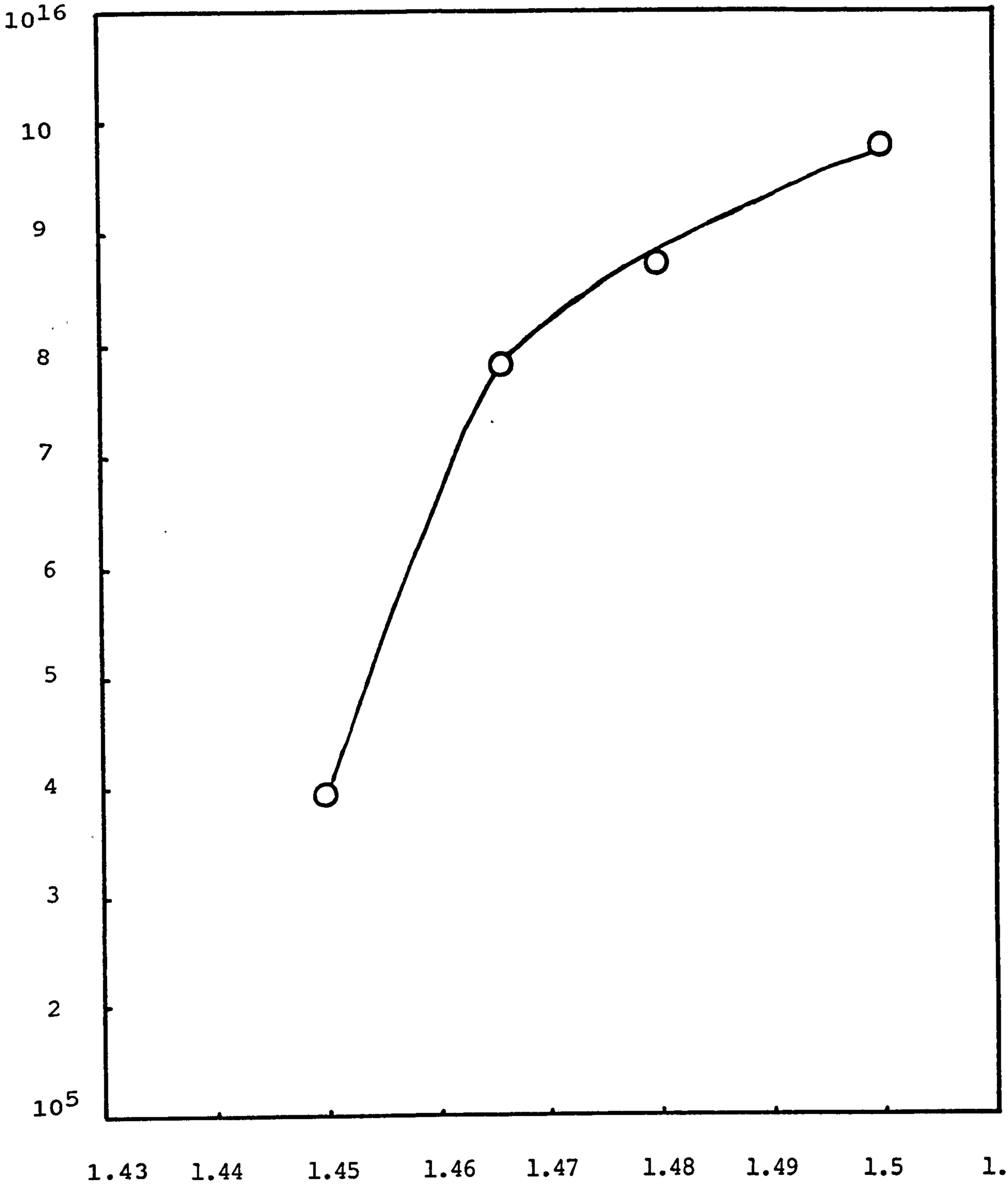


Figure 5.55 The Variation of Carrier Concentration Verces Distance From the Interface.

if copper is diffusing into the CdTe from the copper doped graphite paste back contact and playing the role in doping the CdTe p-type. Alternatively the $CdCl_2$ heat treatment in the presence of oxygen may more strongly dope the outer region of CdTe than the CdTe near to the CdS layer.

If the tangents to the C^{-2} versus V plots; for V=0, are extrapolated to cut the voltage axis then the deduced contact potential, V_{Di} is ≈1.35volts, 2.53volts, 2.7volts and 2.925volts for measurements frequencies of 2kHz, 4kHz, 10kHz and 20kHz respectively. The measured diffusion voltage thus depends on measurement frequency i.e. on charged interface states. The measured contact potential for f=20kHz is also much larger than the maximum built-in voltage, V_D=1.12volts, predicted by Anderson model - see section 5.16.

The expression given by Donnelly and Milnes [82] for the $C^{-2} = 0$ intercept, V_{Di}, takes into account these observations:

$$V_{Di} = V_D - \varphi_m - \beta Q_{IS}^2 \qquad 5.15$$

V_D is the theoretically calculated diffusion voltage, Q_{IS} the charge on the interface states and φ_m the " electric dipole " at the interface. Irrespective of whether the interface states are positively or negatively charged, Q_{IS}^2 is positive and therefore the presence of charged interface states will reduce the value of V_{Di}.

V_{Di} should therefore be larger at the higher frequencies of measurement where the interface states are assumed

smaller role. This is consistent with what is observed in fig.5.53

The observation that $V_{Di} > V_D$ at higher frequencies may be explained by assuming that the electric dipole, φ_m, is negative [84].

Alternatively it is possible that there is an intrinsic layer inside the depletion region [87], in which case the width of the intrinsic layer may be calculated :-

$$C^{-2} = 2(V_{Di}-V)/q\epsilon N_A + (w_i/\epsilon)^2 \qquad 5.16$$

Taking V_{Di}=2.925, N_A=2.94*$10^{15}cm^{-3}$, ϵ=9.6$\epsilon\cdot$ then w≈1.5 μm which is possible as it is less than the thickness of CdTe used (which for this device was 2μm).

5.15 Spectral Response Measurements.

The spectral response of a typical CdS/CdTe solar cell is given in fig.5.56 It is evident that the "heterojunction window effect" is observed i.e. the response occurs for wavelengths within the range defined by the energy bandgaps of the CdS and CdTe. This behaviour is consistent with the fact that photons with energies greater than the energy bandgap of the CdS are absorbed at the front surface of the CdS where they recombine without contributing to the photocurrent. Thus no response is observed for $\lambda < \lambda_{CdS}$ where $\lambda_{CdS}=hc/E_Gq$=520nm. Photons with energies less than the energy bandgap of the CdS are transmitted through the CdS and those with energies greater than the energy bandgap

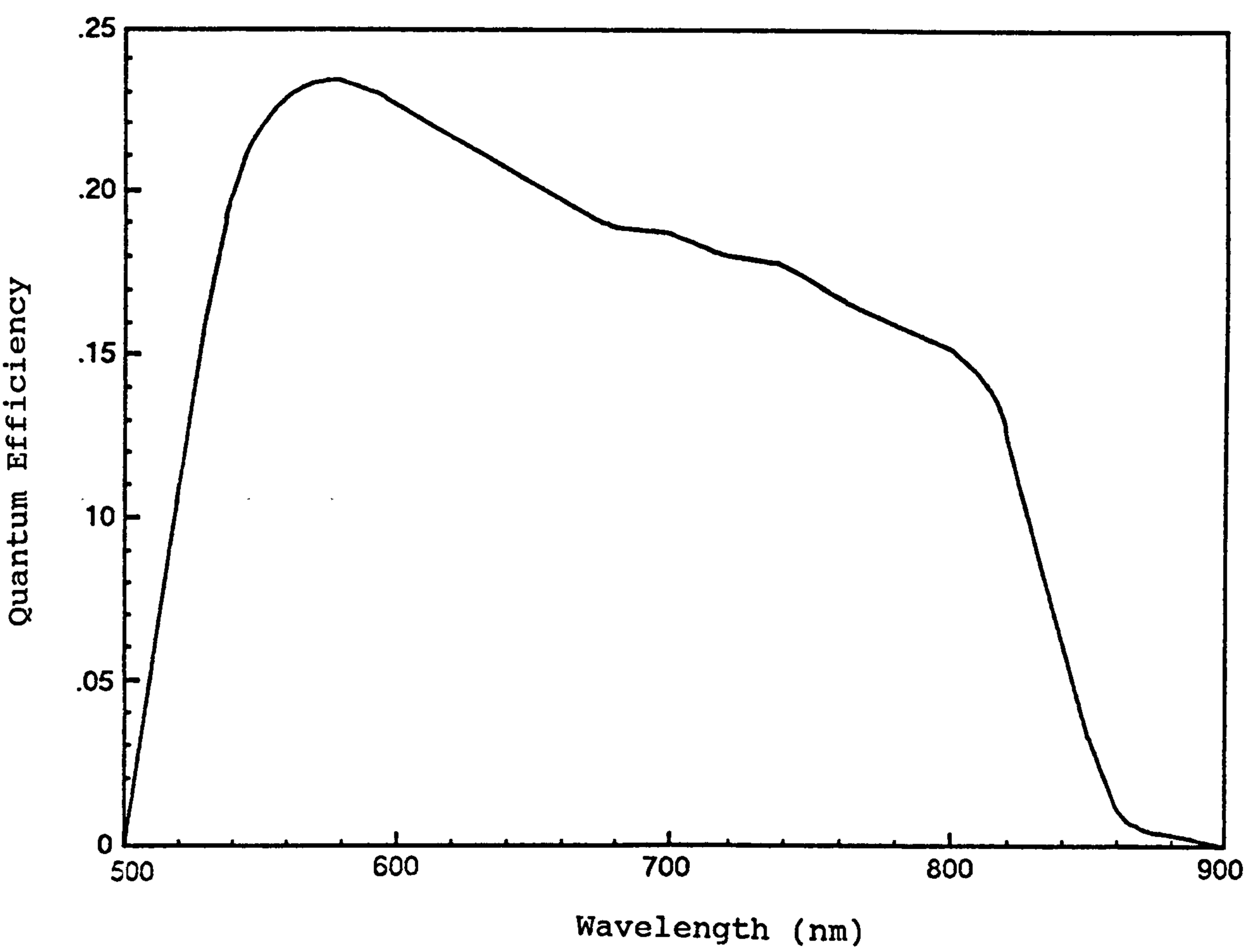


Figure 5.56 Spectral Response Measurement of a CdS/CdTe Solar Cell.

of the CdTe are absorbed within the CdTe near the interface where they contribute the photocurrent. Photons with energies less than the energy bandgap of CdTe will not be absorbed and there should therefore be no response for $\lambda > \lambda_{CdTe}$ where $\lambda_{CdTe} = hc/E_Gq = 815nm$.

If $CdS_{1-x}Te_x$ was found at the CdS/CdTe interface then the long wavelength fall off would be expected to be > 815nm, typically ≈ 850nm [41,44,45,88]. Such an extension of the long wavelength fall-off was not observed in any of the devices produced indicating that significant interdiffusion was not occurring in the devices produced in this work.

The spectral response is observed to be lower for longer wavelengths than for shorter wavelengths consistent with similar observations made in electrodeposited cells [21]. The longer wavelength photons i.e. smaller energy photons are expected to be absorbed deeper in the CdTe away from the interface then higher energy photons and lower response reflects the small minority diffusion length expected in polycrystalline material [89].

Assuming that the following formula for the quantum efficiency, Q.E. is valid [90] :-

$$Q.E^{-1} = 1/L[1+1/\alpha(\lambda)] \qquad 5.17$$

where L is the minority carrier diffusion length and $\alpha(\lambda)$ the absorption coefficient then a plot of $Q.E.^{-1}$ versus $1/\alpha(\lambda)$ should be a straight line with an intercept on the horizontal axis equal to L. Such a plot is shown in

fig.5.57 and the minority carrier diffusion length, L=0.5μm for this device. This method to determine, L, has been used by various workers [90-92] to measure L in semiconductors. Mitchell and Fahrenbruch [91] obtained a value for L in the range 0.4 to 1μm and hence the value obtained in this work is very encouraging.

When the reverse bias voltage was applied to the device the spectral response was increased as shown in fig.5.58. This increase in response is to be expected in polycrystalline devices where the minority carrier diffusion is small. The increase in depletion region width, w with reverse bias permits more efficient collection of the carriers generated.

5.16 Model of CdS-CdTe Solar Cell:

The Anderson model [93] assumes that each semiconductor is characterised by its energy bandgap, E_g, its electron affinity, X and its work function,φ.

For a n-type semiconductor, φ_n is given by :-

$$\varphi_n = X_n + \delta_n \qquad 5.18$$

where δ_n is the energy separation of the Fermi level from the conduction bandedge.

For a non-degenerate semiconductor,δ_1, is given by :-

$$\delta_n = (-kT/q)\ln(N_D/N_C) \quad (eV) \qquad 5.19$$

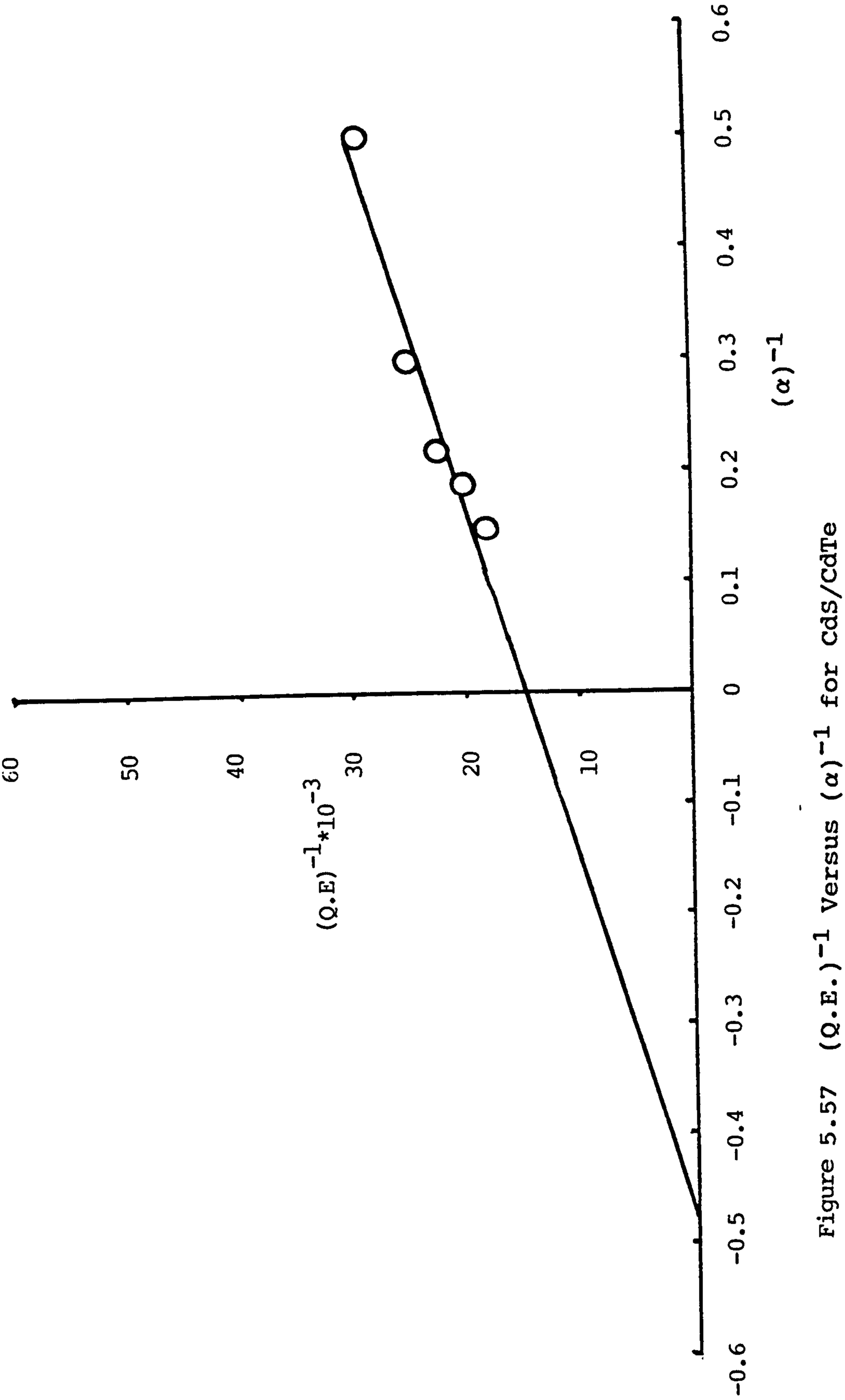


Figure 5.57 $(Q.E.)^{-1}$ Versus $(\alpha)^{-1}$ for CdS/CdTe Solar Cell

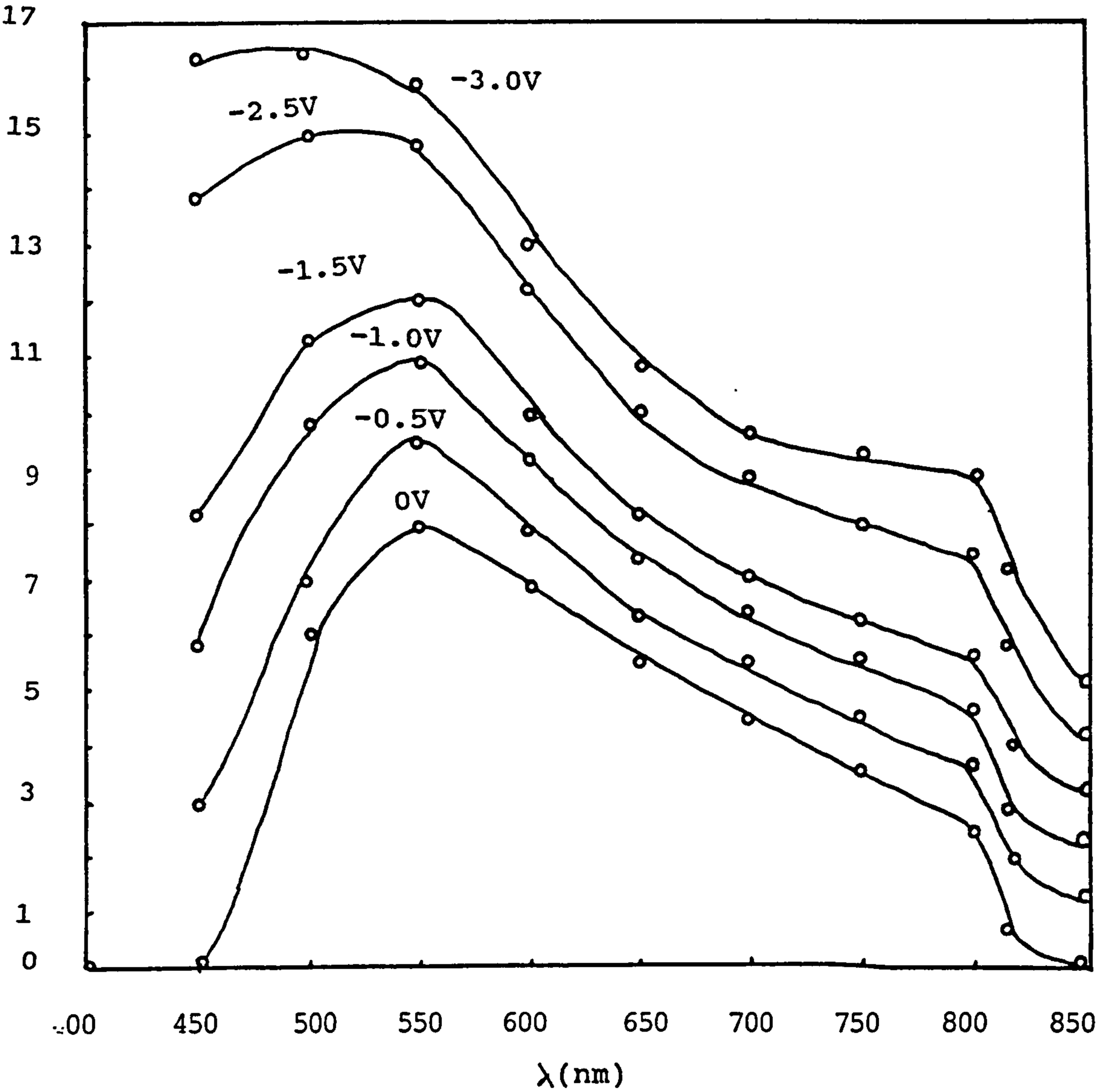


Figure 5.58 Spectral Response of CdS/CdTe Solar Cell for Different Applied Biases

where N_D is the donor concentration and N_C is the effective density of states at conduction bandedge. N_C is given by [94] :-

$$N_C = 2.5*10^{19}(m_n^*/m)^{3/2}(T(k)/300)\ cm^{-3} \qquad 5.20$$
$$= 2.41*10^{18}\ cm^{-3} \text{ for CdS at } 300^\circ k.$$
(For CdS, $m_n^*/m=0.21$ [90]).

Values for δ_n ($=E_c-E_f$) for CdS are given in table 5.3 $\delta n=.1eV$ for $N_D=10^{17}cm^{-3}$ and $\delta_n=0.023eV$ for $N_D=10^{18}cm^{-3}$.

For a p-type semiconductor, φ_p, is given by :-

$$\varphi_p = x_p+E_g-\delta_p \qquad 5.21$$

where δ_p is the energy separation of the Fermi level from the valence bandedge.

For a non-degenerate p-type semiconductor, δ_p, is given by:

$$\delta = (-kT/q)\ln(N_A/N_V) \quad (eV) \qquad 5.22$$

where N_A is the acceptor concentration and N_V is the effective density of states at the valence bandedge. N_V is given by [95] :-

$$N_V = 2.5*10^{19}(m_p^*/m)^{3/2}(T(k)/300)\ cm^{-3} \qquad 5.23$$
$$= 1.31*10^{18}\ cm^{-3} \text{ for CdTe at } 300^\circ k$$
[For CdTe, $m_p^*/m=0.37$ [94]].

Values for δ_p for CdTe are given in the table 5.3.

TABLE 5.3

Carrier Concentration P-CdTe	n-CdS	P-type CdTe = δp (E_F-E_V)eV	n-type CdS ~ δn (E_C-E_F)eV	Built-in diffusion voltage $Vb=Egp+\Delta E_C-\delta n-\delta p$
$10^{14}cm^{-3}$	$10^{17}cm^{-3}$	0.284eV	0.1eV	~0.92eV
$10^{14}cm^{-3}$	$10^{18}cm^{-3}$	0.284eV	0.023eV	~0.993eV
$10^{17}cm^{-3}$	$10^{17}cm^{-3}$	0.1eV	0.083eV	~1.117eV
$10^{17}cm^{-3}$	$10^{18}cm^{-3}$	0.16eV	0.023eV	~1.117eV

δ_p=0.284 eV for $N_{A=10}{}^{14}cm^{-3}$, δ_p=0.16 eV for $N_A=10^{16}cm^{-3}$.
The two semiconductors are shown in isolation of fig.5.59(a)
If the two semiconductors are brought into intimate contact and the interface states are ignored then the Anderson model [93] predicts the energy band profile shown in fig.5.59(b) should result. This type of profile without a "spike" and "notch" is either the conduction band edge or the valence band edge results because $E_{gn}>E_{gp}$, $x_p<x_n<x_p+E_{gp}$ and $\varphi_p>\varphi_n$ in this case [95].
The discontinuity in the conduction band edge, $\blacktriangle E_c$, arises from the difference in the electron affinities of the materials i.e.

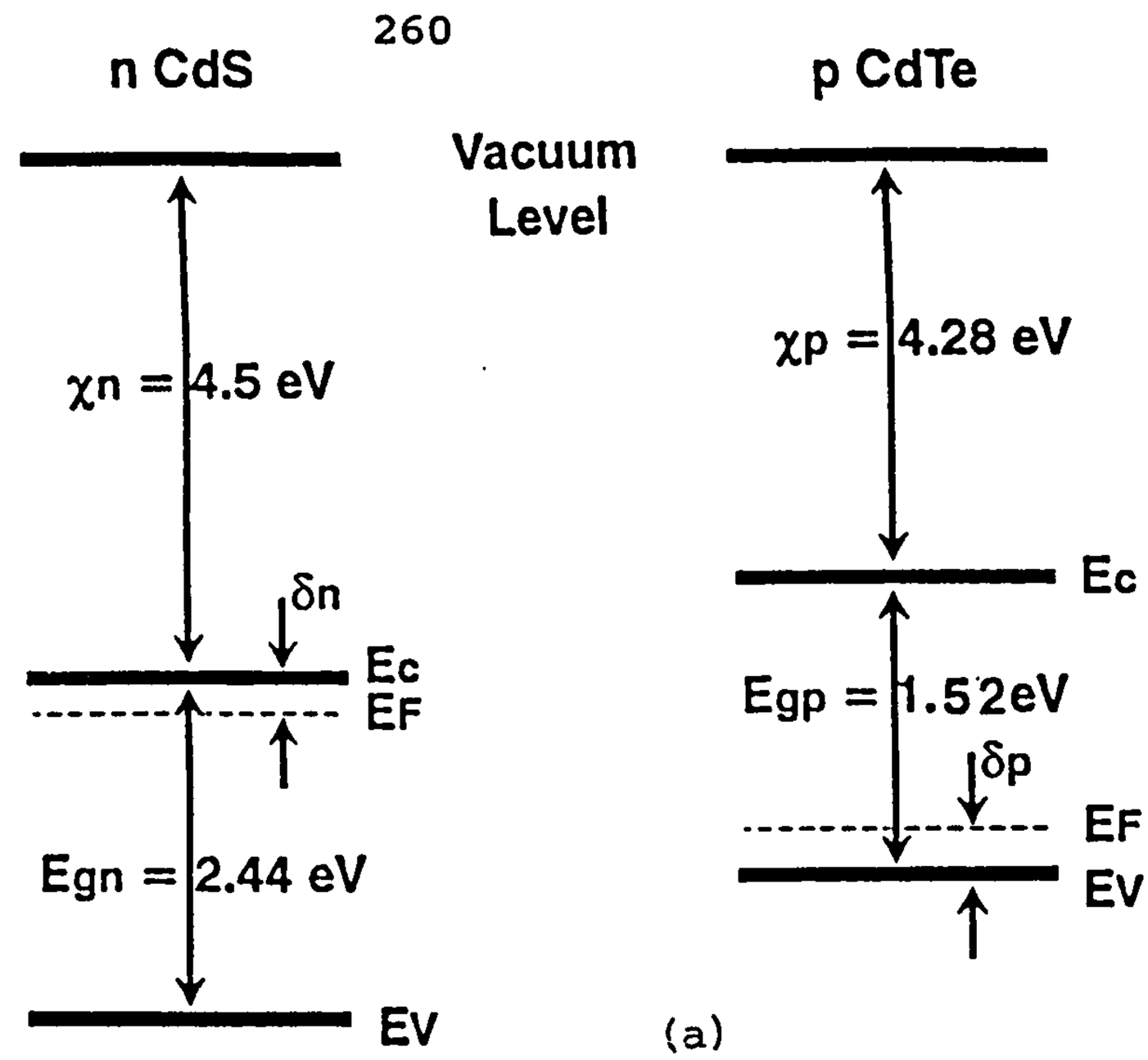
$$\blacktriangle E_c = x_n - x_p \qquad 5.24$$
$$= 4.50 - 4.28 = 0.22eV$$

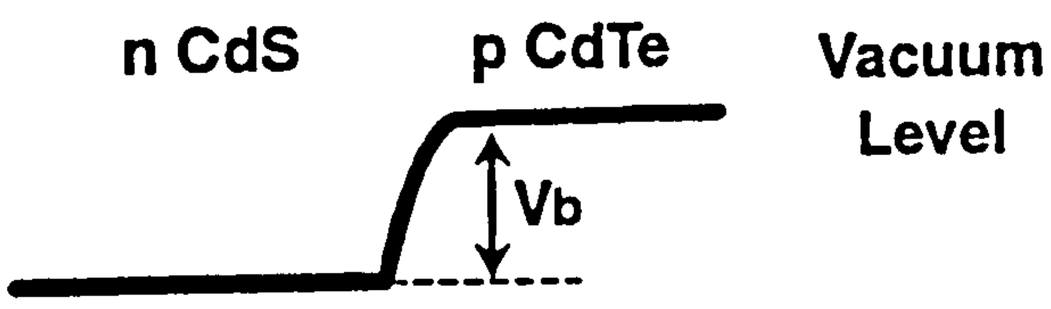
This discontinuity in the valence band edge, $\blacktriangle E_v$, arises from the difference in the energy bandgaps and electron affinities of the two semiconductor materials i.e.

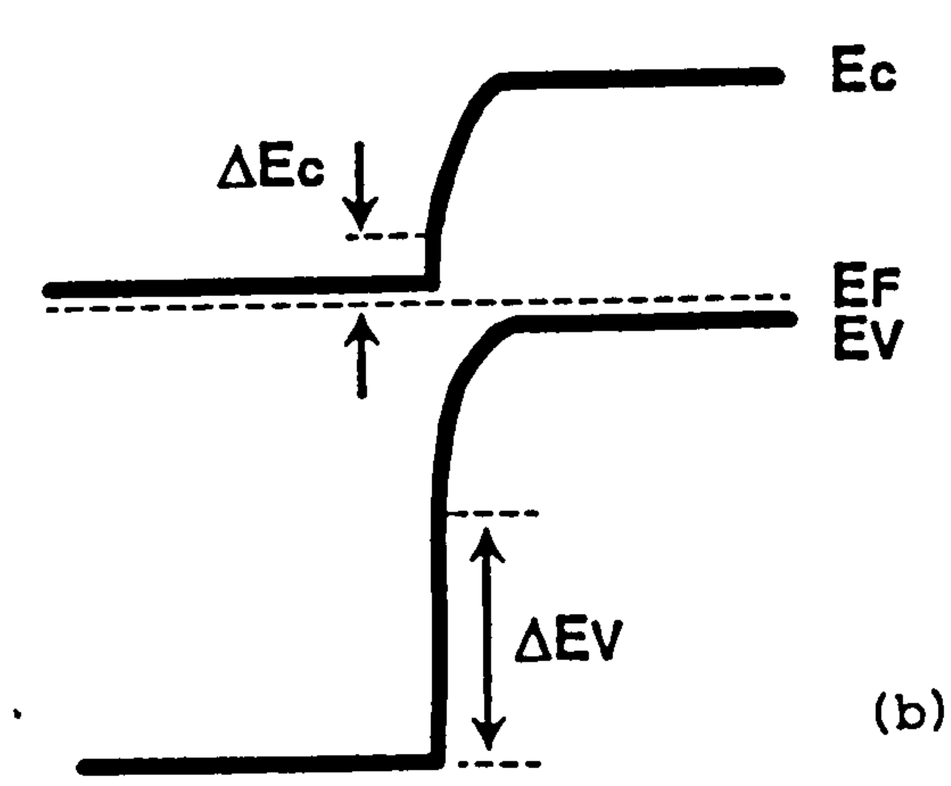
$$\blacktriangle E_v = (E_{gn}-E_{gp})-(x_n-x_p) \qquad 5.25$$
$$= (2.44-1.52) - (4.5-4.28)$$
$$= 0.7 \text{ eV}$$

The total built-in potential is given by

$$V_D = \varphi_p - \varphi_n \qquad 5.26$$
$$= (E_{gp}+x_p-\delta_p) - (x_n+\delta_n)$$
$$= E_{gp}+x_p-x_n-(\delta_n+\delta_p)$$
$$= 1.30 - (\delta_n+\delta_p)$$







Where

$$Vb = Egp + \Delta EC - \delta n - \delta p$$
$$\Delta EC = \chi p - \chi n$$
$$\Delta EV = (Egn - Egp) - \Delta EC$$
$$\delta n = kT \ln (NC/ND)$$
$$\delta p = kT \ln (NV/NA)$$

Figure 5.59 (a) Energy Band Diagram of CdS and CdTe Before Formation of the Hetrojunction.

(b) Energy Band Diagram After Formation of CdS-CdTe Hetrojunction.

Thus if CdS and CdTe were both very heavily doped so that the Fermi level is at the conduction edge in the CdS and the Fermi level is in the valence bandedge in the CdTe then V_D=1.3eV. Using realistic values for the doping in the CdTe (i.e. $N_A=10^{16}cm^{-3}$) and the CdS (i.e $N_D=10^{17}cm^{-3}$) then δ_p=0.16eV and δ_n=0.083eV and V_D is reduced to 1.11 eV.

The fraction of the diffusion voltage in the CdS, V_{DCdS} to the diffusion voltage in the CdTe, V_{DCdTe} is given by :-

$$(V_{DCdS}/V_{DCdTe})=(N_A\epsilon_{CdTe})/(N_D\epsilon_{CdS})=2.04*10^{-2} \qquad 5.27$$

If $N_A=10^{16}cm^{-3}$, $N_D=10^{18}cm^{-3}$, ϵ_{CdTe}=11[90] and ϵ_{CdS}=5.4 [90].

The fraction of the depletion region in the CdS to that in the CdTe is given by :-

$$x_{CdS}/x_{CdTe} = N_A/N_D \qquad 5.28$$

This ratio is 0.1 if $N_A=10^{16}cm^{-3}$ and $N_D=10^{17}cm^{-3}$ and 0.01 if $N_A=10^{16}cm^{-3}$ and $N_D=10^{18}cm^{-3}$.

Even for a carrier concentration difference of one order of magnitude nearly all the depletion region width lies within the lightest doped hetrojunction partner material i.e. in this case, the CdTe.

The results from section 5.14 indicate that interface states cannot be completely ignored because they strongly influence the current transport in forward bias and the

C-V behaviour of the devices.

The evidence suggests an interface state density $\approx 8.2*10^{9}cm^{-2}eV^{-1}$ to account for such behaviour. The charge on the interface states may perturb the values calculated in this section.

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CHAPTER VI

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

Thin films of CdTe have been successfully produced using S.E.L. processing. Synthesising the CdTe by annealing the Cd/Te stacks in nitrogen or vacuum was better than annealing in air because for the former anneals the CdTe produced did not contain $CdTeO_3$. The use of Cd and Te layers < 1000A° thick and an annealing temperature of 450°C (for 15 minutes) produced layers with the best mechanical and optical properties. All the layers produced had the sphalerite crystal structure and the layers synthesised in vacuum or nitrogen consisted of small randomly orientated grains ≈ 1000A° in diameter. Although larger grains were produced when the CdTe was synthesised in air, these grains were also randomly orientated and did not result in solar cells with acceptable efficiencies.

In agreement with other workers, producing CdS/CdTe solar cells using other methods, dipping the samples into $CdCl_2$/methanol solution (1:100 by mass) and then annealing at 450°C for 15 minutes was found to dramatically alter the physical properties of the layers. The layers now consisted of large (> 1.5μm diameter), columnar grains. The layers then needed to be etched in a bromine methanol solution (0.1%) to produce a tellurium rich surface for the electrical properties of the layers to be measured. The layers were p-type with carrier

concentrations $\approx 10^{15}$-$10^{16}cm^{-3}$ as determined using Van der Pauw measurements and C-V measurements on completed devices.

Thin films of CdTe were also produced using the co-evaporation of Cd and Te. These layers differed from the layers produced using S.E.L. processing in that they had wurzite (hexagonal) crystal structure.

Layers of CdS were also deposited and it confirmed that a substrate temperature of 200°C was optimum to produce CdS with good morphology, high transmittance and low enough value of resistivity. A CdS thickness > 1.2μm was essential to avoid the presence of pin holes in the grown layers.

The solar cell devices were fabricated in the superstrate configuration (glass/I.T.O./CdS/CdTe/back contact) in which the I.T.O. coated glass supplied by B.P. Solar International had a resistivity of 8-9 Ωcm. The best devices produced used the CdTe synthesised by annealing in nitrogen, followed by a dip in the $CdCl_2$/methanol followed by another anneal in nitrogen at 450°C for 15 minutes. The CdTe was then etched in the bromine / methanol solution and a copper doped graphite paste back contact applied. Annealing the contact at 450°C for 15 minutes was found to be optimum to produce the highest value of $V_{o.c.}$, $J_{s.c.}$ and F.F.

Such devices had $V_{o.c.} \approx 680mV$, $J_{s.c.} \approx 11mAcm^{-2}$ and F.F. ≈ 0.35 with an overall device efficiency of 2%. The CdTe thickness had to be at least 1.5μm to ensure a high value of $V_{o.c.}$.The spectral response of such devices indicated

that the devices were true CdS/CdTe hetrojunctions devices rather than buried homojunction devices. The minority carrier diffusion length in the CdTe was found to 0.48 μm which was within the range 0.4 - 1.4μm reported by K W Mitchell et. al. [1] for his single crystal CdTe and which were used to produce CdTe/CdS solar cells with efficiencies of 8%.

Detailed analysis of the I-V forward characteristics indicates a thermal type conduction mechanism is operating with J_{oo} = 800Acm^{-2}, $J_o \approx 3.63*10^{-8}$Acm^{-2}, φ = 0.66eV and A= 1.5-2.1. These values are similar to those obtained by other workers producing CdTe/CdS solar cells using other methods and are consistent with a tunnelling-recombination mechanism in which recombination limits the current flow. An interface recombination velocity, S =5.0*10^{5}cm/s a trap density N_t = 7.0*10^{12}cm^{-2} and a capture cross section for the traps, σ = 6.0*10^{-15}cm^2 are estimated if the Donnelly and Milnes model [2] is assumed to be applicable.

The variation of device capacitance with frequency was also used to estimate the density of interface states, N = 2-8*10^{9}cm^{-2}eV^{-1}. This is almost order of magnitude smaller than that measured in the CdS/CdTe devices produced using electrodeposition by Morris et al [3] who were able to produce devices with efficiencies ≈ 10.8%. The good columnar grain structure, the good value of diffusion length, the "low" density of interface states and the promising values for $V_{o.c.}$ and $J_{s.c.}$ indicatethat the CdTe produced and its interface with CdS are

good. The low value of fill-factor ≈ 0.35 is currently limiting the device efficiency. The fill-factor is strongly influenced by the series resistance (≈ 40 Ω) of the device which results from the resistance of the CdS the CdTe and the contact resistances to these materials. The reduction of these resistances further should improve not only the fill-factor but also $J_{s.c.}$ to improve the overall device efficiency. Improving both F.F. and $J_{s.c.}$ by a factor of two would result in a device efficiency ≈ 8%.

To reduce the CdS resistivity further the CdS/I.T.O should be annealed in a mixture of H_2/N_2 ("forming gas"). Matsushita [4], for example report a reduction in CdS resistivity by one order of magnituide by annealing in forming gas at 400°C for 30 minutes. Alternatively "dip CdS" could be used [5] to produce thinner CdS free from pinholes.

The annealing of CdTe after the dip in the $CdCl_2$/methanol solution could be controlled more accurately by using a mixture of air and nitrogen. There is some evidence [6,7] that the ratio of air/nitrogen used strongly affects the resistivity of the CdTe produced. If the concentration of oxygen is too high there is a tendancy to form highly resistive oxides whereas if the concentration of oxygen is too low there may not be adequate type conversion and doping of the CdTe.

Further optimisation of the surface etching of the CdTe prior to forming the back contact needs to be made with the improved CdTe. The bromine/methanol etching may need

to be optimised further and more experiments performed using HNO_3-H_2SO_4 [8], hydrazine [9] and KOH [10].

A wider selection of back-contact materials e.g. N_i-Al [11] or Ni-P [12] should also be used to determine the best back-contact material for the CdTe. An alternate strategy would be to develop the co-evaporation of Cu with ZnTe to produce copper doped ZnTe as the back contact as successfully used by Ametek [13] to avoid the back contact problem.

In a parallel research programme an energy analysis of the use of S.E.L. processing to produce CdTe modules has been made [11]. The energy payback times and energy ratios are very promising for using such a method to produce CdTe/CdS modules. It hoped that when the devices have been optimised the technology may be scaled-up to produce large area devices and thus form the basis on an alternate technology for producing CdTe/CdS modules, in an area where there is extensive patent coverage of the alternate device fabrication techniques.

The S.E.L. technique remains a novel method of producing thin film materials. Now that it has been successfully used to produce CdTe (in addition to $CuInSe_2$ formerly) it would appear to have wide application as a method for producing thin film materials.

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APPENDIX A

Thickness Ratio of Cd and Te to Give a 1:1 Stoichiometry:

Atomic mass of cadmium ≈ 112.40

Atomic mass of tellurium ≈ 127.60

Density of cadmium ≈ 8.64gcm-3

Density of tellurium ≈ 6.25gcm-3

Volume of 1μm of film of diameter 2cm ≈ π*10-4cm3

Mass of 1μm of cadmium of diameter 2cm ≈ 2.71*10-3 gm

Mass of 1μm of tellurium of diameter 2 cm ≈ 1.96*10-3 gm

No. moles of cadmium = 2.71*10-3/112.40 = 2.41*10-5

No. moles of tellurium needed for

1:1 stoichiometry = 2.41*10-5

Mass of tellurium = 2.4*10-5*127.60

= 3.08*10-3g

Thickness of a film of tellurium of mass 3.08*10-3g

and diameter 2cm = 1.5μm.

For a molar ratio of 1.00 Cd : 1.00 Te, the film thickness should be in the ratio :

1.00 Cd : 1.57 Te.

APPENDIX B

Physical Properties of CdS and CdTe Thin Films.

	CdS	CdTe
Energy Band-gap (300 k°)	2.42 eV	1.5 eV
Typical mobility, μ_n	340 $cm^2v^{-1}sec^{-1}$	30 $cm^2v^{-1}sec^{-1}$
Typical mobility, μ_p	.....	65 $cm^2v^{-1}sec^{-1}$
Dielectric Constant (ϵ_r)	9.0-10.3*ϵ_o	9.6*ϵ_o
Thermal Expansion Coeff-icient	$4*10^{-6}$ $^{\circ}c^{-1}$	$4.9*10^{-6}$ $^{\circ}k^{-1}$
Electron Affinity.	4.5 eV	4.28 eV
Lattice Constants(A°)	4.135 (W) 7.749 (W)	4.57 (W) 6.47 (W) 7.47 (C)
P-type dopants	.....	Li, Sb, P, Bi Cu, As, Na,Ag NaCN, AgTe.
N-Type dopants	Cl,Br,Al,Ga I,In.	
Structure	Wurtzite(Hex)	Sphalerite, Wurtzite.
Typical Resistivity	50-100 Ωcm	10^4-10^7 Ωcm
Contact Material	Al,ITO	Ni-Cu,Au,AuCu NiP,HgTe,ZnTe
Diffusion Length	.....	$L_n \approx 0.8$-$1.0\mu m$ $L_p \approx 0.4$-$1.6\mu m$