High Speed All-optical Packet Switching Router Employing Single and Multiple PPM Based Routing Tables

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ABSTRACT

All-optical packet switched networks with flexibility and capability to deal with the bursty traffic is one solution to deal with the ever increasing demand for bandwidth. To fully utilise the potential of such networks and to ensure that high-speed packets, passed through a number of nodes, are faithfully delivered to their intended destination with minimum delay times, packet header processing and routing decision needs to be carried out in the optical domain not in the electrical domain. This is to avoid the speed bottleneck imposed by the slow response of currently available electronic devices beyond 40 Gb/s. At present, packet header recognition is carried out by sequentially correlating the incoming packet header address with every entry of a local routing table. For a small size network, with a reasonable size routing table, sequential correlation is viable both in terms of processing speed and implementation complexity. However, for a large size network with a very large size routing table of hundreds or thousands of entries, the cost, complexity and processing time does become a real issue. The latter will lead to a noticeable increase in the packet processing time at every router, which could be significantly reduced by a non-conventional signal formatting. In this thesis, an all-optical 3-input AND gate and an all-optical 1×2 switch with high contrast ratio are proposed as an essential element in all-optical routers. New routing schemes employing pulse position modulation (PPM) packet header format as well as single and multiple PPM based routing tables (PPRTs) are proposed and investigated. The main advantage of the proposed scheme is reduced size routing table leading to a faster router processing time compared to the routers with conventional routing tables (CRTs). The correlation-time gains offered by the proposed schemes are given by theoretical calculations. For optical packets with 4-bit

binary address, all-optical 1×3 routers employing single and multiple PPRTs with an entry slot of 6.25 ps offer ~ 100 and ~ 400 times faster processing times when compared to the routers employing CRT, respectively. The performance of the proposed routers employing single and multiple PPRTs are assessed in terms of optical signal-to-noise ratio (OSNR) in multi-hop routing by means of numerical simulations and theoretical analysis. It is shown that predicted and simulated OSNR decreases by ~2 dB after each hop. New packet header address formats proposed offers reduced complexity of nodes by employing single or multiple PPM based routing tables. Adopting a hybrid header address format, it is shown that routers with multiple PPRTs can operate at 160 Gb/s with the output intra-channel crosstalk of -18 dB and with output packet power fluctuation of 2 dB. Finally, a WDM router employing a single PPRT, capable of processing packets at different wavelengths simultaneously, is proposed and its inter-channel crosstalk performance is investigated. At 160 Gb/s, results obtained show an inter-channel crosstalk of ~ -27 dB at a channel spacing of greater than 0.4 THz and a demultiplexer bandwidth of 500 GHz.

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DECLARATION

I hereby declare that this thesis is entirely my own work and has not been submitted in support of an application of another degree or qualification of this or any other university, institute of learning or industrial organisation

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Date: 24 October 2008

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GLOSSARY OF ACRONYMS

2R	Reshaping and Re-amplification
3R	Reshaping, Re-amplification and Retiming
AM	Amplitude Modulation
AOFF	All-Optical Flip-Flop
AOLS	All-Optical Label Switching
ASE	Amplified Spontaneous Emission
ATM	Asynchronous Transfer Mode
BER	Bit Error Rate
CB	Conduction Band
CCW	Counter Clockwise
CEM	Clock Extraction Module
CLK	Clock
CP	Control Pulse
CPMZ	Colliding-Pulse Mach-Zehnder
CR	Contrast Ratio
CRT	Conventional Routing Table
CXT	Crosstalk
CW	Clockwise
DCF	Dispersion Compensation Fibre
DFB	Distributed-Feedback
DWDM	Dense Wavelength Division Multiplexing
EDFA	Erbium-Doped Fibre Amplifier
EDWA	Erbium-Doped Waveguide Amplifier
FBG	Fibre Bragg Grating

FDL	Fibre Delay Line
FWHM	Full Width at Half Maximum
FWM	Four Wave Mixing
HEM	Header Address Extraction
IP	Internet Protocol
JET	Just-Enough-Time
LAN	Local Area Network
MAN	Metropolitan Area Network
MEMS	Micro-Electro-Mechanical Systems
MPPRT	Multiple Pulse Position Routing Table
MQW	Multi-Quantum-Well
MSB	Most Significant Bit
MZI	Mach-Zehnder Interferometer
NF	Noise Figure
NOLM	Nonlinear Optical Loop Mirror
OADM	Optical Add/Drop Multiplexer
OBS	Optical Burst Switching
OCS	Optical Circuit Switching
O-E-O	Optical-to-Electrical-to-Optical
OOK	On-Off Keying
OPS	Optical Packet Switching
OSI	Open System Interconnection
OS	All-Optical Switch
OSC	OS Control
OSNR	Optical Signal to Noise Ratio

OXC	Optical Crossconnect
PBS	Polarisation Beam Splitters
PC	Polarisation Controller
PDH	Plesiochronous Digital Hierarchy
PM	Polarisation Maintaining
PoS	Packet over SDH/SONET
PPM	Pulse-Position-Modulation
PPM-HP	Pulse-Position-Modulation Header Processing
PPRT	Pulse Position Routing Table
PSI	Polarisation Sensitive Optical Isolator
RAM	Random Access Memory
RZ	Return to Zero
SDH	Synchronous Digital Hierarchy
SMF	Single Mode Fibre
SMZ	Symmetric Mach-Zehnder
SOA	Semiconductor Optical Amplifier
SONET	Synchronous Optical Network
SPC	Serial to Parallel Converter
STM	Synchronous Transport Module
STS	Synchronous Transport Signal
SW	Switching Window

TAG	Tell-And-Go
TAW	Tell-And-Wait
TOAD	Terahertz Optical Asymmetric Demultiplexer
UNI	Ultrafast Nonlinear Interferometer
VB	Valence Band
WAN	Wide Area Network
XGM	Cross Gain Modulation
XPM	Cross Phase Modulation

GLOSSARY OF SYMBOLS

α	Optical loss of SOA
α_{LEF}	Linewidth enhancement factor of SOA
η_i	Current injection efficiency of SOA
Γ	Confinement factor of SOA
τ_s	Spontaneous recombination lifetime of the carriers
τ_{tot}	Total required time for PPM address correlation
$\Delta\phi$	The phase difference
B_o	Optical bandwidth of the system (i.e. filter optical bandwidth)
$c(t)$	Extracted clock signal
d	Thickness of the active region of SOA
e	The electronic charge
$E(t)$	PPRT entry
G_{OS}	Gain of optical switch
G	Gain of SOA
g	Differential gain of SOA
g_m	Material gain of SOA
g_0	Gain coefficient of SOA
I	Injection current of SOA
L	Length of the active region of SOA

L_{combiner}	Insertion loss of the combiner
L_{MPPRT}	Total power loss due to multiple PPRT generator
L_{splitter}	Insertion loss of the splitter
$m(t)$	Match signal
n_{sp}	The spontaneous-emission factor
N	Carrier density of SOA
N_0	Carrier density (at transparency) of SOA
P_{ase}	ASE noise power
$P_{in}(t)$	Input power
P_{nt}	Sum of the output signal power of all non-target channels
$P_{\text{OSC-in}}$	Minimum required power of the input pulse for OSC
$P_{\text{OSC-out}}$	Peak power of the CP stream generated by OSC
$P_{out}(t)$	Output power
P_{t}	Sum of the output signal power of the target channel
r_{AM}	Amplitude modulation ratio
$r_{\text{on/off}}$	On/off contrast ratio
R_{b}	Data bit rate
R_{MPPRT}	Correlation-time gain by employing multiple PPRTs
R_{PPRT}	Correlation-time gain by employing PPRT
T_{AND}	Time interval required for two successive AND operations
T_{b}	Bit duration

T_{CRT}	Address correlation time of conventional routing table
T_{MPPRT}	Address correlation time of multiple PPRTs
T_{PPRT}	Address correlation time of PPRT
T_s	PPM time slot
T_{sw}	Switching window width
V_g	Group velocity of the control pulses
$W(t)$	Width of the SW profile
w	Width of the active region of SOA
$X_{PPM}(t)$	PPM header frame

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CHAPTER 1 INTRODUCTION

1.1 Background

Fibre-optic communication system has become the backbone behind the Internet due to the huge capacity it offers. As the demand for network capacity is growing rapidly, there is an increasing need for all optical based systems capable of offering a much greater bandwidth than the widely used traditional copper cables and RF based communications technologies. A common way to calculate merit of any communication system is the bit-rate-distance product (BL), where B is the bit-rate and L is the repeater spacing, see Figure 1.1. Optical fibre network was first utilised for a simple point-to-point link with no routing capabilities. The second generation systems such as synchronous optical network (SONET) and synchronous digital hierarchy (SDH) [1, 2] employing wavelength division multiplexing (WDM) [3-6] were developed for high speed links with some switching and routing capabilities. Optical add/drop multiplexers (OADMs) and optical crossconnects (OXCs) were developed and exploited to offer wavelength routing in all-optical domain [7]. However, in all conventional communication networks the switching process (i.e. routing packet etc.) is still performed in the electrical domain requiring the costly optical/electrical/optical (O/E/O) conversion modules [7, 8]. Inclusion of O/E/O conversion modules not only requires additional power, but it also imposes bandwidth bottleneck largely due to the processing speed of the conventional electronic components currently being limited to 40 Gbit/s [9, 10]. Although the electronic processing speed is increasing and in the next few yeas 80 Gb/s may be practically realizable, there is a growing research interest to ensure that the next generation

optical networks are all-optical with no O/E/O conversions at all [11-15]. This is a challenge that a number of researchers have addressed over that last few years, and as a results we are now seeing practical implementation of all-optical networks at speeds far beyond the most advanced O/E/O devices [16]. Of course, the penalty paid for this surge in speed is the cost and complexity of the network. However, with large scale deployment of all-optical systems, it is expected that the cost will drop considerably, thus making it viable for a large scale adaptation at a global level.

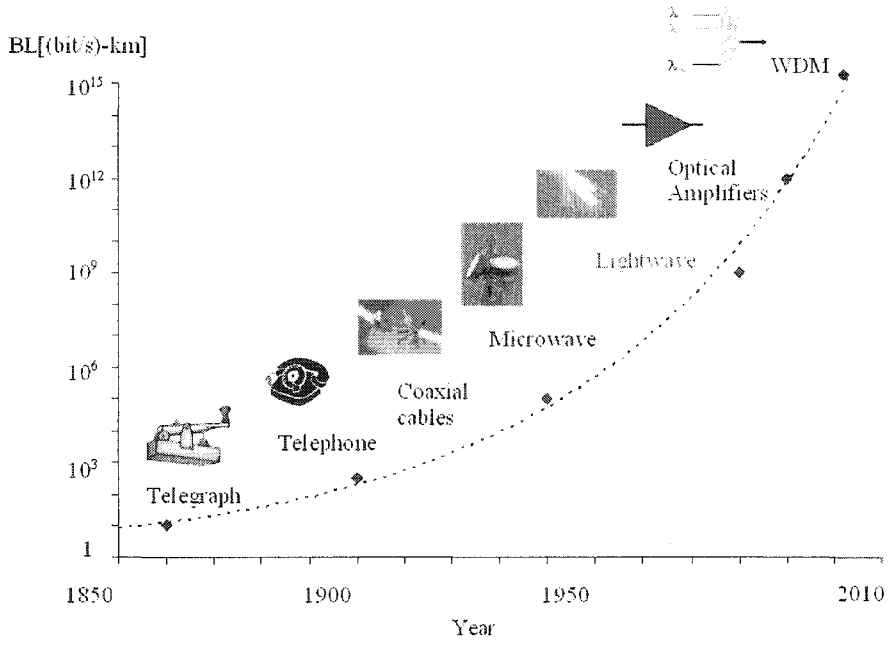


Figure 1.1 BL products against the different communication technologies

All-optical networks based on packet-switching [17-23] are more flexible compared with the traditional circuit-switched networks thus offering bursty traffic as well as higher throughput and switching speed [23, 24]. An all-optical network also offers *transparency* [25] which implies that data can be carried at a mixture of bit rates and protocols, thus the optical layer is capable of supporting different higher layers at the same time.

Figure 1.2 illustrates a typical optical core network where optical packets traverse a number of different nodes to reach their intended destination nodes. Packets are composed of payload (information) and a header which contains the destination address. At each node, packet routing decision is carried out by comparing the packet header address with the node identification located in the routing table (RT). If the packet header address matches the node address then the packet is doped otherwise it is passed on to the next stage.

There are a number of packet header recognition and processing techniques that have been developed in recent years [22, 26-28] including the self-routing [29, 30] and the codeword matching [31-33]. Self-routing is the most simplest scheme where, at each node, the packet header address bit sequence extracted are directly used as the control signal to route the packet to the relevant output port of the optical switch (OS). For a larger size network, packets will normally require a longer header field, thus resulting in increased system complexity. In [29], a self-routing scheme that identifies the network nodes output ports instead of the output ports of the nodes themselves has been proposed. This scheme is applicable to networks with arbitrary topologies. It only requires a single-bit processing and allows multiple addresses for the same nodes. By sharing address bits, it is possible to reduce the packet address length by up to 80%. However, self-routing schemes are only suitable for small or medium size networks, since the header length is noticeably expanded as the number of nodes increases.

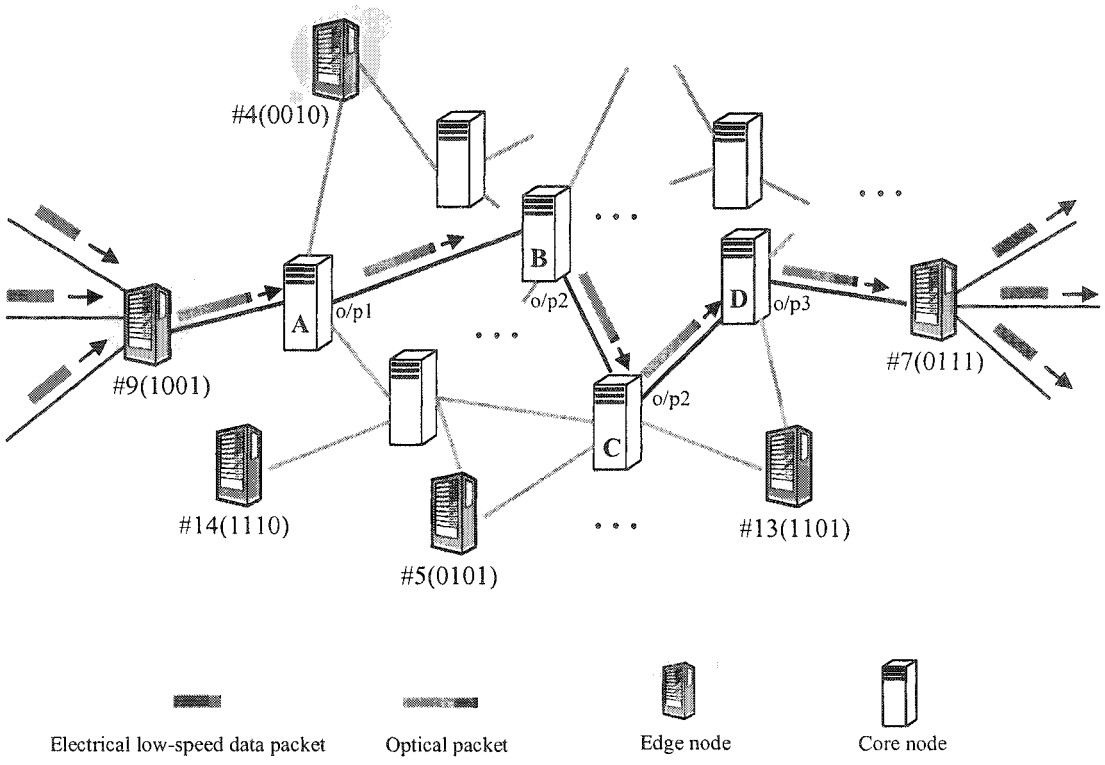


Figure 1.2 An optical core network with 16 edge nodes

At present, nearly all optical header recognition and processing schemes are based on the packet header address correlation requiring a large size routing table (> 5×10^5 entries) [34, 35]. In [31-33], all-optical bank correlators, and all-optical logic circuits have been employed, respectively to implement all-optical codeword matching in small-scale networks with a routing table of many entries. However, for larger-scale networks, the implementation of the above schemes would be a challenging and time consuming task due to complexity of all-optical configurations, a large size routing table and lack of all-optical storage. For a small size network (i.e. reduced size routing table) header processing could be implemented using a bank of all-optical mirror-based correlators [31] and all-optical logic gates (OR, XOR, AND) [36-53]. However, for a larger size network, the correlation becomes a challenging task due to the exponential increase in the number of routing table entries. In addition, all-optical

logic gates employing active nonlinear devices such as the semiconductor optical amplifiers (SOAs) [54-57] suffer from a long gain recovery time (~ 1 ns) after each correlation, thus limiting the operational speed to 80 Gb/s. Therefore, to carry out a large number of correlation at high data rates (> 80 Gb/s) in the optical domain with a minimum processing time, one desires to utilise either a significant number of parallel gates or a small number of gates for sequential correlation. However, these solutions are not feasible in the current practical systems.

An alternative packet header processing method based on the pulse-position-modulation based header processing (PPM-HP) has been proposed in [58, 59]. In this scheme both the incoming packet header address bits and the routing table entries are converted from return-to-zero format into a PPM format. The advantages of this scheme are (i) significantly reduced routing table entries, where each entry contains more than one header address information in the form of a PPM pulse, (ii) considerably reduced correlation processing time by using only a single bitwise AND gate instead of a large number of gates with a low response-time, and (iii) offering multiple transmitting modes (unicast, multi-cast and broadcast) embedded in the optical layer. The conventional PPM router requires a serial-to-parallel converter (SPC) to extract the individual bits from the incoming packet header address, an array of 1×2 switches and the delay lines. For packets with a long header address sequence, the switching stages at the header address conversion module will contribute to the deterioration of the extinction ratio of the output PPM address and increased system complexity. In CHAPTER 4, an enhanced node architecture based on the PPM address format no longer employing SPC and an array of 1×2 switches has been proposed, thus significantly reducing the system complexity.

The processing time of the conventional PPM router is limited by the length of the PPM address time frame (i.e. the entry length of the PPM routing table). In CHAPTER 5, a new routing scheme based on the multiple pulse position routing tables (multiple PPRTs) has been proposed, where by checking the most significant bits (MSBs) of the packet address, only a subset of the header address is converted into a PPM format, thus resulting in a reduced length of PPRT entries leading to significantly reducing router's processing time. A simplified and efficient routing scheme based on a hybrid header address has been proposed in CHAPTER 6, where the packet header address is based on the binary and the PPM formats. The hybrid address correlation scheme employing multiple PPRTs offers improved processing time and reduced system complexity. The abovementioned PPM routers are only designed for routing packets at a single wavelength. To increase the network throughput, an all-optical router based on the PPM correlation capable of routing WDM packets at multiple wavelengths simultaneously is presented in CHAPTER 7.

1.2 Aims and Objectives

This PhD research work aims to investigate the three main issues in all-optical routing scheme:

All-optical ultrafast header processing and address correlation

Investigate the current and future trends of all-optical header processing and address correlation schemes in all-optical networks (above 80 Gb/s). The node complexity is reduced by adopting the PPM formatted packet header address, and address correlation time is significantly improved by reducing the size of the routing table. To achieve this, the followings have been carried out:

- Defined new optical packet profile, node architecture
- Considerably reduced numbers of all-optical correlators
- Designed an optical logic for address correlation
- Carried out full-analysis of the node architecture and complete simulations of multi-hop routing
- Carried out system analysis (crosstalk, etc.)
- Compared analytical and simulated results

All-optical component

Investigate and analyse all-optical components, such as all-optical serial-to-parallel converter, all-optical switches with a high extinction ratio, and all-optical logic gates.

1.3 Chapter Outline

The thesis is organised into eight chapters as outlined below:

CHAPTER 1 - INTRODUCTION: It presents the research fundamental background and the aims and objectives of the research. It also outlines the original contributions made.

CHAPTER 2 - LITERATURE REVIEW OF ALL-OPTICAL ROUTING SCHEMES AND ALL-OPTICAL SWITCHES: The footprint of optical network evolution is presented in this chapter. All-optical packet-switching routing, address correlation schemes, and all-optical switches used for ultrafast optical processing are also introduced in this chapter.

CHAPTER 3 - SEMICONDUCTOR AMPLIFIER, SYMMETRIC MACH-ZEHNDER AND ITS APPLICATIONS: The structure and the nonlinearities of the SOA, and operation principle of the SMZ (i.e. the building block of the router) are illustrated in this chapter. Besides, a number of all-optical elements such as all-optical 3-input AND gate based on four-wave mixing, all-optical serial-to-parallel converter based on SMZ and an all-optical high contrast ratio 1×2 switch based on the SMZs are first reported and evaluated in simulation.

CHAPTER 4 - PPM BASED PACKET HEADER ADDRESS FORMAT: Converting a conventional binary address pattern into a PPM format will require a SPC, an array of 1×2 switches, and a number of fibre delay lines. In this chapter, a simplified routing scheme with no PPM address conversion modules is presented, thus offering reduced complexity.

CHAPTER 5 - ULTRA-FAST ALL-OPTICAL PACKET SWITCHED ROUTER WITH MULTIPLE PPRTS: In this chapter, a new routing scheme is proposed to improve the header address correlation time. The length of each PPRT entry is further reduced by introducing a novel multiple PPRT scheme. From the simulation results, therefore, it is shown that the header processing time is also reduced in comparison with the router using a single PPRT.

CHAPTER 6 - ALL-OPTICAL PACKET-SWITCHED ROUTER WITH A HYBRID HEADER ADDRESS FORMAT: A simplified and efficient routing scheme based on the hybrid header address is proposed in this chapter, where the

packet header address is based on the binary and PPM formats. The hybrid address correlation scheme employing multiple PPRTs offers improved processing time and reduced system complexity.

CHAPTER 7 - MULTIPLE WAVELENGTH ROUTER FOR WDM SYSTEM: In this chapter, a router designed for WDM optical transmission system capable of simultaneously routing packets at multiple wavelengths with no wavelength conversion modules is outlined. At the input of the router, packets at multiple-wavelengths are fed into a bank of PPM-HP modules via a WDM demultiplexer. Packets at specific wavelengths are processed at the PPM-HP modules.

CHAPTER 8 - CONCLUSIONS AND FUTURE: A summary of the research work is presented in this final chapter. The key findings and the comparisons of different proposed routing schemes will be outlined. The proposed further research directions and the challenges of realising all-optical packet-switched networks will be also discussed in the last chapter.

1.4 Original Contribution

Contributions to the knowledge of this research work are as follows:

- Proposed and investigated an enhanced PPM router architecture based on the PPM address format, which significantly reduces the system complexity compared with the previous PPM routing scheme, see CHAPTER 4.

- Proposed a new routing scheme based on the multiple pulse-position routing tables, resulting in significantly reduced header address correlation time, see CHAPTER 5.

- Proposed a simplified and efficient routing scheme based on packets with a hybrid address. The new routing scheme employing multiple PPRTs offers faster processing time and reduced system complexity, see CHAPTER 6.

- Proposed a new WDM router architecture for increasing the system throughput, which requires no wavelength conversion modules thus reducing the system complexity, see CHAPTER 7.

- Investigated the crosstalk characteristics of an all-optical serial-to-parallel converter, see Section 3.4.

- Further improvement of the existing ultrafast optical switches with higher contrast ratio, see Section 3.6. Have proposed a new all-optical 3-input AND gate, see Section 3.7.

The list of publications during this research works are as follows:

Articles and Letters in Journals

1. H. Le-Minh, Z. Ghassemlooy, W. P. Ng and M. F. Chiang, "All-optical router with PPM header processing in high speed photonic packet switching networks", accepted by IET Communications.

Conference papers

1. M. F. Chiang, Z. Ghassemlooy, W. P. Ng, H. Le Minh and V. Nwanafio, "Crosstalk investigation of an all-optical serial-to-parallel converter based on the SMZ", *proceeding of the 7th Annual Postgraduate Symposium on the Convergence of Telecommunications, Networking and Broadcasting (PGNET 2006)*, ISBN: 1-9025-6013-9, pp. 217-221, Liverpool, UK, Jun. 2006.

2. H. Le-Minh, Z. Ghassemlooy, W. P. Ng and M. F. Chiang, "All-optical packet router based on multi-wavelength PPM header processing", *proceeding of the 11th European Conference on Networks & Optical Communications (NOC 2006)*, ISBN: 3-923613-40, pp. 360-367, Berlin, Germany, Jul. 2006.

3. H. Le-Minh, Z. Ghassemlooy, W. P. Ng and M. F. Chiang, "Simulations of all-optical multiple-input AND-gate based on four wave mixing in a single semiconductor optical amplifier", *proceeding of the 14th IEEE International Conferences on Telecommunications 2007 (ICT-MICC 2007)*, ISBN: 978-1-4244-1094-1, pp. 191-196, Malaysia, May 2007.

4. M. F. Chiang, Z. Ghassemlooy, H. Le-Minh and W. P. Ng, "All-optical packet-switched routing based on pulse-position-modulated header", *proceeding of the 7th IASTED International Conferences on Wireless and Optical Communications (WOC 2007)*, ISBN: 978-0-88986-659-1, pp. 291-296, Montreal, Canada, May-Jun. 2007.

5. H. Le-Minh, Z. Ghassemlooy, W. P. Ng and M. F. Chiang, "Bit error rate performance of multiple-channel OTDM demultiplexer employing a chained symmetric Mach-Zehnder switch", *proceeding of the 50th IEEE Global Telecommunication Conference (GLOBECOM 2007)*, ISBN: 978-1-4244-1043-9, pp. F07P05, Washington DC, USA, Nov.-Dec. 2007.

6. M. F. Chiang, Z. Ghassemlooy, W. P. Ng and H. Le-Minh, "Simulation of an all-optical 1×2 SMZ switch with a high contrast ratio", *proceeding of the 8th Annual PostGraduate Symposium on the Convergence of Telecommunications, Networking*

and Broadcasting (PGNET 2007), ISBN: 1-9025-6016-7, pp. 65-69, Liverpool, UK, Jun. 2007.

7. M. F. Chiang, Z. Ghassemlooy, W. P. Ng and H. Le-Minh, "Ultra-fast all-optical packet-switched router with multiple pulse position routing tables", *proceeding of the 12th European Conference on Networks & Optical Communications (NOC 2007)*, ISBN: 978-91-633-0869-7, pp. 571-578, Kista Stockholm, Sweden, Jun. 2007.

8. M. F. Chiang, Z. Ghassemlooy, W. P. Ng, H. Le-Minh, and A. Abd El Aziz: " Multiple-hop routing in ultra-fast all-optical packet switching network using multiple PPM routing tables", *proceeding of IEEE International Conference on Communications 2008 (ICC 2008)*, ISBN: 978-1-4244-2075-9, pp. 5231-5325, Beijing, China, May. 2008.

9. M. F. Chiang, Z. Ghassemlooy, W. P. Ng, H. Le-Minh, and A. Abd El Aziz: " An ultrafast 1×M all-optical WDM packet-switched router based on the PPM header address", *proceeding of ICEE 2008*, Paper No. 2631, Tehran, Iran, May. 2008.

10. M. F. Chiang, Z. Ghassemlooy, W. P. Ng, H. Le Minh, and C. Lu: "Ultra-fast all-optical packet-switched routing with a hybrid header address correlation scheme", *proceeding of IEEE International Conference on High Performance Switching and Routing 2008 (HPSR 2008)*, ISBN: 978-1-4244-1982-1, pp. 92-97, Shanghai, China, May. 2008.

11. M. F. Chiang, Z. Ghassemlooy, W. P. Ng, and H. Le Minh, "Simulation of an all-optical 1×2 SMZ switch with a high contrast ratio", *proceeding of the 6th Symposium on Communication Systems, Networks and Digital Signal Processing 2008 (CSNDSP 2008)*, ISBN: 978-1-4244-1876-3, pp. 475-478, Graz, Austria, July 2008.

12. A. Abd El Aziz, Z. Ghassemlooy, W. P. Ng and M. F. Chiang, "Optimisation of the key SOA parameters for amplification and switching", *proceeding of the 9th Annual PostGraduate Symposium on the Convergence of Telecommunications, Networking and Broadcasting (PGNET 2008)*, ISBN: 978-1-902560-19-9, pp. 107-111, Liverpool, UK, Jun. 2008.

Posters

1. M. F. Chiang, Z. Ghassemlooy, W. P. Ng and H. Le-Minh, "Future Ultra-high speed Optical Networks: Optical Router based on Slotted-Time-Domain Processing" Booklet of Presentations in 2006 of *Britain's Top Early-Stage Engineers on UK Engineering Research and R&D at the House of Commons (Poster presentation for SET for BRITAIN 2006)*, pp. 14, London, UK, Dec. 2006.

2. M. F. Chiang, Z. Ghassemlooy, W. P. Ng and H. Le-Minh, "Ultrafast all-optical packet-switched router", *UK GRAD Programme Yorkshire & North East Hub, Poster Competition & Network Event*, Leeds, 9 May 2007, Poster No. 15.

3. M. F. Chiang, Z. Ghassemlooy, W. P. Ng and H. Le-Minh, "Ultrafast all-optical packet-switched router", *Northumbria University, CEIS, annual research forum* 2008.

CHAPTER 2 LITERATURE REVIEW OF ALL-OPTICAL ROUTING SCHEMES AND ALL-OPTICAL SWITCHES

2.1 Introduction

Optical fibre is an ideal transmission media for light due to its low power attenuation [60]. However, as optical signals travel through the fibre, there are several impairment factors which distort the signal quality due to the fibre characteristics, such as intermodal dispersion [61], chromatic dispersion [62], polarisation mode dispersion [63] and fibre nonlinearities [64]. Other factors generated by the optical devices, such as the accumulated noise [65], crosstalk [66, 67] also deteriorate the system performance, thus limiting the total throughput of the optical network. Crosstalk (*CXT*) can be classified into inter-channel *CXT* and intra-channel *CXT*: the former one denotes that the undesired signal is at a different wavelength from the desired signal. The later one happens when the undesired and desired signals are at the same wavelength [62]. In order to achieve a low loss and high bit-rate long distance transmission link, each network generation has brought about a fundamental breakthrough and noticeable improvement in system performance. In this chapter, the evolution and topologies of optical network are introduced in Sections 2.2 and 2.3, respectively. The basic architecture of an all-optical packet switching core router and different header recognition scheme are illustrated in Section 2.4. A number of optical switches and all-optical switches are outlined in Sections 2.5 and 2.6, respectively. Finally, Section 2.7 will conclude this chapter.

2.2 Evolution of Optical Network

Fibre-optic communication systems have been deployed worldwide since 1980 and constitute the backbone behind the Internet. A breakthrough came about in 1970s with the developed of compact optical source and low-loss fibres. Following this, terrestrial lightwave systems became commercially available from 1980 onwards. The 1st generation optical systems (networks) developed in 1970s adopted the operation wavelength of 800 nm (known as the 1st window) and used GaAs semiconductor laser and a PIN photodiode as an optical source and receiver, respectively. The bit-rate offered was ~45 Mb/s with a repeater spacing of up to 10 km, far higher than what could have been achieved with the copper cable or radio frequency (RF) based transmission systems [68]. 2nd generation systems were introduced in 1980s where the operation wavelength was shifted to ~1300 nm, where optical fibre exhibits the minimum dispersion and fibre losses are below 0.5 dB/km [69, 70]. It offered higher bit-rates of 100 Mb/s and 1.7 Gb/s with multi-mode fibre and of sing-mode fibre (SMF) with a repeater spacing of about 50 km, respectively [60]. The system based on SMF deployed in 1980 is still forming the worldwide fibre based backbone network. It will take some time before the fibres will be replaced with those operating at higher wavelengths.

The 3rd generation systems came about in late 1980s that adopted operating wavelength of 1550 nm where optical fibre display the minimum loss of 0.2 dB/km but with slightly higher dispersion compared with the 1300 nm wavelength [60, 62]. Using dispersion compensating fibre (DCF) together with the distributed-feedback (DFB) semiconductor laser sources bit-rate in excess of 10 Gb/s with a repeater spacing of about 60~70 km were achieved [60]. 4th generation introduced in early

1990s saw the development and deployment of WDM based technology capable of offering increased total capacity in the orders of magnitudes. The main breakthrough came about by the development of erbium-doped fibre amplifier (EDFA) which made it possible amplification at 1550 nm window, thus being able to transmit high speed data over a long fibre span [60, 71]. In 2003, 373 channels each operating at 10 Gb/s were transmitted over 11000 km of SMF offering a *BL* product of 41000 (Tb/s)-km, a magnificent achievement since the early days of optical fibre communications [60].

5^{th} generation introduced in early 2000 show an increase in the number of wavelengths, thus leading to creation of three new bands: C-band (1530 ~ 1565 nm), as well as L-band (1565 ~ 1625 nm) and S-band (1460 ~ 1530 nm), see Figure 2.1 [72]. Raman based optical amplifiers [73, 74] were readopted since EDFAs are not cable to operate at such a wide spectral band.

WDM technology first introduced in 1980 and became commercially available in 1995 [6, 25, 75]. The enormous capacity of the WDM systems is achieved by having a very narrow channel spacing of 0.4 nm (50 GHz) or less. In principle, the capacity of a SMF is >30 Tb/s [60, 76], therefore a large number wavelength could be used provided the channel spacing is kept to a minimum as well as the gain of optical amplifier is flat across all wavelength. However, in practical system the minimum channel spacing is limited by the inter-channel crosstalk and by the amplifier gain response [60, 76]. Basically, WDM systems are often classified as coarse or dense systems, depending on their channel spacing (typically, channel spacing of > 5 nm and <1 nm for coarse and dense WDM systems, respectively [60]. In most commercially available WDM systems channel spacing is 100 GHz (0.8 nm at 1552

nm [60, 77]. Recently, the International Telecommunication Union (ITU) has specified narrower channel spacing of 25 and 50 GHz for future WDM systems [25, 62].

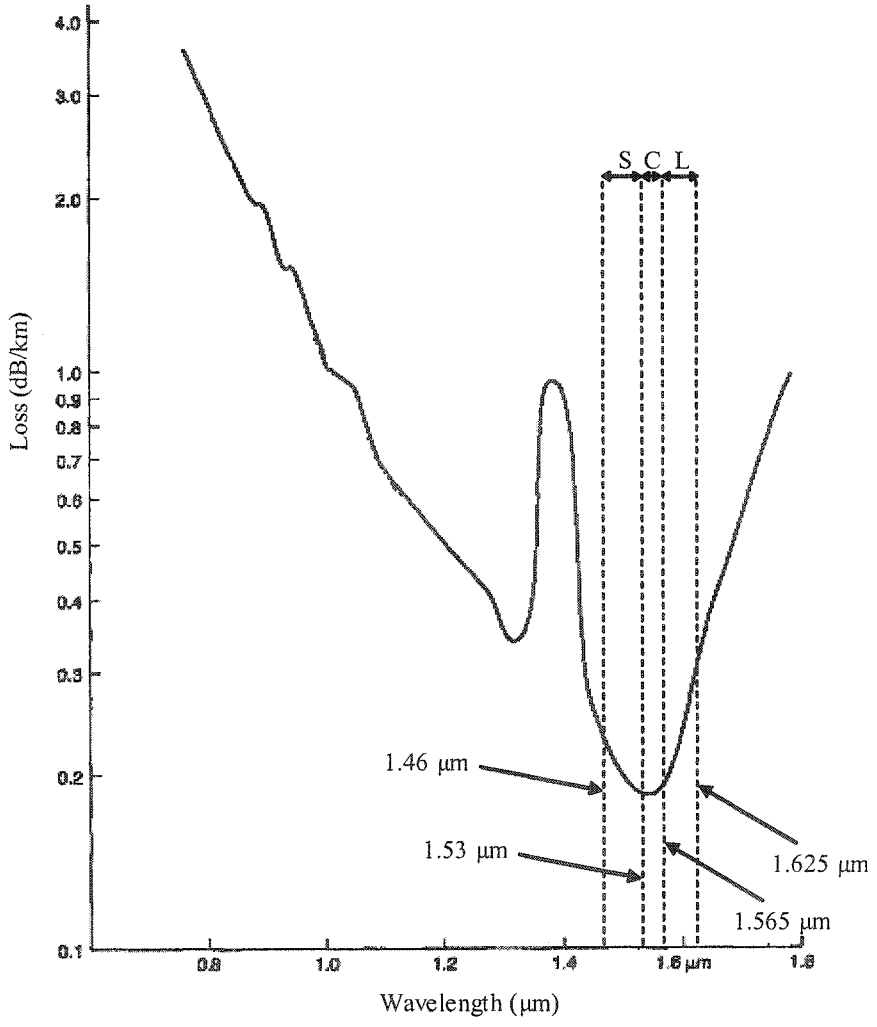


Figure 2.1 Fibre loss (dB/km) versus wavelength (μm)

2.3 Optical Network Topologies

Optical networks can be divided into three groups depending on the area they cover, see Figure 2.2:

- Local-area network (LANs): In LANs, the transmission distance are short such as a campus or a town (normally < 10 km), therefore the fibre losses [60], dispersions [62, 63] and nonlinear effects [64] are not major issues [60]. LANs is often called the access network and is the most closest to the end-users [78].

- Metropolitan-area networks (MANs): MANs interconnects with a number of LANs in big cities. Typically, a ring topology is used in MANs to connect with WANs by the edge nodes (or egress nodes) [60, 79, 80].

- Wide-area networks (WANs): WANs cover a large area such a country or a continent, and are often called as transports networks or core networks [60, 81], where routers (or nodes) in the core networks are located in large metropolitan areas.

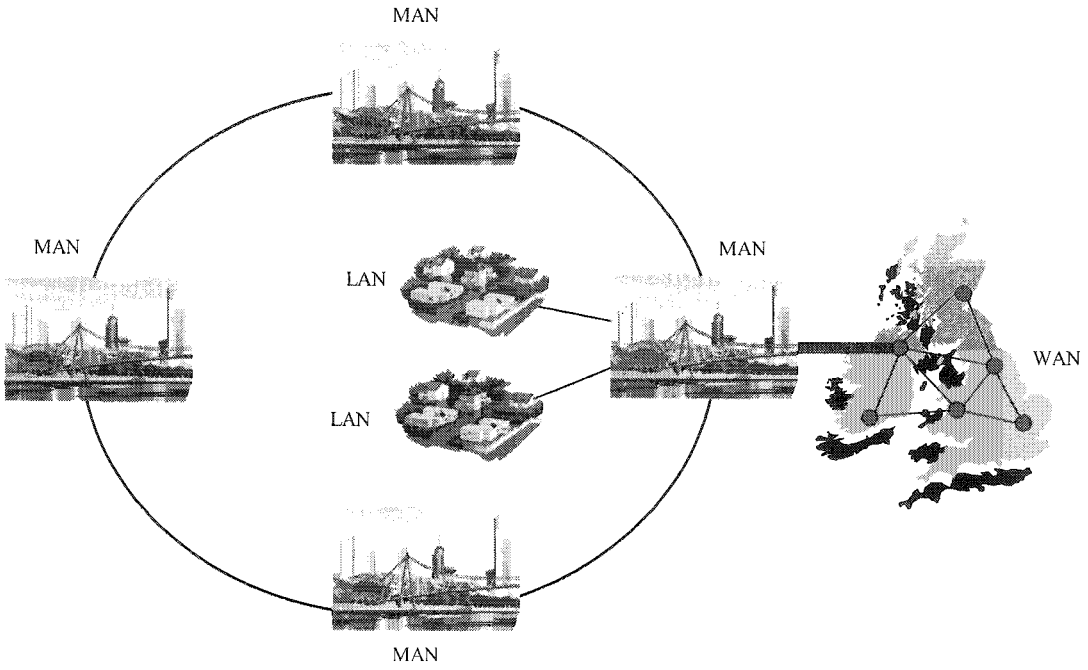


Figure 2.2 A typical optical network showing LAN, MAN, and WAN

In today's optical transport networks, synchronous digital hierarchy/synchronous optical networks (SDH/SONET) are the most important optical standards, the switching processes in SDH/SONET are performed in the electrical domain, which can be slow. SHD/SONET was designed to carry several former digital transmission standard, such as plesiochronous digital hierarchy (PDH) [82] and asynchronous transfer mode (ATM) [83-85]. SONET is used in USA and Canada only, the basic operation bit-rate is 155.52 Mb/s, which is also standardised as synchronous transport module – 1 (STM-1). Nevertheless, SDH is used in rest of the world with a basic operation bit-rate of 51.84 Mb/s (i.e. one third of STM-1), which is also standardised as synchronous transport signal - 1 (STS-1). In STS-1, a frame is 810 octets in size. Each frame is transmitted as 3 octet of overhead followed by 89 octets of payload. This transmission process is repeated nine times until a complete frame is transmitted (i.e. 810 octets) in 125 ms [86, 87].

Optical transport networks such as SDH and SONET are associated with the open system interconnection (OSI) layer 1, see Figure 2.3. The physical layer (i.e. layer 1)

consists of a number of optical components including fibres, transmitters, fibres, amplifiers, and receivers [60, 88].

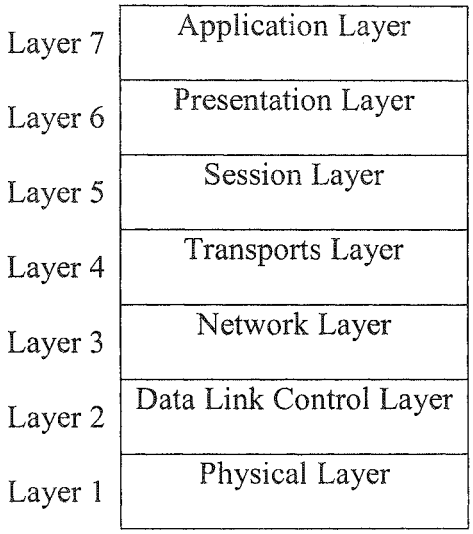


Figure 2.3 The OSI model

Figure 2.4 shows the network architecture of telecommunication system. Typically, the Internet protocol (IP) packets [89-91] sent by the end-users are converted to ATM cells [83-85] before being applied to SDH/SONET transportation circuit and to the backbone WDM systems. Packet over SDH/SONET (PoS) is an alternative scheme for routing IP packets, where IP packets are directly packed into SDH/SONET with no ATM layer at all.

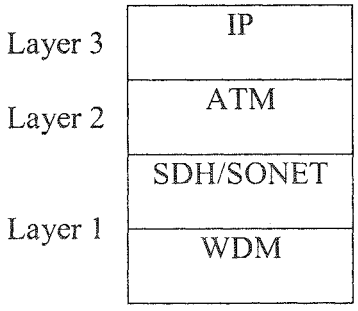


Figure 2.4 The telecommunication core networks architecture [60]

In optical networks to deliver the data across the network to its destination, a number of switching techniques have been proposed as outlined below.

Optical circuit switching (OCS): Currently used SDH/SONET networks are based on circuit switching which are more suitable for voice and real-time traffic [60, 92]. The main advantage of employing OCS is that it uses simple processing and buffering schemes. However the data traffic being the dominant traffic is not optimised for circuit switching [93]. Wavelength routing technology [60, 94] is based on OCS and is currently used in the WDM network, the incoming data at a specific wavelength can be switched to its corresponding output by using OXCs. Although the point-to-point connection is simple, the fibre capacity is not used efficiently. In the wavelength routing, the connection for each hop is established by using a wavelength, called *lightpaht* [95, 96]. Because the capacity is fixed in one *lightpath*, therefore, the resource becomes wasteful while only carrying a small amount of data [97].

Optical code division multiplexing (OCDM) switching: In OCDM switching, routing information is coded by transmitting a series of short pulses named chips within a bit duration. Each switching node is assigned a unique code with "chips". Only a data with the same code can be decode by the unique switching node, the rest of data with different codes will be considered as "noise" to this specific node [98-100]. Basically, there are two methods in OCDM switching: OCDM-label switching and OCDM-path switching. In OCDM-label switching, the routing information is carried by an optical-encoded label at the head of the payload data. In OCDM-path switching, the routing information is carried by the data bits themselves, each individual data bit is optically encoded, this manner is very similar to the wavelength

routing [60, 94], but the routing information is carried by the optical code rather than the wavelength [97].

Optical burst switching (OBS): OBS is a compromise to achieving a truly "*transparent*" optical packet switching. In OBS, many packets are combined into a single burst, and the data and control signals are transmitted on different channel, with the control signals being processed electronically [8, 101, 102]. There are mainly three different methods for transmitting the control signals: Tell-and-wait (TAW), tell-and-go (TAG), and just-enough-time (JET). In TAW scheme [103-105], the source node transmits the control packet first, and waits for the response message from next node, then sends the burst data. In TAG scheme [103-105], the source node transmits the control packet first and immediately transmits the optical burst without waiting for response from next node. In JET scheme [103-105], there is a time delay between the transmission of the control packet and the optical burst data.

Optical packet switching (OPS): OPS is considered as the most desirable switching technique for the next-generation optical network. It is aimed to offer a better efficient utilisation of huge bandwidth providing by fibre. In OPS, fast routing is achievable by employing all-optical switches and all-optical signal processing techniques [24, 62]. However, the main issue in OPS is the lack of optical memory for buffering. Packet header recognition and processing are required in each switching node, thus increasing the node complexity [13, 18, 79, 106-108].

2.4 All-optical Packet Switching Core Router and Header Recognition Scheme

All-optical packet-switched networks are aimed to offer networks with fast switching [109] and more flexible utilisation of the optical bandwidth[62, 110]. However, in order to achieve a truly all-optical packet-switched network, all-optical header processing and address correlation are required at every router. In this section, the basic optical packet format and the fundamental router architecture are illustrated. Several different approaches for optical packet header processing are also introduced in this section.

2.4.1 All-optical packet switching core-router

Optical packets across the core network are assembled by the edge router from MANs. Typically, an optical packet is composed of three parts: the clock, the address and the payload, see Figure 2.5. Clock signal is used for synchronising the timing within a router, and the address information is employed for labelling packet destination. The payload is the real information, which is composed of slow-speed packets having the same destination. Optical packets are delivered from one node to another across the optical core network until reaching their destination nodes, see Figure 1.2. The node/router delivers the packets to different routs based on the information extracted from the packet address.

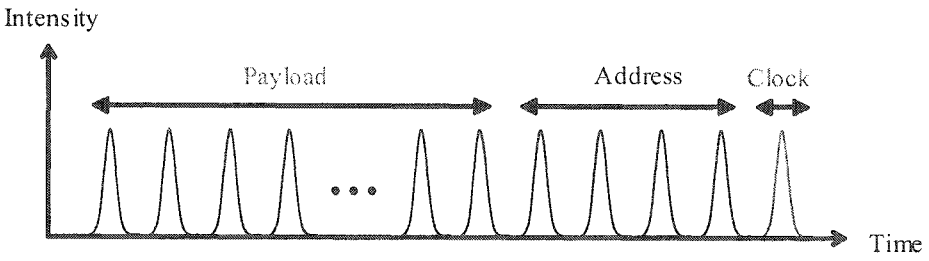


Figure 2.5 A typical format of an optical packet

Figure 2.6 shows the fundamental architecture of a core router in an all-optical packet-switched network. Basically, the router is composed of a number of key modules, such as the clock extraction module for synchronisation, the packet header extraction module for retrieving packet destination, a routing table for storing the routing information (i.e. the shortest path through a number of core routers to its destination), the packet address correlation module for comparing the packet address and routing table thus making the routing decision, the optical switch control module for controlling the optical switches, and optical switches for switching the input packets. There are other optical modules (not shown in the figure) such as reshaping and re-amplification (2R) [111-115] and reshaping, re-amplification and retiming (3R) [116-121] regenerators and optical buffering module [9, 109, 122-128].

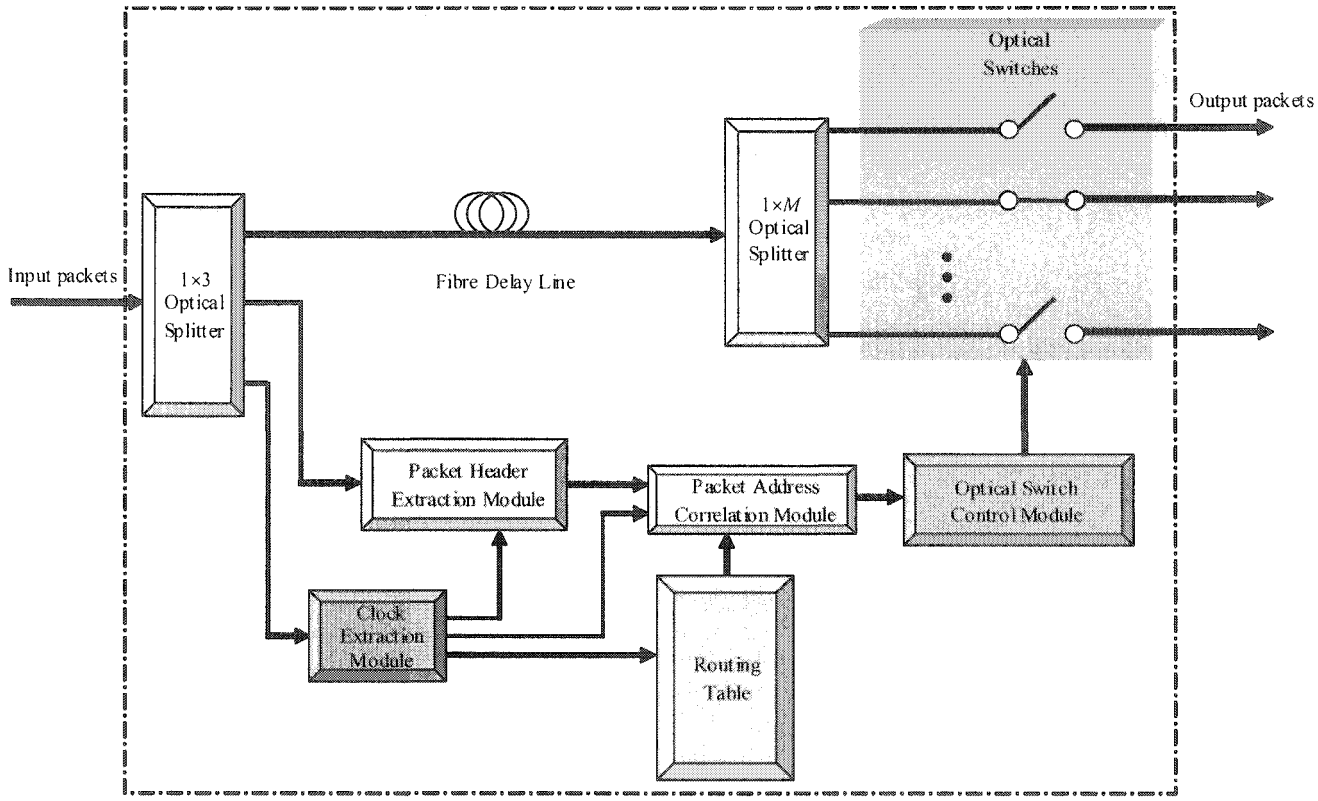


Figure 2.6 A block diagram of an optical packet-switched router architecture

In any network, contention is an issue, which happens when more than one packet are switched to the same output port at the same time. There are three schemes to solve packet contention problem: Optical buffering, deflection routing and wavelength conversion.

Optical Buffering: In traditional electrical packet switching, buffering can be easily achieved by using electrical random-access memory (RAM). However, this is not easily possible in optical domain, there is no optical RAM nowadays. Typically, optical buffers are implemented by using Fibre Delay Lines (FDL). FDL is an easy way to achieve buffering, however it is not flexible enough. This is because FDL does not have random access capability, thus packets can be retrieved only after it is passed through a specific length of fibre. Additionally, a long length of fibre is needed to achieve a short delay time (1 μs delay with 200 m of fibre) [106].

Deflection Routing: By means of forwarding the contention packets to different paths. However, using alternative path usually results in more propagation delay (i.e. require to travel a longer path to its destination) [129-131]. Deflection routing may also result in forwarded packets still circulating within the network, thus requiring more sophisticated protocols to avoid this [106].

Wavelength Conversion: When two packets try to leave an output port at the same time, one of them can be converted to a different wavelength by using a Wavelength Converter (WC) [11, 132-140]. This approach is the most efficient way because it does not delay the signals or use deflection routing [106]. However it requires large numbers of WCs with low noise figures and high extinction ratios, thus maintaining the original bit rates, data format, polarisation, and power.

2.4.2 Packet header and header recognition

Apart from the contention problems, packet header processing in all-optical domain is a major challenge for achieving an all-optical packet-switched router. Packet switching requires signal processing of the packet header address inside the router. It includes packet header (clock and address) extraction and packet address correlation. The conventional header processing is done electrically by transmitting the packet header at a much lower speed than the payload [141-143]. In all-optical label switching (AOLS) [18, 20, 144-147], header recognition is often carried out by transmitting the header and payload in two different dimensions (amplitude, wavelength, phase, or polarisation). However, it is not an easy task to maintain the same polarisation or phase along the transmission path because of the dispersion and nonlinear effects associated with fibre and optical devices [146, 148]. Header

transmitted in different amplitude is also deteriorated by strong power fluctuations due to different power loss/gain characteristic of each optical path along the transmission path [146, 149]. Header with different wavelength would result in different arrival time due to the chromatic dispersion when packet propagates through the network [62, 146]. AOLS have been widely studied for implementing all-optical routing [148, 150-154]. However in most cases, label swapping/modification [15, 155-158] are required at each switching node (i.e. the router), thus increasing the complexity of the router.

A number of all-optical packet header processing and address correlation schemes have been proposed, and could be classified into three schemes:

- Self routing [29, 30, 159-161]: The packet header address is set for directly controlling the on/off status of the output switches. This scheme is less complex because no correlation is carried out between address and routing table. However, as the number of hops increases, the length of the header address also increases proportionally.
- Fibre Bragg grating (FBG) Correlators [27, 31, 162, 163]: A passive device often used in the network. However, as the length of the address increases, the numbers of the required correlators increase exponentially.
- Logic gate correlation: All-optical logic gates, such as XOR [47, 48, 50] and AND gates [49, 164, 165]: are often used to compare the address information with the local routing table. However, the complexity of the address recognition module increases exponentially as the length of the address increases. In IST-LASAGNE (all-optical label swapping employing optical logic gates in network nodes) project [148], the packet label/address is

recognised in all-optical domain by employing a cascade of SOA-MZI structure. Another all-optical address recognition scheme based on logic gates has also been demonstrated experimentally in [14, 22, 154], where the address bits are serially checked by employing a cascaded of XOR operations. However, the numbers of SOA-MZI structures are increasing as the numbers of the address bit increase.

In this thesis, alternative all-optical header processing and header correlation schemes based on PPM routing table (PPRT) are proposed and investigated. The main merits of these schemes are:

- Faster header address processing time
- Employing only a single bitwise AND operation thus avoiding the long recovery time of all-optical logic gates,
- Multiple transmission modes (unicast, multi-cast and broadcast) embedded in the optical layer.

2.5 All-optical Switches

Optical switches are the key elements in an all-optical packet switching node for switching and processing modules. There are a number of optical switching technologies as outlined below:

Bulk mechanical switches: By moving a mirror to reflect the light, or by bending the fibre in the interaction region to switch the light to different output ports. The switching time of bulk mechanical switches is about **10ms** [166].

Micro-Electro-Mechanical System (MEMS) switches: Placing tiny movable mirrors in silicon substrates and controlling it by using electromagnetic or electrostatic method. The switching time of MEMS switches is about **10ms** [167-169].

Bubbles switches: Using a technology which is similar to the inkjet printer, which create bubbles to deflect the light. The switching time of bubble switches is about **10ms**[62, 170].

Liquid crystal switches: Applying a voltage to a liquid cell can change the polarisation of light. By employing polarisation beam splitters and combiners light could be switched. The switching time of liquid crystal switches is about **4ms** [62, 170].

Thermo-optic switches: Temperature is used to change the refractive index of the two waveguides. The phase will be different between the two waveguides, thus resulting in switching. The switching time of thermo-optic switches is about **3ms** [62, 170].

Electro-optic switches: Changing the refractive index in the coupling region by applying a voltage. The switching time of electro-optic switches is about **10ps** [62, 170].

2.6 Ultrafast All-optical Switches

All optical switches such as ultrafast nonlinear interferometer (UNI), Terahertz optical asymmetric demultiplexer (TOAD) [171, 172], and Mach-Zehnder

interferometer (MZI) [173-175] are based on the concept of cross-phase modulation (XPM) of SOA, where the phase difference between signals results in destructive or constructive interference, thus achieving switching functions. All-optical switches are widely employed to carry out the routing decision in optical domain due to their ultrafast switching time (**< 1ps**) [106, 176].

2.6.1 Ultrafast nonlinear interferometer (UNI)

The basic structure of an UNI is shown in Figure 2.7. The input signal of UNI is first split into two orthogonal polarisations by a polarisation sensitive optical isolator (PSI) (i.e. PSI 1) [54, 106]. A time delay between the two orthogonal polarised signals is then generated by passing a polarisation maintaining (PM) birefringent fibre [177]. This is because in a birefringent fibre, the refractive indices for two orthogonal polarised signals are largely different thus inducing a time delay between those two polarised signals. The delay is determined by the length and property of the PM birefringent fibre. By injecting a high power control pulse (CP) between the two orthogonal polarised signals before entering SOA, a phase difference is introduced between the two polarised signals. Signal polarisations are rotated due to different phase shift.

Finally, after passing through the second PM bifringent fibre, two different polarised signals are retimed to overlap, which can be separated by the second PSI (i.e. PSI 2). The second PSI is set at 45° to the orthogonal signal polarisations. The CP is eventually filtered out by an optical filter in the output port. With the presence of CP, the input signal is emerged from the output port. The main drawback of UNI is that it requires a length of PM birefringent fibre (>15 m) for inducing the time delay between two polarised signals, thus having low integratablity [106].

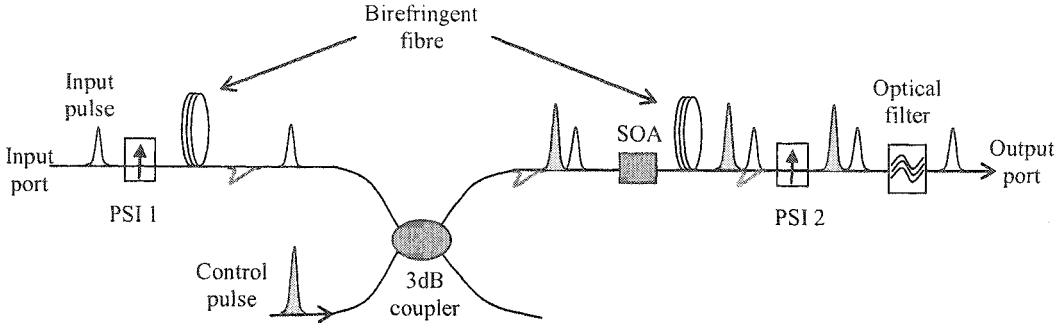


Figure 2.7 The structure of UNI [106, 178]

2.6.2 Terahertz optical asymmetric demultiplexing (TOAD)

Nonlinear optical loop mirror (NOLM) switches were first proposed in 1988 [179-181]. The switching window (SW) for NOLM can be made very narrow (<0.7 ps), and therefore NOLM switches can switch very fast. However, because NOLM only depends on the weak nonlinear interaction in the fibre, it requires higher power control pulses and long lengths of fibre (>100 m) to ensure phase shift. Despite NOLM providing a very fast switching time, it is not commercially used due to its poor integratablity. In 1993, TOAD switches were proposed to improve its integratablity [106, 182, 183]. TOAD is composed of a fibre loop, two 3-dB couplers, a SOA, an optical circulator, and two optical filters, see Figure 2.8. The input signal is first split into two parts with different propagation directions: clockwise (CW) and counter clockwise (CCW). The CP is used either at a different polarisation or a different wavelength to distinguish from the input signals. Without CP, both CW and CCW signals experience the same phase and recombine at the 3-dB coupler, thus emerging from the reflected port. With the presence of CP, CW and CCW signals experience a different phase shift thus existing from the output port. The switching window width of TOAD is determined by the position of SOA within the fibre loop. The CP is eventually filtered out by the optical filters in the output and reflected ports.

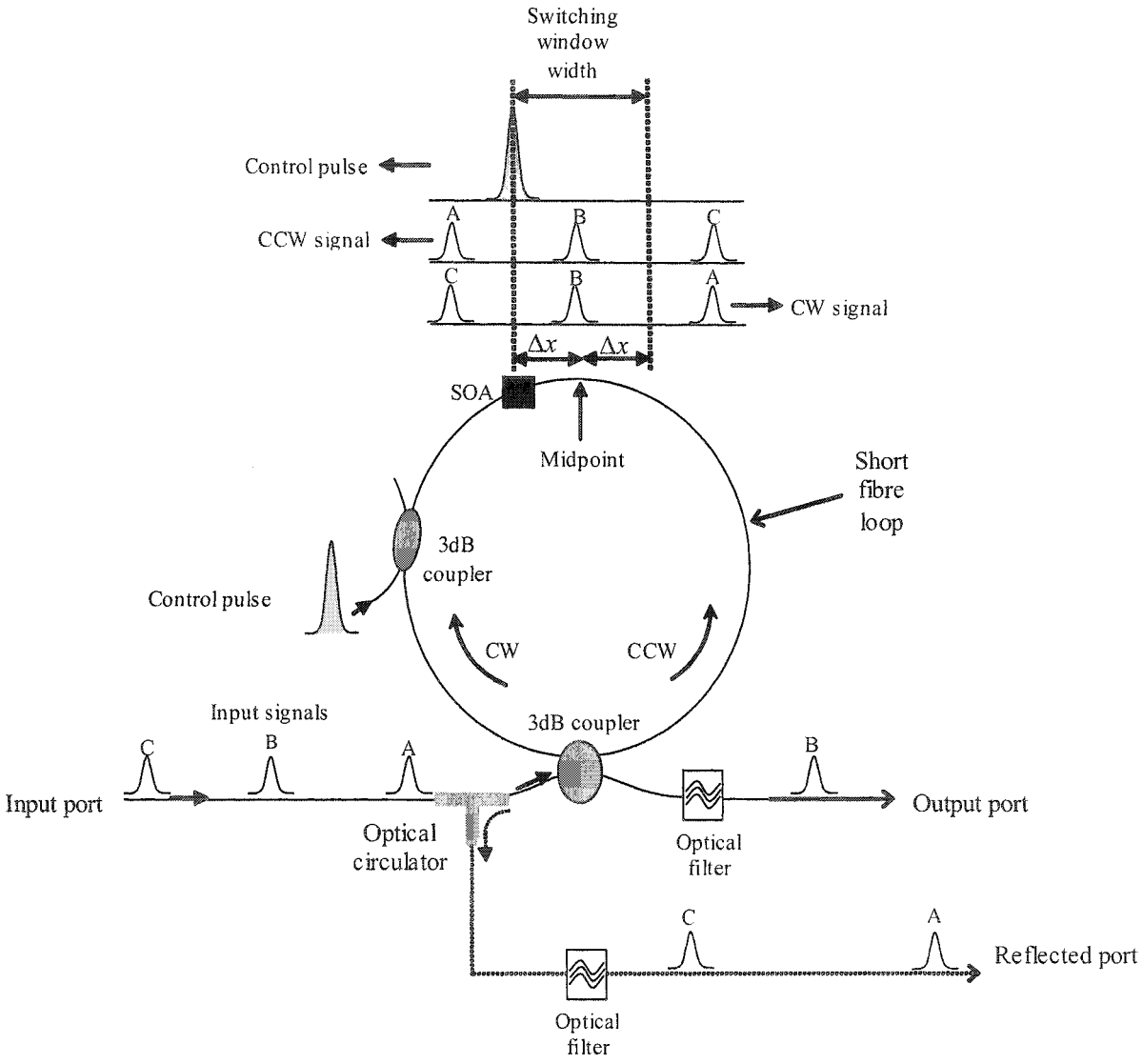


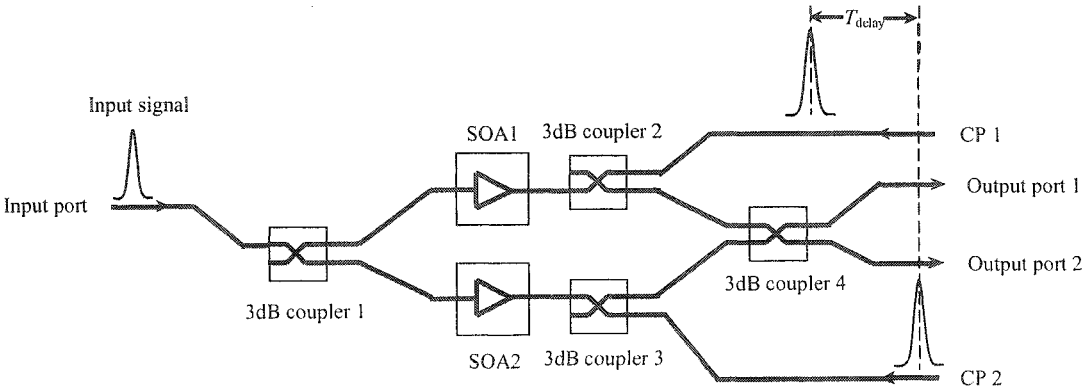
Figure 2.8 The structure of TOAD [178]

2.6.3 Mach-Zehnder interferometer (MZI)

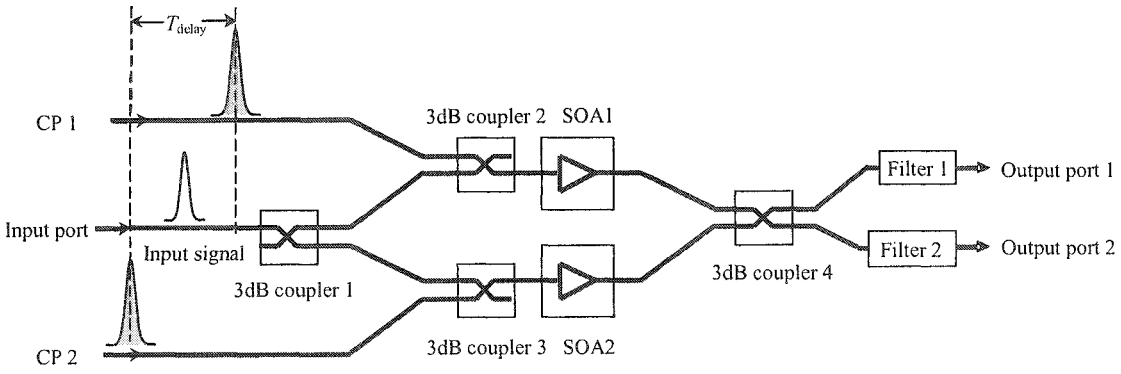
The MZI switch is first proposed in 1993 [176, 184, 185]. In general, there are mainly two types of MZI structure: Colliding-Pulse Mach-Zehnder (CPMZ) and SMZ, see Figure 2.9(a) and (b), respectively. Basically, the MZI is a two arms optical waveguide [186] with two SOAs and a number of 3-dB couplers. The input signal is first split to the upper and lower arms. Without CP, signals from two arms experience the same phase shift and recombine at the output 3-dB coupler (i.e. coupler 4) thus

exiting from the output port 1. By applying CPs into these two arms at different time, the signals from two arms experience a different phase shift thus emerging from the output port 2. Figure 2.9(c) shows the SW created by applying CPs, the width of the SW (i.e. T_{sw}) is equal to the delay time between CP1 and CP2 (i.e. T_{delay}). Input signals within the SW will be switched to the output port 2.

In CPMZ, the input signal and CP propagate in counter directions. As a result, no output filters are required. In SMZ, the input signal and CP propagate in the same direction, therefore additional output filters are imperative for separating the CP and signal. More operation principles will be discussed in Section 3.3.



(a)



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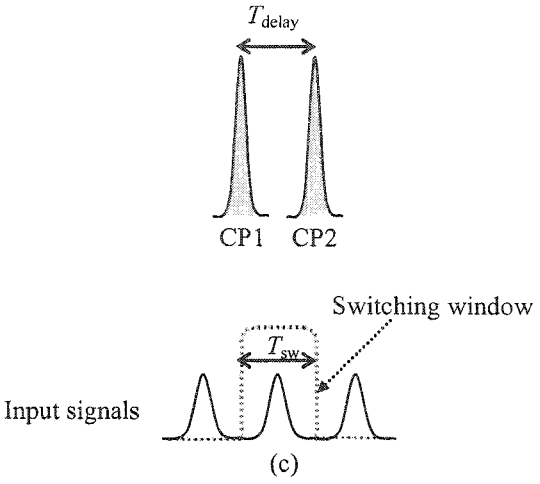


Figure 2.9 Two basic structures of MZI switch: (a) CPMZ (b) SMZ, and (c) MZI switching window [178]

2.7 Summary

This chapter introduced the evolution history and the topology of today's optical networks. The development of the WDM technology has significantly increased the overall throughput of optical fibre communications. However, the fibre capacity is still being under utilised. OPS has been proposed to offer networks with fast switching and more flexible utilisation of the fibre bandwidth. In order to achieve a truly all-optical packet-switched network, packet header recognition and processing are required in each router. In this chapter the fundamental router architecture was presented, and the weaknesses of several different approaches for optical packet header processing were also discussed. Moreover, different types of switches and all-optical switches were introduced, where the latter switches employ the nonlinear effects of SOA, thus achieving fast switching operation (switching time < 1 ps). Three main nonlinear effects of SOA and some SMZ-based applications will be introduced in the next chapter.

CHAPTER 3 SEMICONDUCTOR AMPLIFIER, SYMMETRIC MACH-ZEHNDER AND ITS APPLICATIONS

3.1 Introduction

Optical amplifiers can be classified into two groups: fibre amplifiers [187] and waveguide amplifiers [188, 189]. Fibre amplifiers such as EDFAs [71, 190, 191] and Raman amplifiers [192, 193] are widely used in long-haul transmission due to their polarisation insensitive, high output saturation gain, low gain dynamics, and low noise figure. Nevertheless, waveguide amplifiers such semiconductor amplifiers (SOAs) and Erbium doped waveguide amplifiers (EDWAs) [194, 195] are mainly used for all-optical signal processing such as wavelength conversions and switching due to their compact size, strong nonlinearities with fast dynamic, and low cost compared to fibre amplifiers [188]. All-optical switches employing SOA's nonlinearities are widely used for all-optical signal processing and switching purpose due to their ultrafast switching time. Among different types of all-optical switches, SMZ is used as the building block in the proposed router due to its short and square switching window and compact size [184].

In this chapter, the fundamental structure of SOA and three nonlinear effects of SOA are introduced. In Section 3.3, the operation principle of SMZ is presented and explained. An-optical serial-to-parallel converter based on SMZs is also investigated in Section 3.4. Furthermore, other applications based on SMZs, such as all-optical logic gates and high contrast ratio 1×2 all-optical switch are introduced and

investigated in Sections 3.5 and 3.6, respectively. Finally, an-optical three-input AND gate is proposed in Section 3.7.

3.2 Semiconductor Optical Amplifier

Figure 3.1(a) and (b) show the structure of SOA. Basically, SOA is a semiconductor laser but with anti-reflections in both end faces. When an SOA is DC biased through the mental contact, the input optical signals travel through the optical waveguide between the p-n junctions (i.e. the active region) will be amplified by means of stimulated emission [196]. Generally speaking, SOAs are capable of amplifying signals from 1310 nm to 1550 nm bi-directionally with the gain of ~ 30 dB [197]. Comparing it with the EDFA, SOAs have a small size and high nonlinear characteristics, thus making them an attractive building block in all-optical signal processing.

There are two most widely used types of SOA active layer structures: multi-quantum-well (MQW) [57, 198] and a bulk SOA [57]. Generally speaking, MQW SOAs have higher gain, a larger saturation power, and a lower noise figure (NF) compared to the bulk SOAs [199]. However, bulk SOAs can achieve larger optical confinement factor as well as larger phase-to-amplitude coupling factor, thus having stronger nonlinear effects due to the simpler manufacture process [199]. As a result, bulk SOAs might be suitable for applications requiring strong cross phase modulation. In this work bulk SOAs are used.

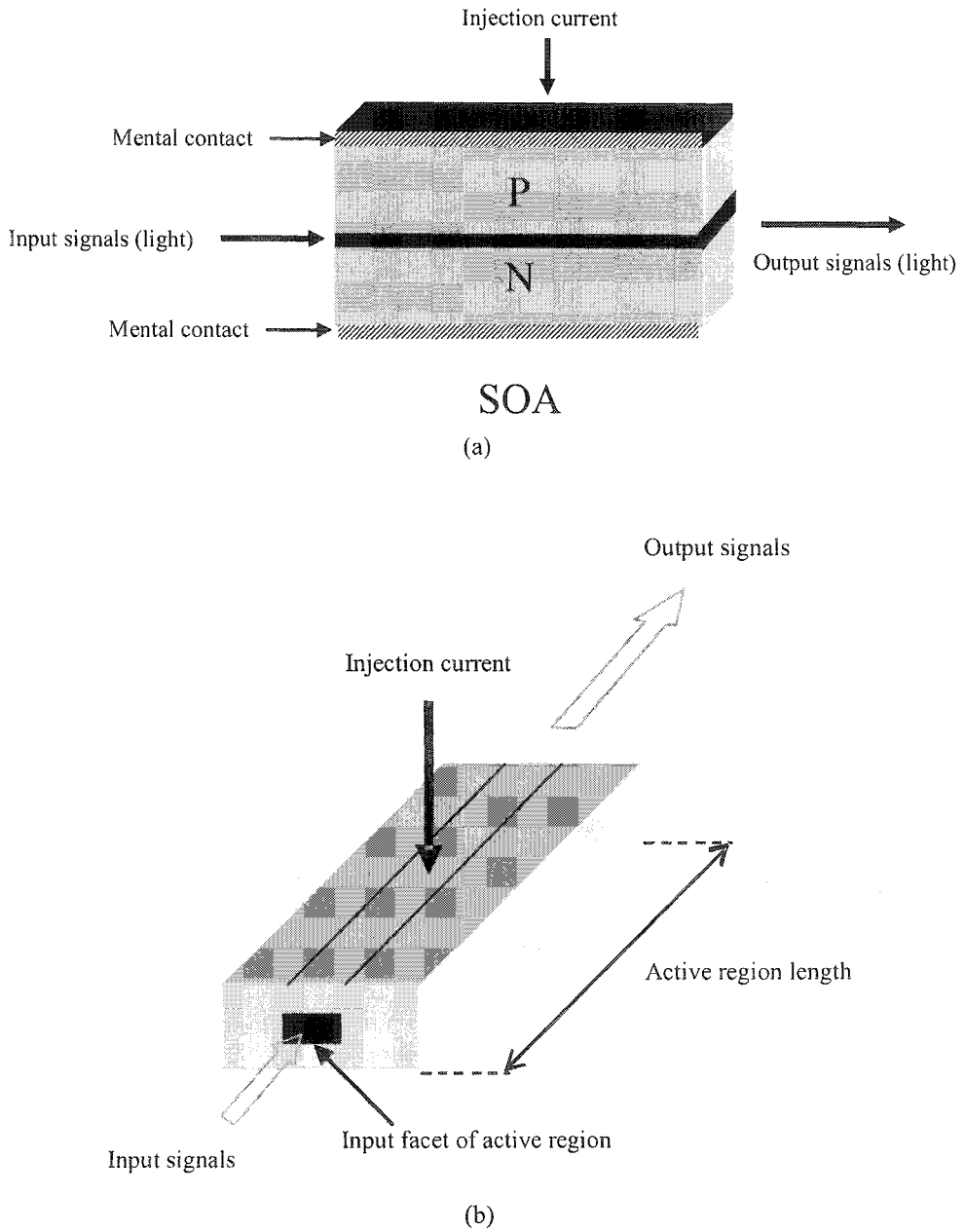


Figure 3.1 (a) Diagram of a SOA and (b) p-n junction in SOA

3.2.1 SOA principle

The injection current source will energise the electrons in the valence band (which is also called the carriers). These energised electrons occupy in the conduction band (CB) and leave holes in the valence band (VB) of the active region. Figure 3.2 shows three radiative phenomena in the SOA [57]:

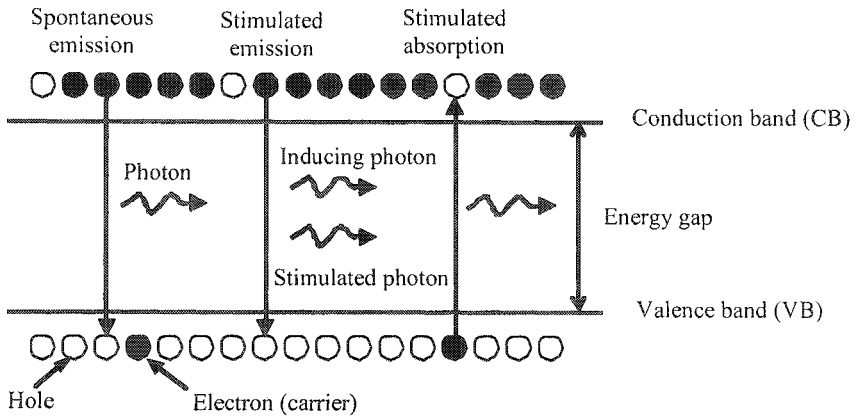


Figure 3.2 Three radiative phenomena in the SOA [200]

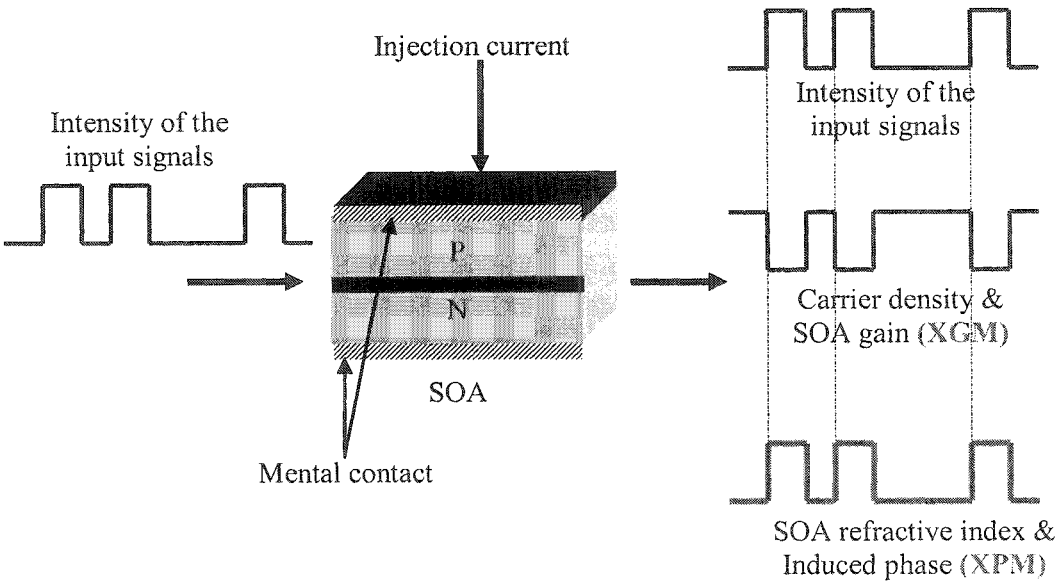
- **Stimulated absorption:** This is a loss process of the incident photon. An incident light (photon) with sufficient energy can stimulate an electron from the VB to the CB thus reducing the number of incident photon. The occurrence of stimulated absorption is more frequent when there are many incident photons and high electron density in the VB [201].

- **Stimulated emission:** When SOA is not DC biased, the electron density in the VB is much higher than in the CB, and as a result less photon emerges at the SOA output due to the stimulated absorption process, thus appearing as with no amplification gain. Once the injection current is sufficiently high, the carrier population in the CB exceeds that in the VB. In this case, stimulated emission process is greater than the stimulated absorption process. As a result, SOA has an optical gain. Stimulated emission is a process that an incident light (photon) with a suitable energy causes stimulated recombination of a CB carrier with a VB hole. In this recombination, electron loses its energy by releasing a simulated photon which has the same phase, wavelength and direction with the original incident photon [57]. Note that, both of the original photon and the simulated photon can induce more stimulated transitions.

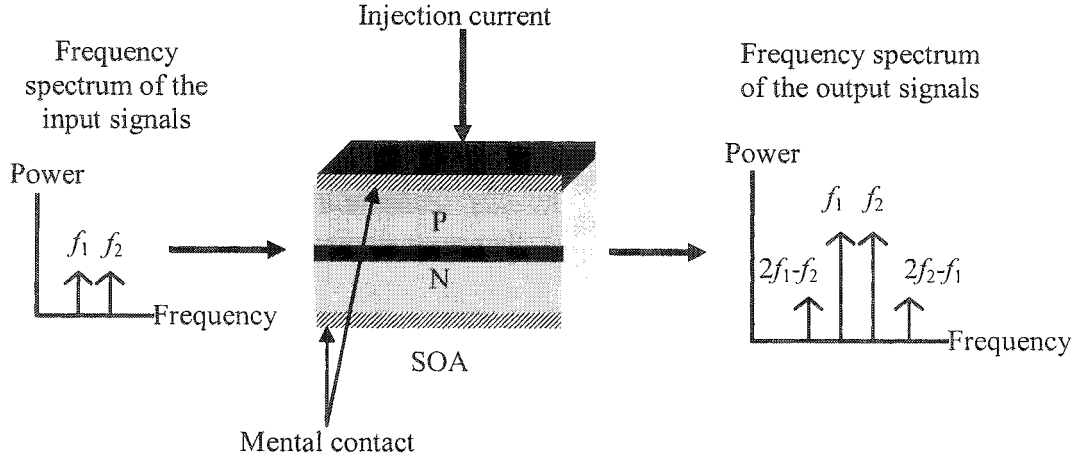
- **Spontaneous emission:** Is an unavoidable process which results in amplified spontaneous emission (ASE) noise [60]. In this process, the carriers in CB spontaneously recombine with the VB holes but emit a photon with a random phase and direction over a wide range of wavelength. The probability of spontaneous emission is increased with a high electron (carrier) density in the CB [201].

3.2.2 SOA nonlinearities

SOA is often used for optical signal processing because of its nonlinear characteristics. Due to the stimulated emission process, the excited electrons in the CB are depleted, and as a result the electron density (carrier density) is decreased. The reduction (drop) of the carrier density in the CB leads to three nonlinear effects, see Figure 3.3:



(a)



(b)

Figure 3.3 SOA nonlinearities (the output responses are simplified for clarity): (a) XGM & XPM and (b) FWM

- **Cross-gain modulation (XGM):** Light entering the SOA will reduce the carrier density in the active region. The carrier population in the active region is proportional to the SOA gain. Therefore, as the power of the incident light increases, more carriers in the CB is depleted, thus decreasing the SOA gain. The drop in the SOA gain will affect all signals propagating through it.

- **Cross-phase modulation (XPM):** The input light signal will reduce the carrier density within the active region causing a temporal refractive index change, thus inducing a temporal optical phase change (i.e. XPM). This phase change will be imprinted onto signals concurrently propagating through the SOA. [202].

- **Four-wave mixing (FWM):** The interactions between two or more input signals with different wavelengths result in generation of new output frequency components (i.e. FWM) [134, 203]. By taking advantage of FWM, the desired pattern can be modulated at a different frequency. A number of applications such as all-optical wavelength converters [134, 138, 204-206] and all-optical logic gates [38, 164, 207, 208] have been developed based on the FWM.

3.3 Symmetric Mach-Zehnder Switch

Among a range of all-optical switch configurations, the SMZ structure provides a short and square switching window (SW), a compact size, thermal stability and low-power operation [184].

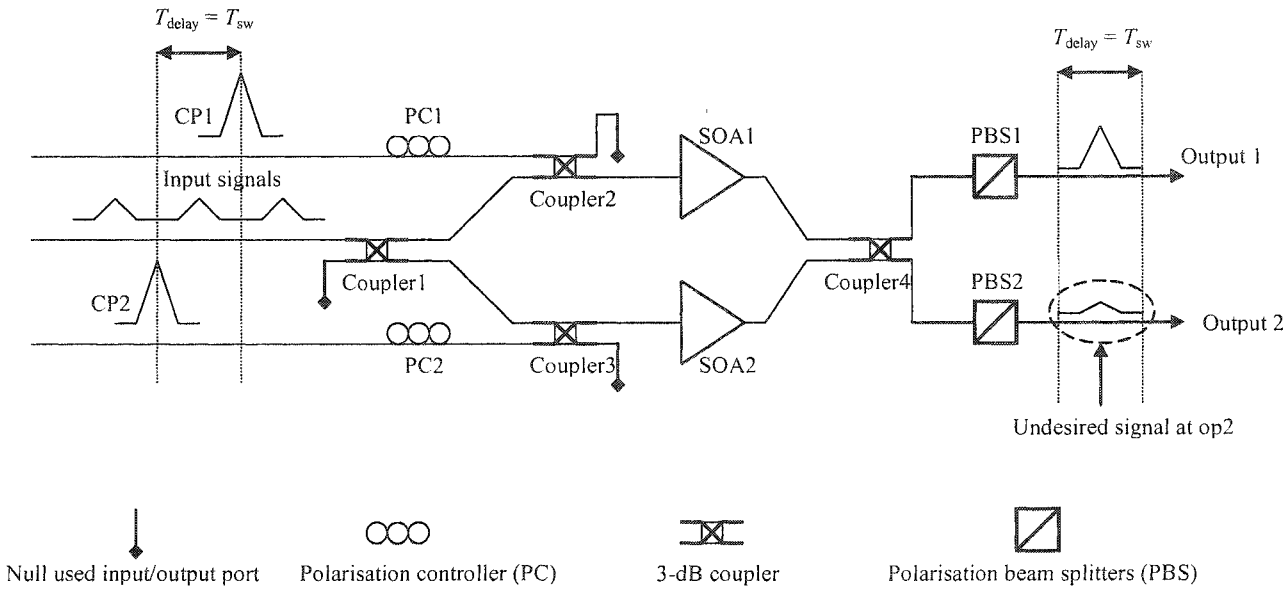


Figure 3.4 SMZ structure

Figure 3.4 shows the structure of SMZ switch, which is composed of two SOAs, four 3-dB couplers, two polarisation controllers (PCs), and two polarisation beam splitters (PBSs). By means of injecting two high power control pulses (CP1 and CP2) into SOA1 and SOA2, respectively at different time, the induced phase difference between two arms enables the SMZ either to be switched ON or OFF, thus creating a SW. For example, with no CPs, the upper and lower arms of the SMZ are in the balance state and the input signal emerges from the output2. Applying CP1 changes the gain characteristics of the SOA1, as a result the SMZ becomes un-balanced and the input signal emerges from output1. However, the undesired signal will also emerge from output2 due to the incomplete destructive interference, more discussions can be found in Section 3.6. By applying CP2, delayed by T_{delay} with respect to CP1, to the SOA2 the SMZ once again becomes balanced and therefore the input signal emerges from output2. To be able to distinguish between the control and data pulses at the output ports, CPs are launched at orthogonal polarisation with respect to the data pulses by using two PCs. At the output ports, two PBSs are used to separate CPs from the data pulses [209].

The SOA gain G is approximately given by [199]:

$$G=e^{\Gamma(g_m-\alpha)L}=e^{\Gamma[g_0(N-N_0)-\alpha]L}=e^{\Gamma\left[g_0\left(\frac{\eta_i I\tau_s}{eLwd}-N_0\right)-\alpha\right]L}, \tag{3.1}$$

where Γ is the confinement factor, g_m is the material gain, α is the optical loss, g_0 is the gain coefficient, I is the injection current, N is the carrier density at the operating current I, N_0 is the carrier density at transparency, η_i is the current injection efficiency, τ_s is the spontaneous recombination lifetime of the carriers, e is the electronic charge, and L, w, d are the length, width, and thickness of the active region of the SOA.

The power at output1 and output2 of the SMZ are given as [210]:

$$P_{out,1}(t) = \frac{1}{8} P_{in}(t) \cdot \left[G_1(t) + G_2(t) - 2\cos(\Delta\phi)\sqrt{G_1(t) \cdot G_2(t)} \right], \tag{3.2}$$

$$P_{out,2}(t) = \frac{1}{8} P_{in}(t) \cdot \left[G_1(t) + G_2(t) + 2 \cdot \cos(\Delta\phi)\sqrt{G_1(t) \cdot G_2(t)} \right], \tag{3.3}$$

where $P_{in}(t)$ is the power of the input signal and $\Delta\phi$ is the phase difference of the input signals between the upper and lower arms of the SMZ given by [210]:

$$\Delta\phi = -0.5\alpha_{LEF} \ln(G_1 / G_2), \tag{3.4}$$

where α_{LEF} is the linewidth enhancement factor.

The width of the SW profile is given by [210]:

$$W(t) = \frac{1}{4} \cdot \left[G_1(t) + \cdot G_2(t) - 2 \cdot \cos(\Delta\phi) \cdot \sqrt{G_1(t) \cdot G_2(t)} \right]. \tag{3.5}$$

Further explanations of SMZ in practical system could be found in APPENDIX – B.

3.4 All-Optical Serial-to-Parallel Converter (SPC) Based on SMZ

In packet switched networks, all-optical serial-to-parallel conversion (SPC) is essential for address recognition. A SPC using surface-reflection all-optical switches has been proposed in [211], but it requires a number of micro lens and mirrors. In this section, a SPC based on the SMZ configuration is proposed. Crosstalk is an important issue when signals are propagating through the networks. The accumulated crosstalk due to different elements and nodes will result in increased power penalty at receiver thus degrading the system bit-error-rate (BER) performance [62, 212]. SMZs are used as the fundamental building block in the proposed router, see CHAPTERS 4-6. Here,

the crosstalk characteristics of a SPC based on SMZ are investigated to achieve SMZ switching with a low *CXT* performance.

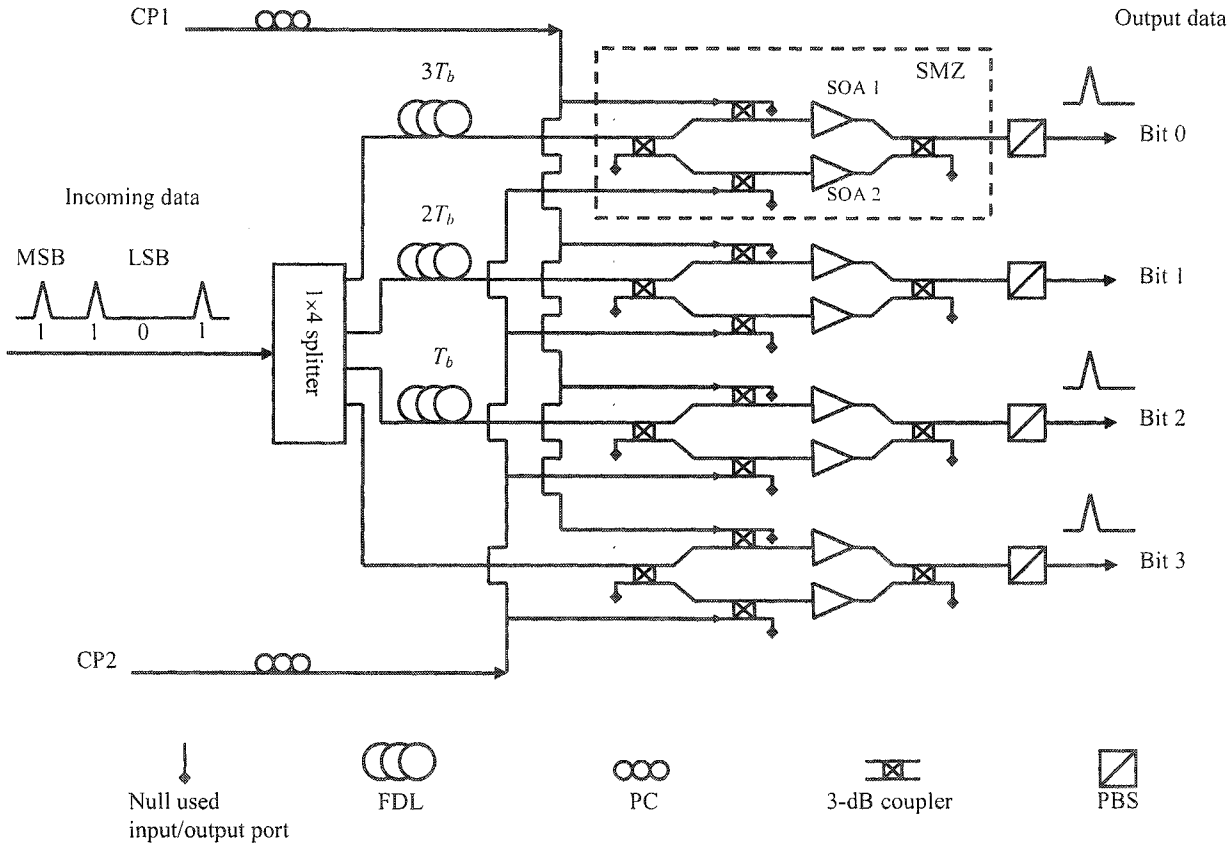


Figure 3.5 SPC system block diagram

Figure 3.5 shows the block diagram of a SPC, which is composed of a number of SMZ modules, fibre delay lines (FDLs), 1×4 splitter and a number of 3-dB couplers, PCs, and PBSs The incoming data signal is split using a 1×4 splitter before being applied to the inputs of the parallel SMZ modules. The first 3 outputs are delayed by $3T_b$, $2T_b$ and T_b, respectively for selecting the bit 0 ('1'), bit 1('0'), bit 2 ('1') and bit 3 ('1') bits of the input signals. Introducing correct delay is essential in order to ensure that the data signal sits in the centre of the SMZ SW. Identical CP1 is applied to all SMZs prior to the target data signals in order to saturate the SOAs in the upper arms, thus turning on the switch. After T_{sw} delay time, CP2s are applied to the SMZs to

saturate the SOAs in the lower arms, thus turning off the switch. Polarisation controller (PC) is used to distinguish between CP1 and CP2 and the data pulses. Polarisation beam splitters (PBS) at the output ports of the SPC are used to separate the data signals and CPs. The numbers of SMZs is equal to the numbers of serial bits being converted.

With a high power CP applied to the SMZ, the SOA gain saturation is abruptly dropped (i.e. ΔG). However, once CP has exited the SOA, the gain recovery is rather slow (orders of magnitude higher than the saturation time), see Figure 3.6(a). Note the slight difference in the gain profiles for SOA1 and SOA2 in the recovery region (i.e. Δg), which results in an uncompleted cut-off edge of the SW profile, see Figure 3.6(b). As a consequence, the undesired signals are also switched to the output1 of SMZ (see Figure 3.4), which are main source of the intra-channel *CXT* defined as the ratio of the transmitted energy of one non-target channel to the transmitted energy of a target channel [174]:

Here the intra-channel *CXT* is defined as the ratio of the transmitted energy of one non-target channel to the transmitted energy of a target channel [209]:

$$CXT = 10\log_{10}\left(E_{nt}/E_{t}\right), \tag{3.6}$$

where E_{nt} and E_t are the output signal energy due to the non-target and target channels, respectively, expressed by [209]:

$$E_{nt} = \int_{t_c+T_{b/2}}^{t_c+T-T_{b/2}} W(t)p_p(t-t_c)dt\,, \tag{3.7}$$

$$E_t = \int_{t_c - T_b/2}^{t_c + T_b/2} W(t) p_p(t - t_c) dt \,, \tag{3.8}$$

where $p_p(t)$ is periodic train of data signal, T_b is the bit slot duration, t_c is the centre of the switching window, T is the channel period, and $W(t)$ the width of the SW profile is given is given in (3.5):

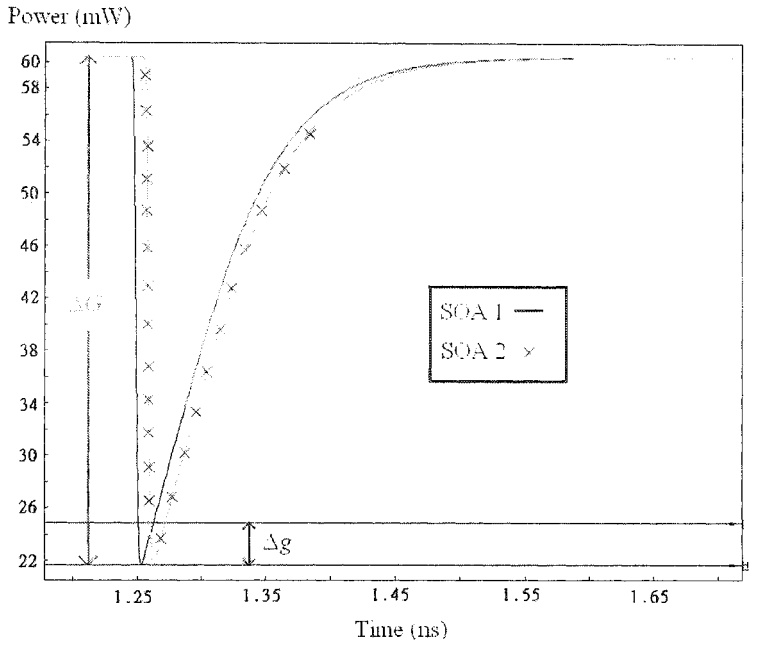
In this simulation, optical pulse with sech^2 shape is used because experimental evidence suggested that pulse from gain-switched semiconductor laser are more close to sech^2 shape rather than Gaussian shape [213].

The energy of the optical pulse with sech^2 shape is calculated as follows [214]:

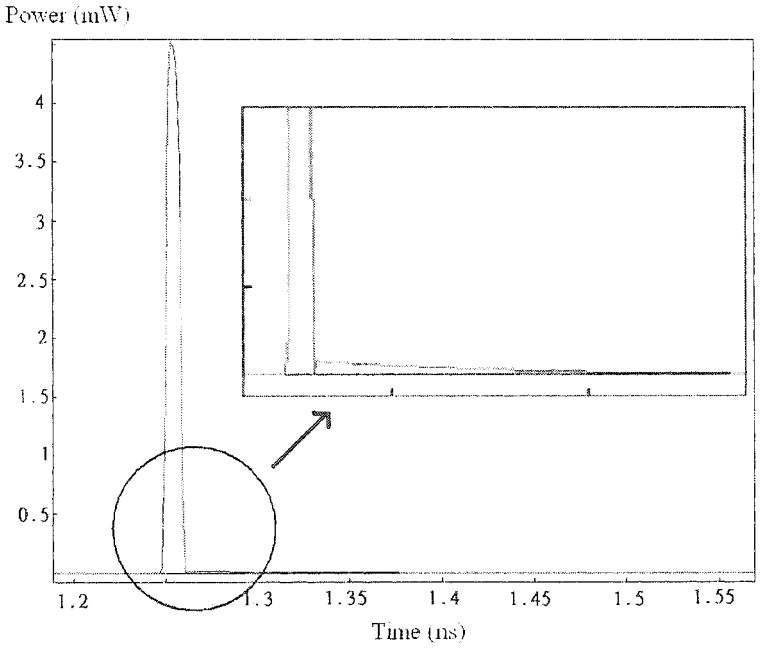
$$E_{\text{sec}\,h^2} = \frac{P_{\max} \times \tau_p}{0.88} \,, \tag{3.9}$$

where $E_{\text{sech}}{}^2$ is the energy of the optical pulse with sech^2 shape, $P_{\max}$ is the peak power of the pulse, τ_p is the FWHM of the pulse.

As a result, the *CXT* ratio could be calculated by measuring the peak power of the desired and undesired signals.



(a)



(b)

Figure 3.6 (a) The gain profiles of SOA1 and SOA2, and (b) the SW profile of SMZ output1

The simulation is carried out by using the Virtual Photonics simulation package (VPI^{TM}), also see APPENDIX – A. All the main parameters used are shown in Table 3.1 and Table 3.2 [21]. Note that, the SOA model used in the thesis is only valid for optical pulses of tens of picosecond duration [215]. For short pulses, the pulse shape

will be distorted and the spectrum of the pulse will be shifted due to the SOA gain saturation [216]. The feasibility of SMZ switching by employing short pulses with FWHM of 2 ps has been demonstrated experimentally in [217-219]. Addtionally, another benefit of employing SMZ is that the induced frequency chirp can be omitted, since chirp is proportion to the rate of index change, which can be cancelled by the two-arm SMZ configuration [220].

Table 3.1 SOA simulation parameters

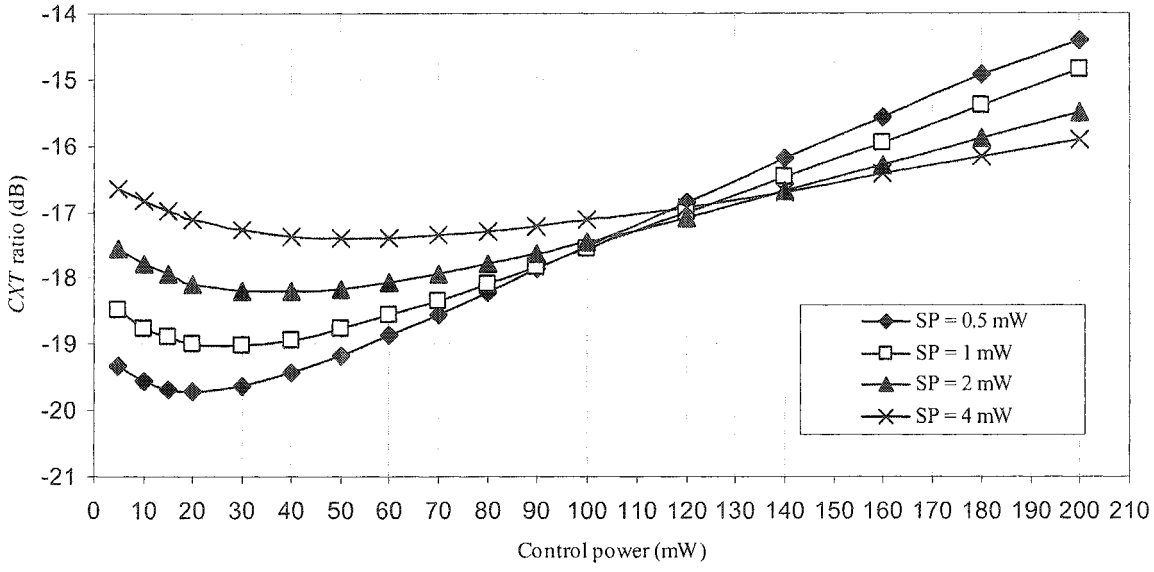
Parameters	Values
Iniect current	0.15 A
Length	500×10^{-6} m
Width	3×10^{-6} m
Height	80×10^{-9} m
Confinement factor	0.15
Differential gain	2.78×10^{-20} m^2
Carrier density at transparency	1.4×10^{24} m^{-3}
Initial carrier density	3×10^{24} m^{-3}
Linewidth enhancement factor	4
Recombine constant A	1.43×10^{8} s^{-1}
Recombine constant B	1×10^{-16} m^3s^{-1}
Recombine constant C	3×10^{-41} m^6s^{-1}

Table 3.2 Signal and control pulses default parameters

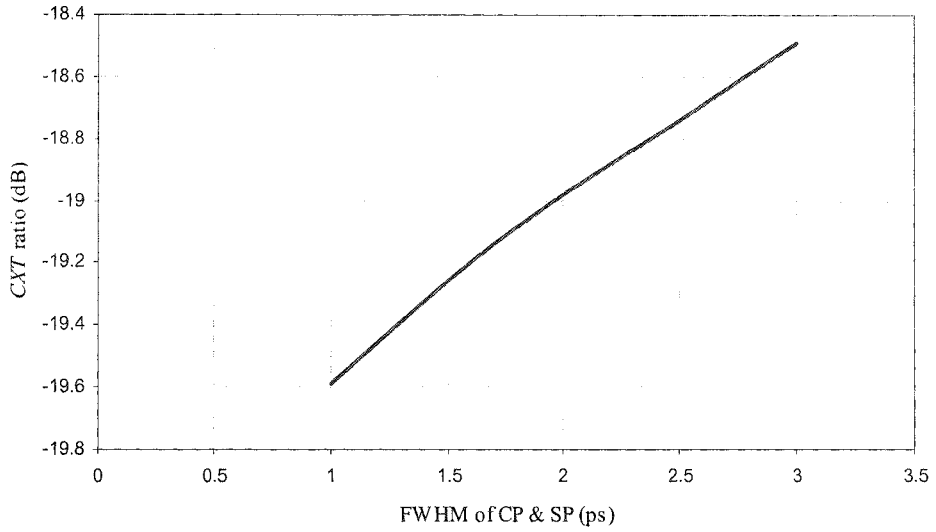
Parameters	Values
Operation bit rate R_b	80 Gb/s
Wavelength of signal & control pulse	1554 nm
Signal & control pulse widths (FWHM)	2 ps
Width of the switching window T_{sw}	10 ps
Signal pulse power/energy	1 mW/2.27 fJ
Control pulse (CP) power/energy	20 mW/45.45fJ

Figure 3.7(a) shows *CXT* against the CP power for different values of input signal power (SP). The lowest *CXT* is achieved when both SP and CP are at low values. E.g., for CP and SP of 20 mW and 0.5 mW, respectively the *CXT* is about –20 dB. In amplified systems, intra-channel *CXT* of -20 dB results in ~1 dB power penalty at the

receiver [62]. Other all-optical SPC reported in [221] offers a low *CXT* of -30dB, however this scheme requires a two-dimensional microlens array, two optical lens, and two surface-reflection all-optical switches. Note, that the output *CXT* of SPC won't affect the router performance. This is because in this work the output parallel bits are only used as CPs to switch a single clock bit. However for CP > 120 mW, the best *CXT* is achieved for SP of 4 mW. Note that the minimum level of *CXT* not only increases with the SP power but is also achieved at higher values of CP power. This is because higher power CPs contribute to the increased gain saturation of the SOA, and consequently resulting in a higher gain difference in the recovery region, thus leading to a higher *CXT*. *CXT* changes very little (about 1 dB) with the duration of the CP and SP, provided they have the same full width at half maximum (FWHM), see Figure 3.7(b). This is because *CXT* mostly depends on the pulse power rather than pulse width. Small increase in the *CXT* is due to the higher average power of the non-target pulses residing within the SW.



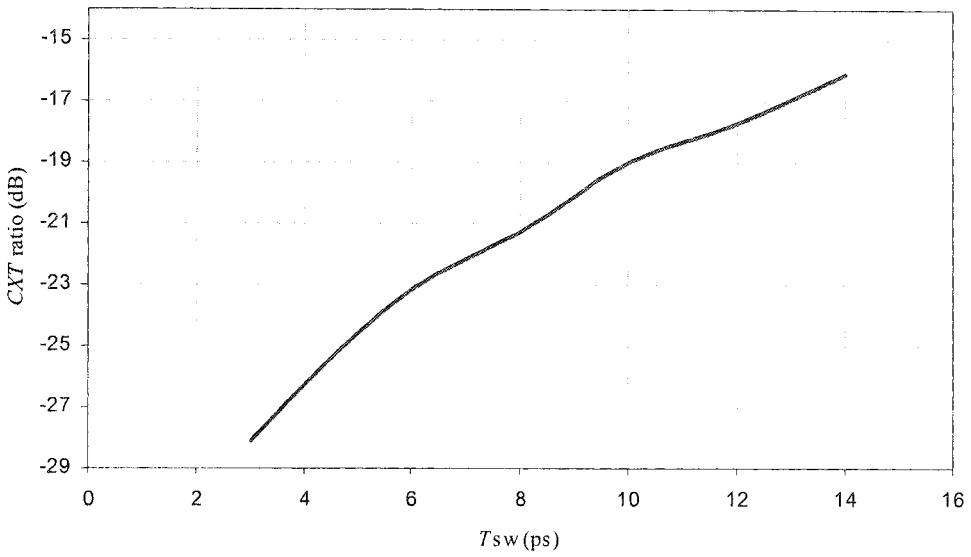
(a)



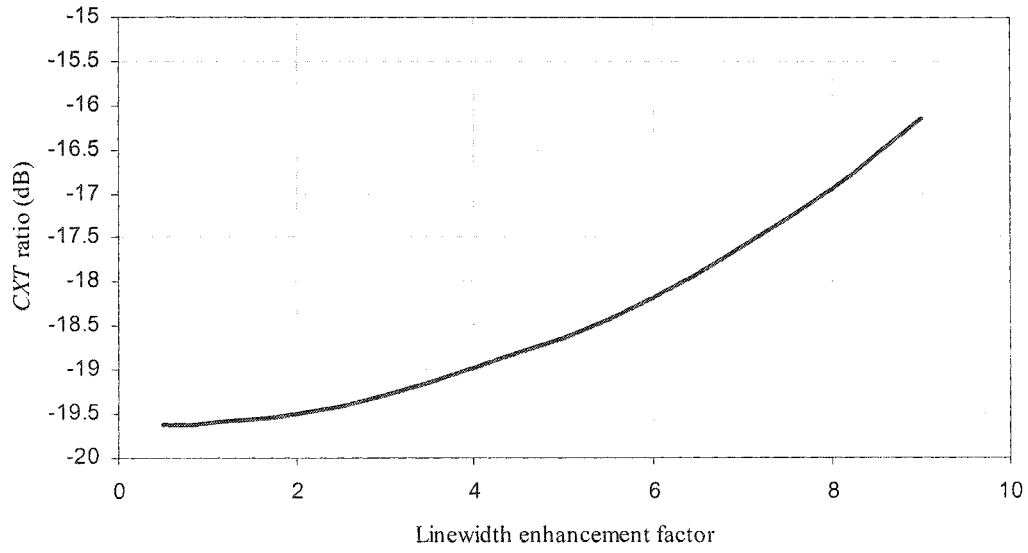
(b)

Figure 3.7 Crosstalk versus (a) control power, and (b) FWHM of CP and SP

As shown in Figure 3.8(a), *CXT* increases with the size of the SW width, due to the greater difference between G_1 and G_2 profiles. Although small T_{sw} leads to a lower *CXT*, but it results in reduced level of the output signal, due to lower gain of the SW. In Figure 3.8(b), *CXT* increases rapidly with α_{LEF}. This is because higher values of α_{LEF} will result in increased phase difference between G_1 and G_2 at the off (low) state of the SW, therefore leading to higher output power $P_{out,1}$ of the non-target pulses and consequently a higher *CXT*.



(a)

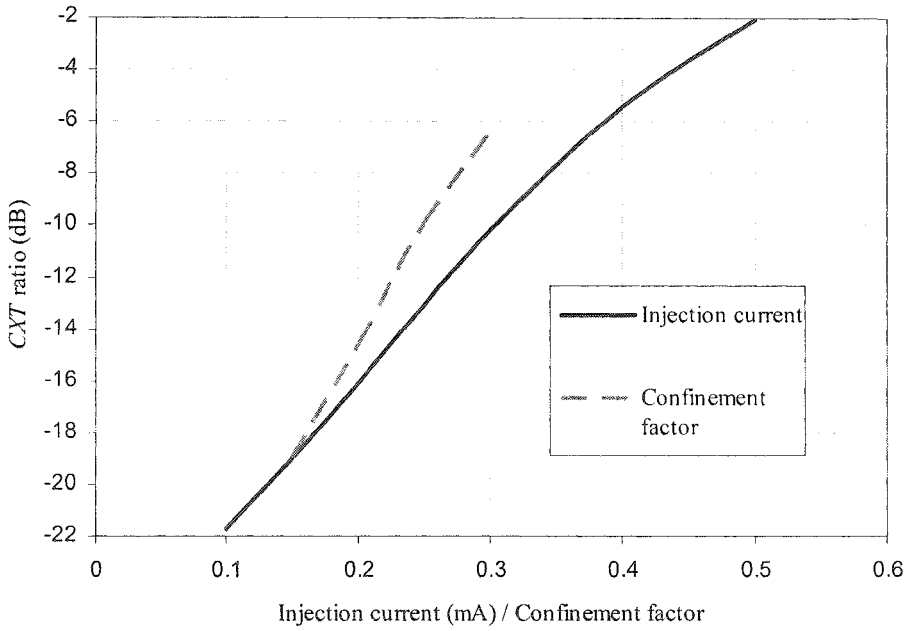


(b)

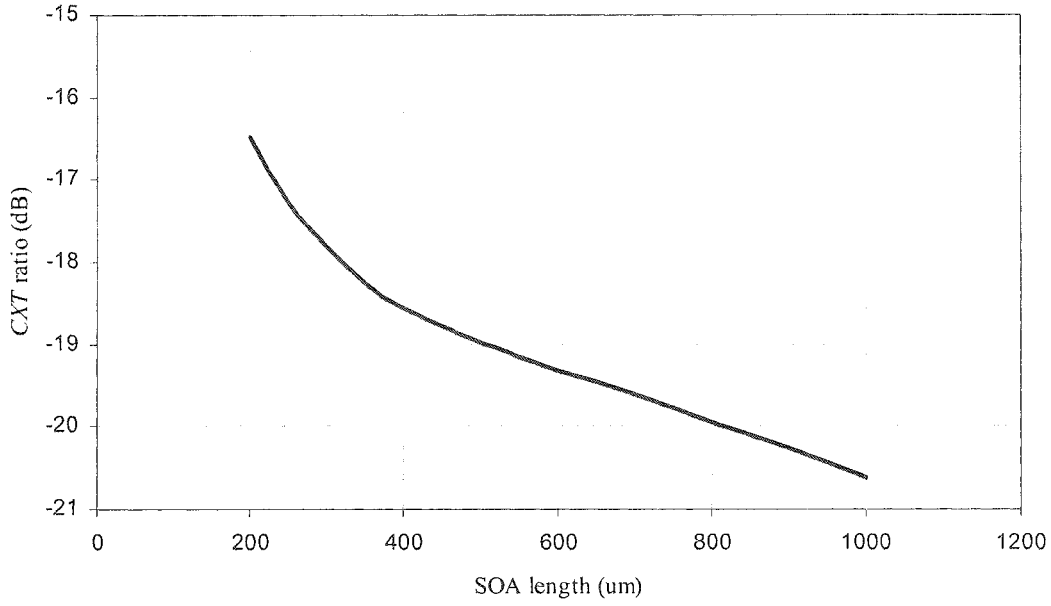
Figure 3.8 Crosstalk versus (a) CP1 and CP2 delay times, and (b) linewidth confinement factor

The following investigation focuses on the *CXT* characteristics against the injected current and the confinement factor, showing a linear behaviour as illustrated in Figure 3.9(a). This can be explained by (3.1), where higher values of I and Γ will result in a higher G. Note that higher I and Γ also contributes to a faster gain recovery time (i.e.

increased Δg) and increased ΔG (see Figure 3.6), respectively. Finally, Figure 3.9(b) shows the decrease in *CXT* with the SOA length, since longer SOA results in a higher gain for both the SW and non-target pulses, see (3.1).



(a)



(b)

Figure 3.9 Crosstalk versus (a) inject current and confinement factor, and (b) SOA length

The lowest level of *CXT* is achieved for the following system parameters: CP and SP with FWHM of 1 ps, T_{sw} of 3 ps, L of 1000 μm, I of 0.15 A, Γ of 0.15, α_{LEF} of 0.5, SP power of 0.5 mW, and CP power of 20 mW. Simulation results showed that, for data rates of 80, 160, and 320 Gb/s, the lowest level of *CXT* observed are at –33.27, –28.20, and –22.78 dB, respectively, but at the cost of reduced output power levels of 2.80, 1.40, and 0.47 mW, respectively.

From the simulation results, it is shown that the proposed SPC can operate at a relatively low control power (~20 mW) and achieve the minimum *CXT* level of -20 dB. Furthermore, by carefully selecting the SOA parameters the *CXT* level of the SPC could be further controlled to ensure the optimum performance.

3.5 All-Optical Logic Gates Based on SMZ

In future ultra-high speed photonic networks, signal processing such as clock recovery, packet header extraction, address correlation and etc. could be realised by employing all-optical switches and all-optical logic gates. SMZ structure would be one option to realise optical logic gates such as AND, XOR, and NOT [222], see Figure 3.10. The preliminary simulation results and simulation parameters adapted are shown in Figure 3.11 and Tables 3.3 and 3.4, respectively.

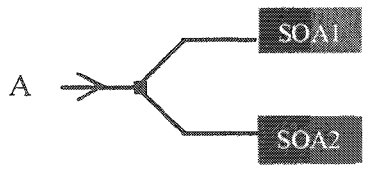
Table 3.3 SOA simulation parameters

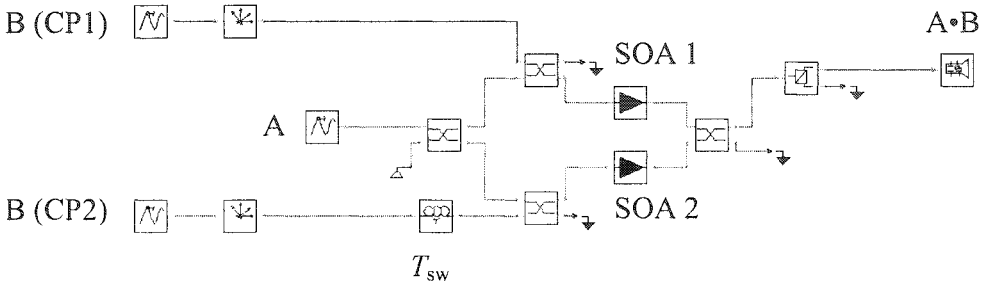
Parameters	Values
Iniect current	0.15 A
Length	500×10^{-6} m
Width	3×10^{-6} m
Height	80×10^{-9} m
Confinement factor	0.15
Differential gain	2.78×10^{-20} m^2
Carrier density at transparency	1.4×10^{24} m^{-3}
Initial carrier density	3×10^{24} m^{-3}
Linewidth enhancement factor	5
Recombine constant A	1.43×10^{8} s^{-1}
Recombine constant B	1×10^{-16} m^3s^{-1}
Recombine constant C	3×10^{-41} m^6s^{-1}

Table 3.4 Signal and control pulses default parameters

Parameters	Values
Bit interleaved time	1.5 ns
Wavelength of data packet	1554 nm
Signal & control pulse widths	2 ps
Signal pulse power/energy	1 mW/2.27 fJ
Control pulse (CP) power/energy	20 mW/45.45fJ

A	B	A • B
0	0	0
0	1	0
1	0	0
1	1	1





Optical pulse transmitter

Polarisation controller (PC)

3-dB coupler

Fibre delay line (FDL)

Semiconductor optical amplifier (SOA)

Polarisation beam splitter (PBS)

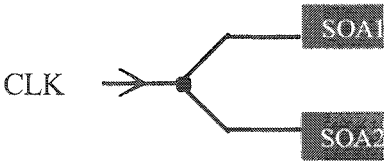
Null source

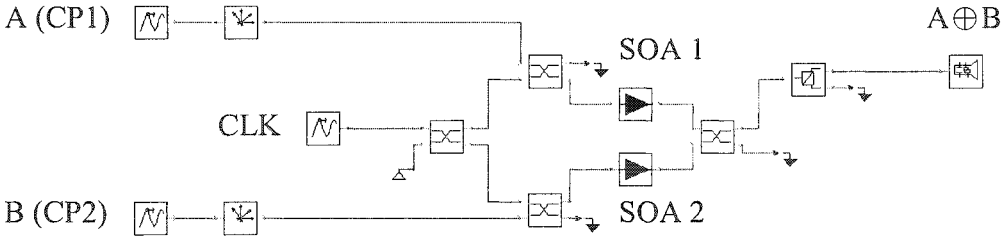
Ground

Virtual scope

(a)

A	B	A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0





(b)

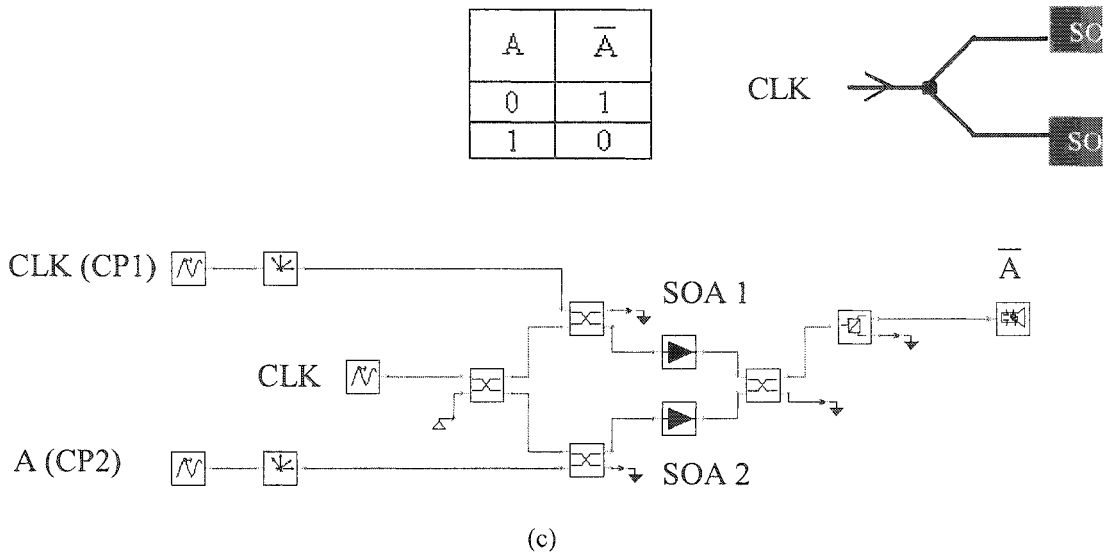
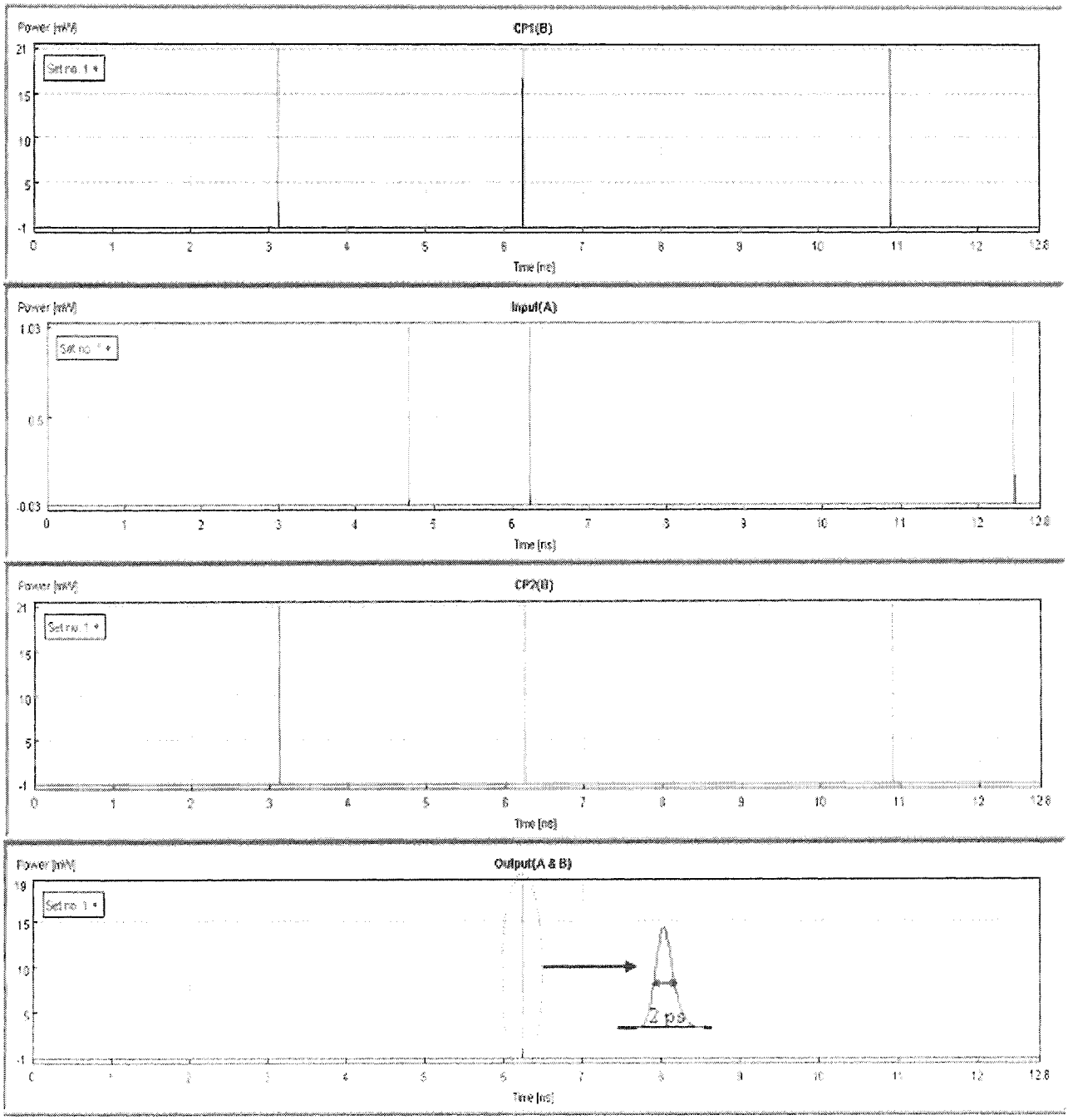


Figure 3.10 (a) AND, (b) XOR and (c) NOT gates based on SMZ

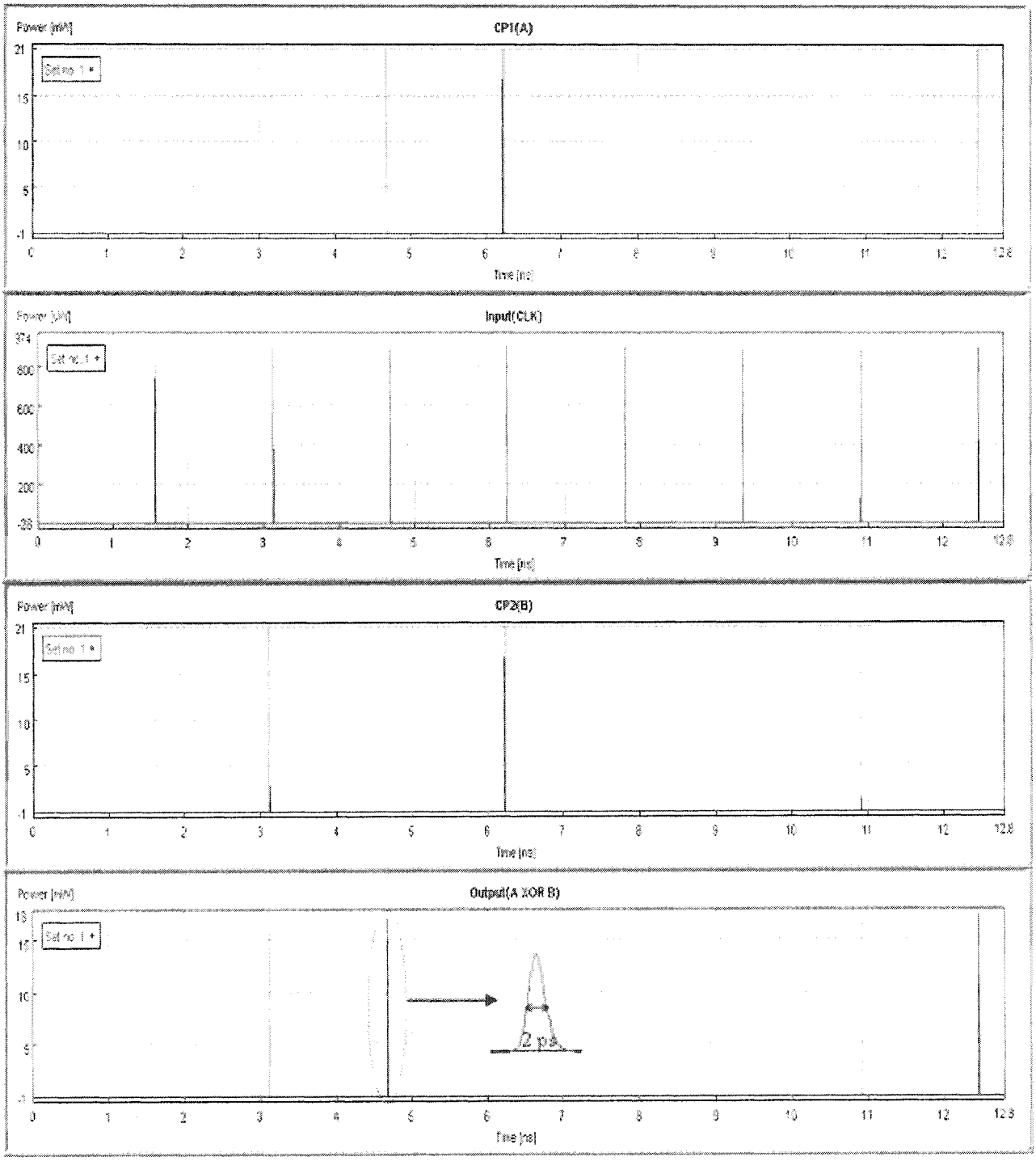
To implement the logic AND operation (i.e. A•B) based on the SMZ structure, signal A is applied to the input of the SMZ, signal B is used as CP1 and CP2 applied to SOAs with a time delay ($T_{delay} = T_{sw}$), see Figure 3.10(a). In the absence of input signal (i.e. A = 0) no signal emerges from the output (i.e. A•B = 0). With input signal (i.e. A = 1) and no CPs (i.e. B = 0) the output is still zero (i.e. A•B = 0). However, with input and CPs signals (i.e. A•B = 1) there is a signal at the output, see Figure 3.11(a). Note that the two signals B shown in Figure 3.11(a) represent CP1 and CP2, respectively. CP1 and CP2 have the same amplitude with a delay of T_{sw}.

For achieving the logic XOR operation (i.e. A⊕B) in the SMZ structure, the clock signal (CLK) is applied to the input of the SMZ, with signals A and B acting as CPs to the SMZ, see Figure 3.10(b). The output signal is high only when the SMZ is in an unbalance state (i.e. A≠ B), see Figure 3.11(b) for the simulation time waveforms.

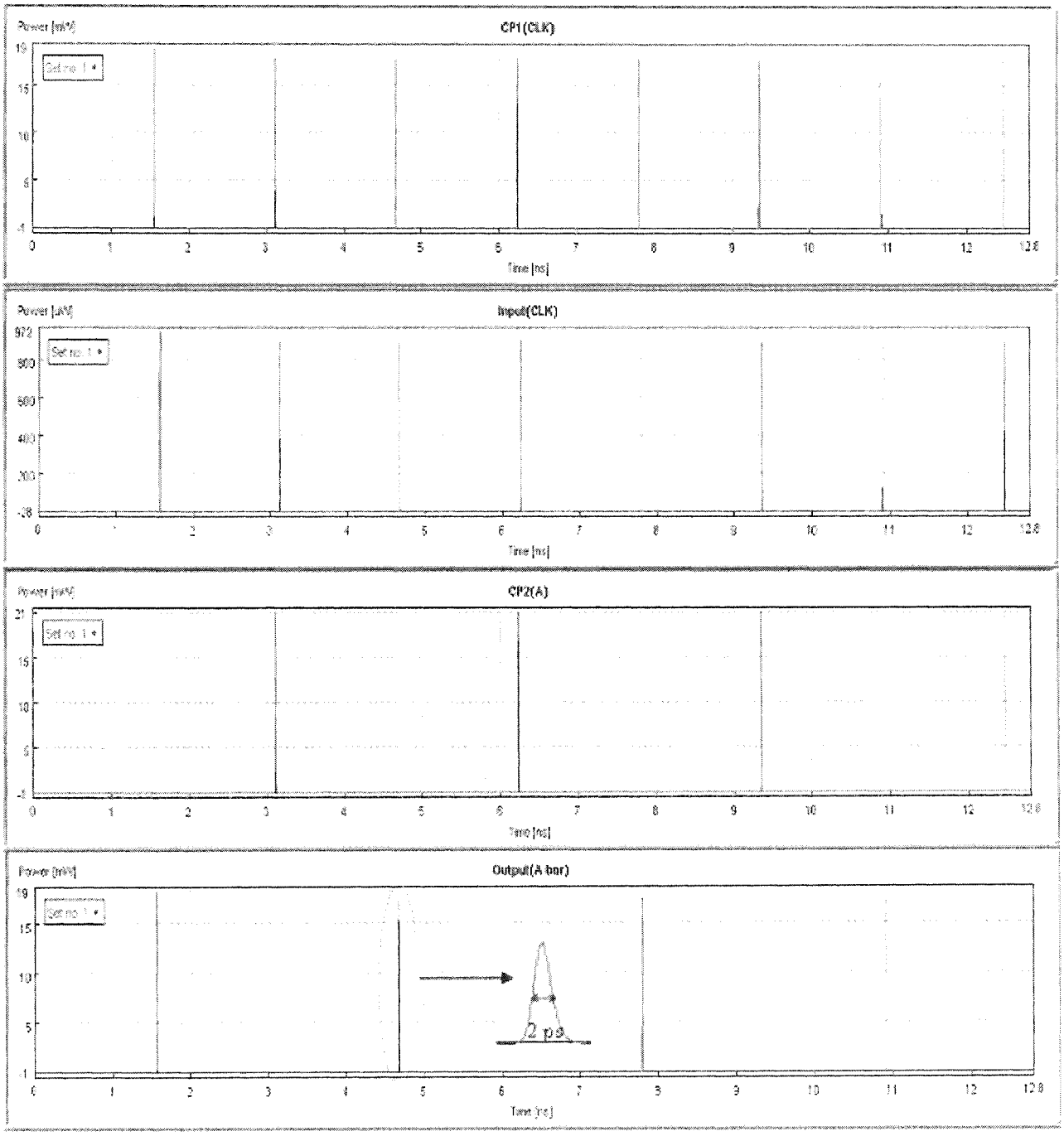
Similarly, the NOT logic operation can be realised by the same operation principle. CLK is applied to the input of SMZ as well as the SOA1, see Figure 3.10(c). With A = 1 the SMZ is in a balance state, thus $\overline{A}$ = 0, see Figure 3.11(c) for the simulation time waveforms. More on the operation principles of all-optical NOT gate will be given in the next section.



(a)



(b)



(c)

Figure 3.11 Simulation results of all-optical (a) AND, (b) XOR and (c) NOT gates based on the SMZ (also see the enlarged pulse waveforms)

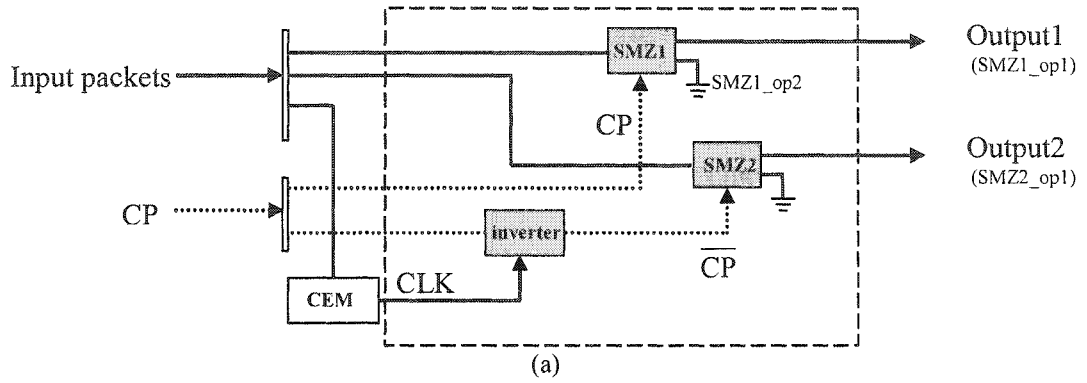
3.6 High Contrast Ratio 1×2 All-optical Switch Based on SMZ

SMZ function is based on the cross-phase modulation of semiconductor optical amplifiers (SOAs) [55], where switching is performed by introducing a phase difference between signals propagating in two arms of interferometer [173] by injecting a high power optical control pulse to SOAs. However, in practice, it is not simple to maintain an exact phase shift of 180^{o} in SOAs. Therefore, in most cases, only the output port 1 of SMZs are used (i.e. output 1 in Figure 3.4) for switching purpose due to its low inter-output contrast ratio (*CR*) [223]. A practical all-optical 1×2 router employing SMZs, should have a high inter-output *CR* for lower values of output crosstalk (*CXT*). Therefore, a novel all-optical 1×2 switch with a high inter-output *CR* (> 32 dB) based on three SMZs is proposed in this section.

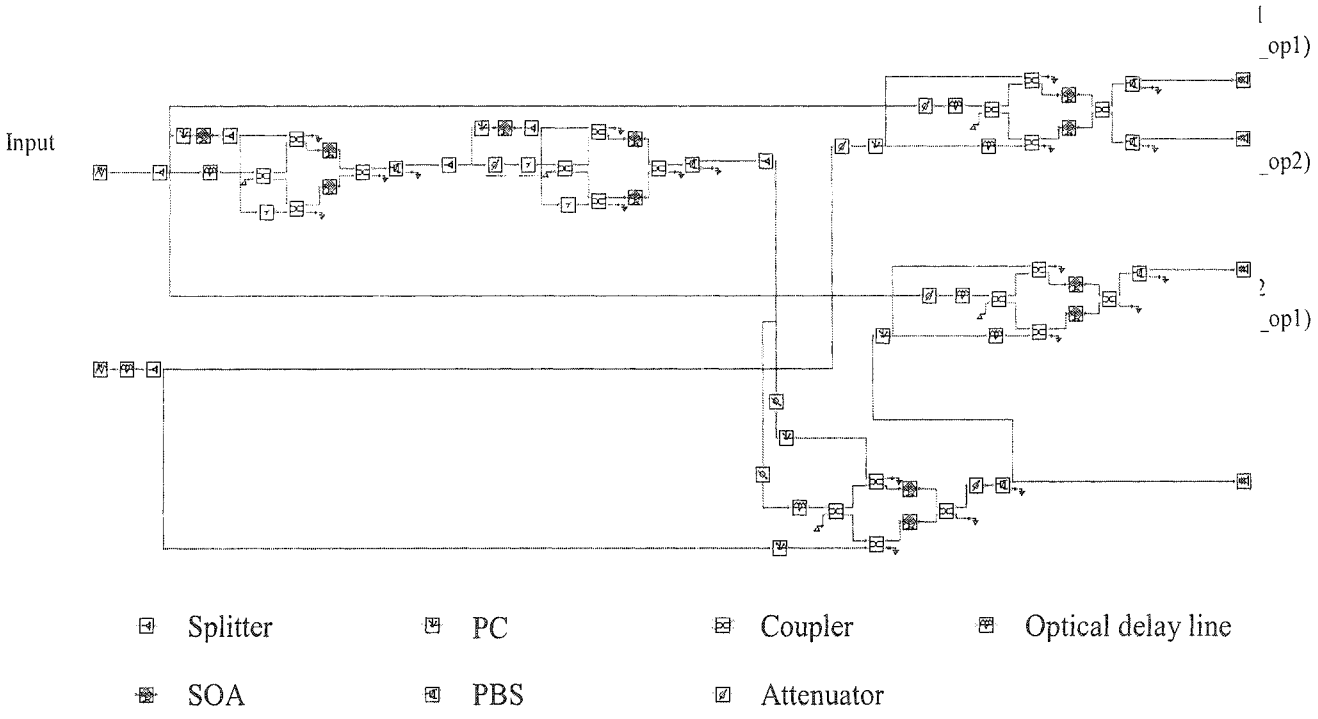
The inter-output *CR* of a 1×2 switch is defined as the power ratio between the switched and non-switched signals outputs_{ij} where $i, j = 1$ or 2. Typically the value of inter-output *CR* observed at the SMZ output 2 (CR_{21}) is less than 10 dB [223]. Here a 1×2 switch utilising an optical inverter that offers improved CR_{21} is introduced.

Figure 3.12(a) shows a schematic diagram of the proposed 1×2 switch. The input packet is applied to the SMZ_1, SMZ_2 and to the clock extraction module (CEM) [224]. More descriptions of the CEM could be found in APPENDIX – D. The extracted clock signal is used as a CP in the optical inverter. To achieve a high inter-output *CR*, each SMZ only uses its output port 1. In the absence of CP, the input packet is switched to the output 2 since SMZ_1 is in the OFF state. With the CP the SMZ_1 is ON and SMZ_2 is OFF, thus the packet is switched to the output 1. Note that the extracted

clock and CP signals should be fully synchronised in time to ensure correct operation of the switch. Figure 3.12(b) shows the VPI equivalent of Figure 3.12(a).



(a)



(b)

Figure 3.12 (a) An all-optical 1×2 switch, and (b) VPI based model

The proposed all-optical 1×2 switch is simulated using the Virtual Photonics Inc. simulation software and its inter-output *CR* is numerically investigated. All the main simulation parameters used are shown in Table 3.5 and Table 3.6.

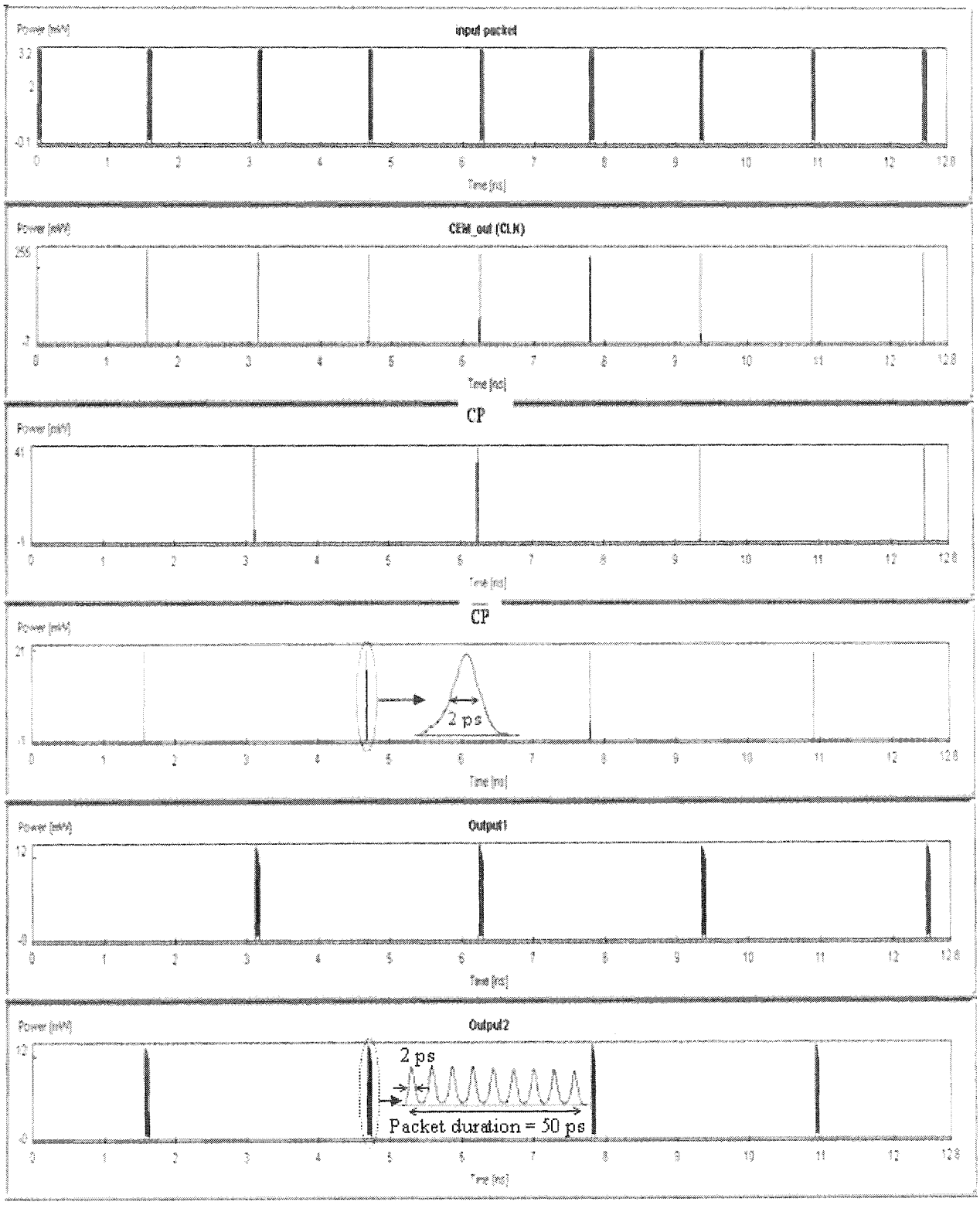
Table 3.5 SOA simulation parameters

Parameters	Values
Iniect current	0.15 A
Length	500×10^{-6} m
Width	3×10^{-6} m
Height	80×10^{-9} m
Confinement factor	0.15
Differential gain	2.78×10^{-20} m^2
Carrier density at transparency	1.4×10^{24} m^{-3}
Initial carrier density	3×10^{24} m^{-3}
Linewidth enhancement factor	5
Recombine constant A	1.43×10^{8} s^{-1}
Recombine constant B	1×10^{-16} m^3s^{-1}
Recombine constant C	3×10^{-41} m^6s^{-1}

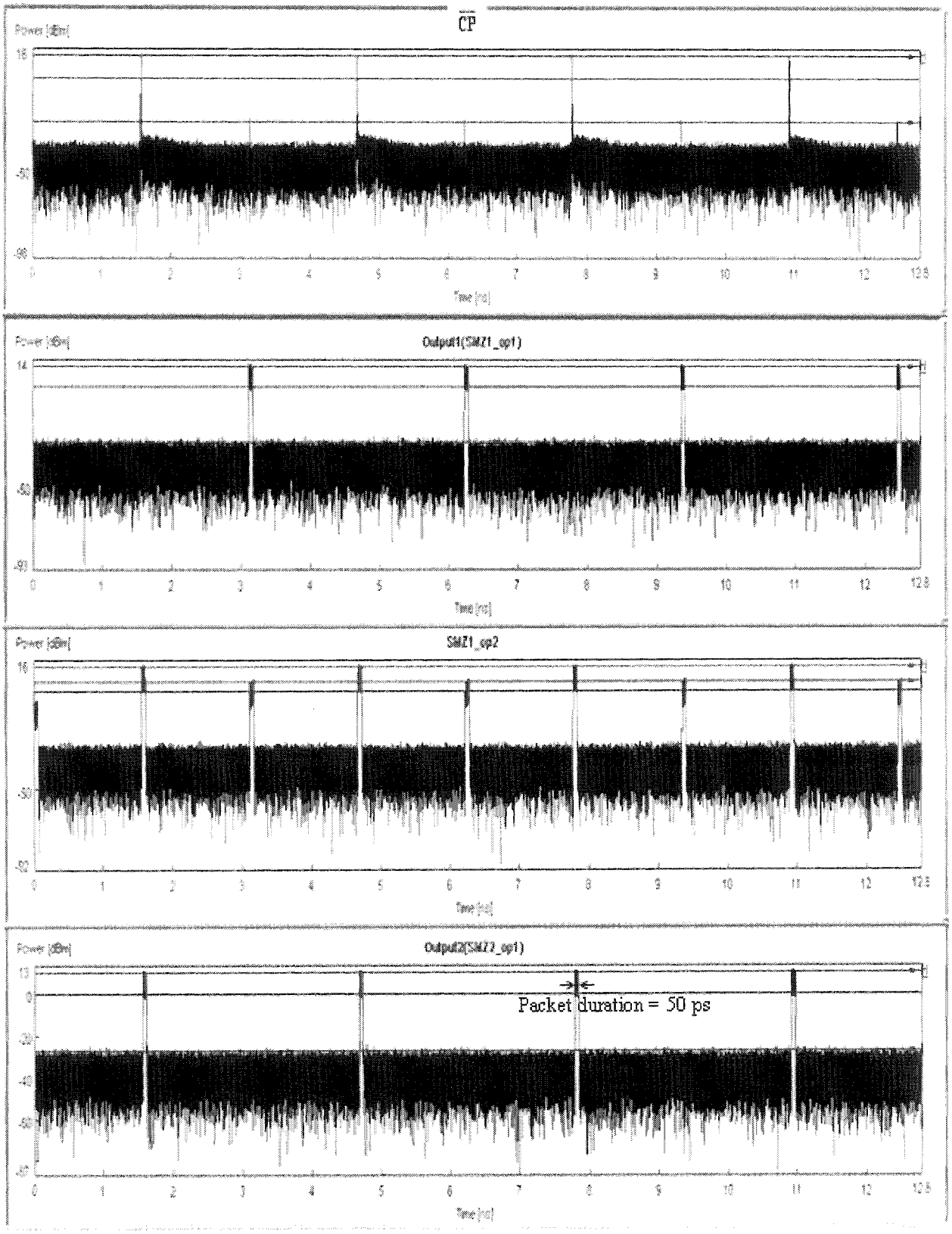
Table 3.6 Signal and control pulses default parameters

Parameters	Values
Data packet bitrate $R_b = 1/T_b$	160 Gb/s
Bit duration T_b	6.25 ps
Packet payload length	1 byte (8 bits)
Packet guard time	1.5 ns
Wavelength of data packet	1554 nm
Data & control pulse widths (FWHM)	2 ps
Packet pulse peak power/energy	1 mW/2.27 fJ
Control pulse (CP) power/energy	40 mW/90.91 fJ

The input packet is composed of one clock bit and eight payload bits. Figure 3.13(a) illustrates the captured simulated time waveforms at various points. It is shown that with the CP present the input packets are switched to the output 1. Figure 3.13(b) depicts the output power intensities (in dB) at the outputs 1 and 2, $\overline{CP}$, and SMZ1_op1. It is shown that at the SMZ_op2, CR_{21} of a single SMZ is about 7.5 dB (which is low). This is due to phase shift not being exactly 180^{o} in SOA leading to incomplete destructive signals at the SMZ_op2. By employing an optical inverter and dual SMZs, the CR_{21} has been significantly improved to about 35 dB.


input packet
CEM_out (CLK)
CP
$\overline{CP}$
2 ps
Output1
Output2
2 ps
Packet duration = 50 ps
Time [ns]

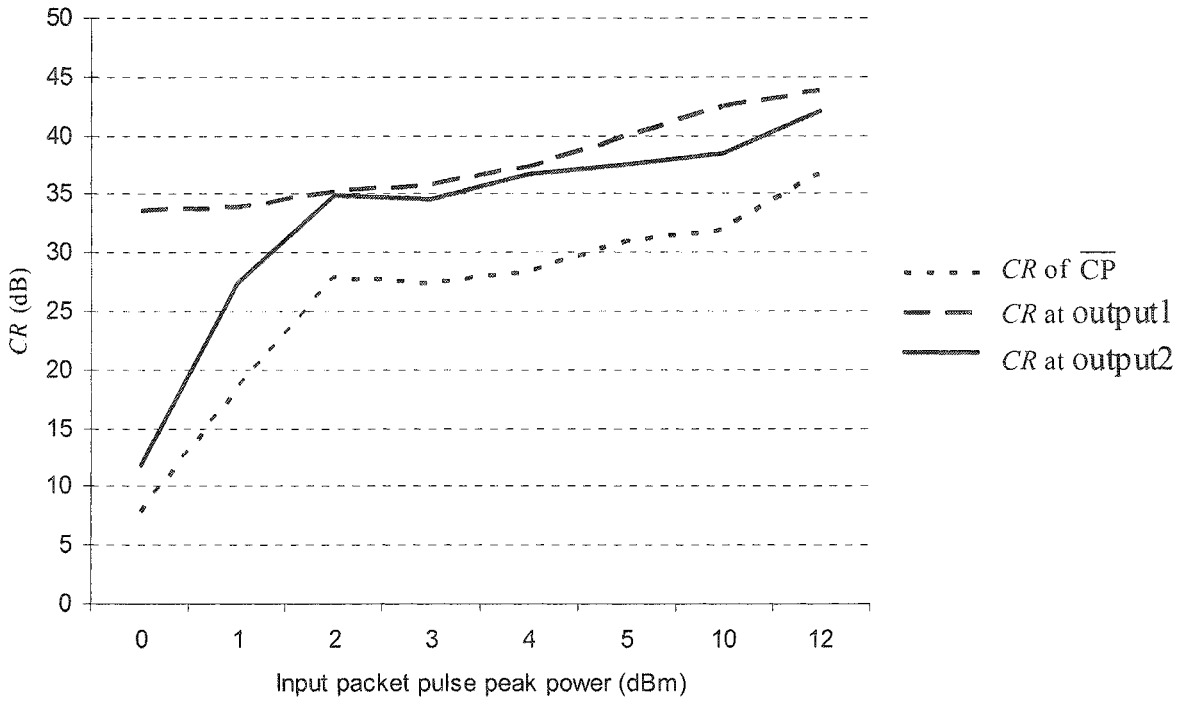
(a)



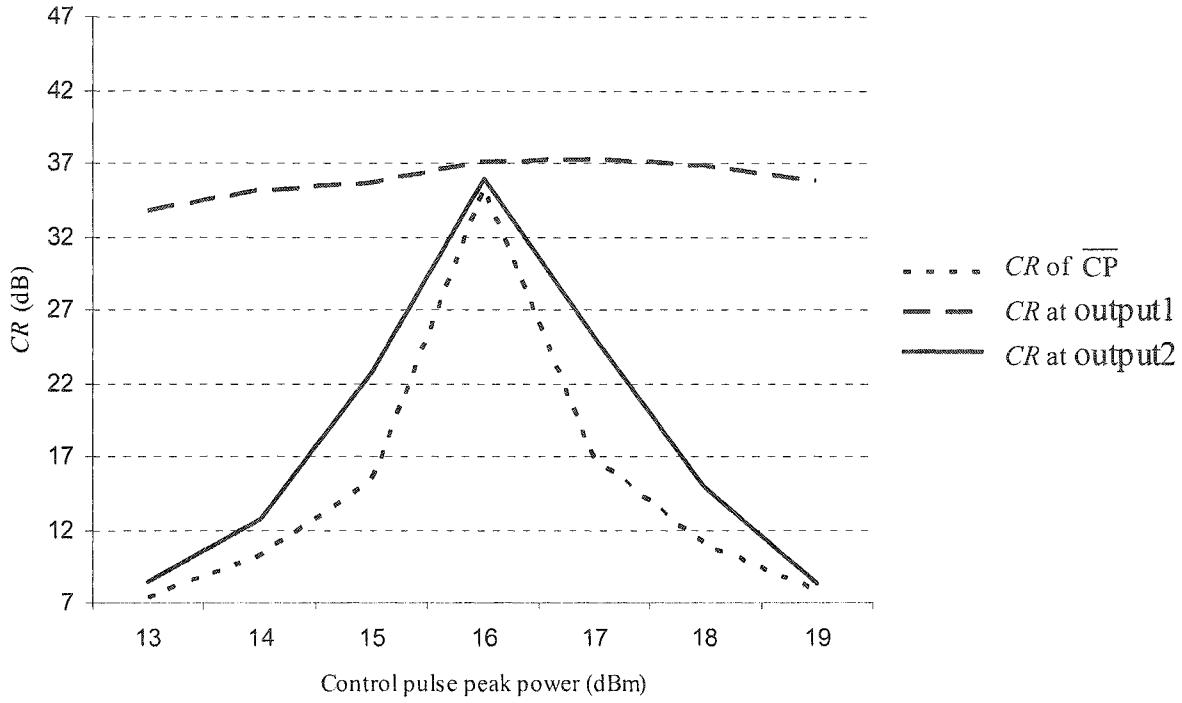
(b)

Figure 3.13 (a) Output waveforms (also see the enlarged pulse waveforms), and (b) *CR* ratio observed at $\overline{CP}$, the proposed 1×2 switch output 1, output 2, and SMZ1_op2

Figure 3.14(a) and (b) display the inter-output *CR* for $\overline{CP}$, and at the outputs 1 (i.e. CR_{12}) and 2 (i.e. CR_{21}) against the input power and the control pulse power, respectively. The proposed 1×2 switch illustrates a high inter-output *CR* over a wide range of input powers. However, the *CR* shows higher sensitivity to the control power reaching a maximum value of 35 dB at a control power of 16 dBm. Note that the *CR* for output 1 is almost flat compared with the others. This is because of a CP with a higher *CR* is applied directly to the SMZ_1. The variation in the *CR* at the output 2 (i.e. CR_{21}) is due to $\overline{CP}$ with different power levels (i.e. varying *CR* values) being applied to the SMZ_2. The result shows that the inter-output *CR* of the 1×2 switch is mainly dependent on the *CR* of optical inverter.



(a)



(b)

Figure 3.14 The observed contrast ratio (*CR*) against (a) the input packet power and (b) the control pulse power

By carefully selecting the power of the control pulses, inter-output *CR* of > 32 dB was achieved over a wide range of input packet power (12 dB). The proposed 1×2 switch offered an improvement in the inter-output *CR* of ~ 25 dB in comparison with a single SMZ switch. The proposed switch could potentially be adopted for high-speed signal processing and packet routing in all-optical networks.

3.7 Three-input AND Gate Based on FWM using a Single SOA

Most of the reported AND gates exploit the XGM and XPM characteristics of SOAs when being used in optical interferometer switches such as SMZ [55], terahertz optical asymmetric demultiplexer (TOAD) [172] and ultrafast nonlinear interferometer (UNI) [54]. However, these schemes are based on a two-input AND-gate configuration inherited from the 2×2 optical switch employing two identical SOAs. In these structures, the input and control ports are used as the AND-gate inputs. Realisation of an AND gate with more than two inputs will require a hybrid combination of parallel and cascading of two-input AND gates, which results in a complex optical circuit and additional noise accumulation. In addition, employing more than one SOA in an AND gate (such as in SMZ) will effect the AND gate performance such as the output amplitude modulation, on/off ratio and input/output power characteristic due non-identical SOAs (This is a practical problem, where no two SOA will have the same characteristics). In this section, the three-input AND gates based on the FWM using a single SOA is proposed, which offers reduced complexity and transparency with respect to the modulation format of data signal compared to the existing switch-based AND-gates.

Figure 3.15 shows the schematic diagram of an M-input AND gate based on FWM. Assuming that M is the total number of input frequencies, the number of generated components (beat and modulated signals) N_{out} is given by:

$$N_{out} = \frac{M^2(M-1)}{2}. \tag{3.10}$$

For practical reasons it is necessary that the output of the optical bandpass filter contains a combination of all M input frequency components. Note that since each pair of input signals beats with one another and get modulated with other input signals, only up to three signals are required to generate a new frequency component. Therefore, the FWM operation is limited to $M \leq 3$. If $M \geq 4$ then output signals do not contain components composed of all different input frequencies.

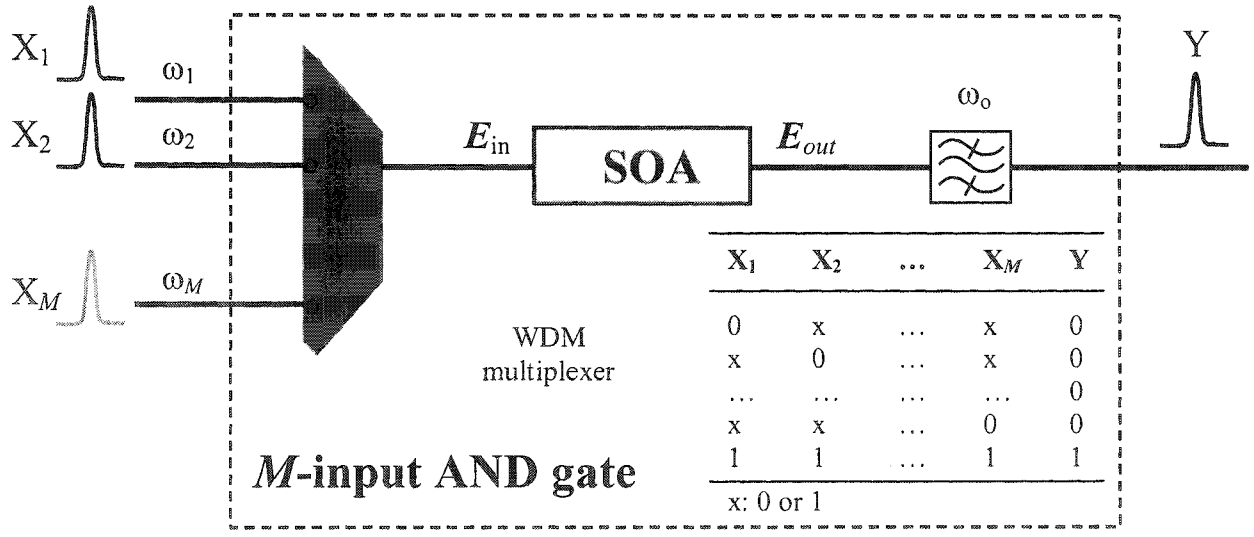


Figure 3.15 Schematic of a *M*-input AND gate based on SOA-FWM

For $M = 2$, signal beating at $\omega_2 - \omega_1$ will modulate both input signals at ω_1 and ω_2, generating two new signals of $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$. For $M = 3$, there will be three beating signals at $\omega_3 - \omega_2$, $\omega_3 - \omega_1$ and $\omega_2 - \omega_1$ modulating with three input signals (ω_1, ω_2 and ω_3). The resultant nine (N_{out}) generated signals [205], in which there are three output signals of interest (dashed lines), contain all three input frequency components at $\omega_1 + \omega_2 - \omega_3$, $\omega_3 + \omega_1 - \omega_2$ and $\omega_2 + \omega_3 - \omega_1$. The output Y (one of the three modulated components) can be obtained by using an optical bandpass filter with a resonant frequency of ω_0. The VPI setup diagram for the three-input AND gate is shown in Figure 3.16(a). The input signals f_1, f_2 and f_3 are at 193.1, 193.4 and 194.1

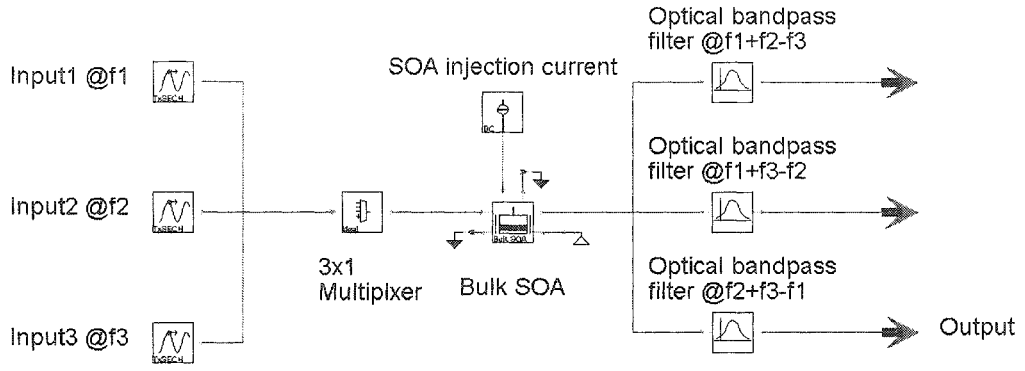
THz, respectively. Note that $\omega = 2\pi f$. Three bandpass filters at centre frequencies of $f_1 + f_2 - f_3$, $f_1 + f_3 - f_2$, and $f_2 + f_3 - f_1$ are used to select three possible resonant frequencies. Here for the performance investigations, Y is obtained at the resonant filter frequency $f_0 = f_2 + f_3 - f_1$ instead of other two generated frequency components in order have the maximum output power [138]. The AND gate operation at a bit rate of 10 Gb/s is shown in Figure 3.16(b). The simulation parameters used in this simulation are shown in Tables 3.7 and 3.8.

Table 3.7 Main simulation parameters

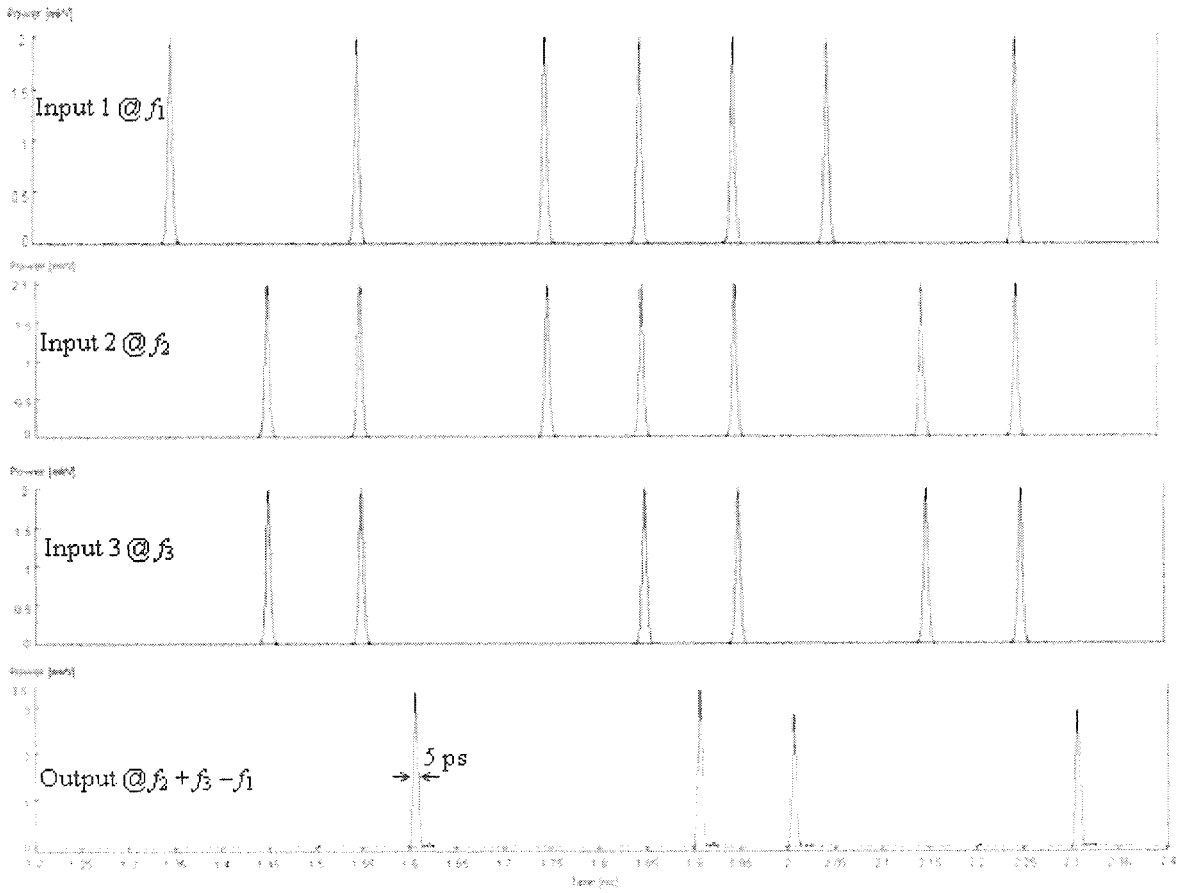
Parameters	Values
X_1 signal frequency – f_1	193.1×10^{12} Hz (1554 nm)
X_2 signal frequency – f_2	193.4×10^{12} Hz (1551 nm)
X_3 signal frequency – f_3	194.1×10^{12} Hz (1546 nm)
X_1 pulse peak power– P_1	2 mW
X_2 pulse peak power– P_2	2 mW
X_3 pulse peak power– P_3	2 mW
Pulse energy	11.36 fJ
Pulse width (FWHM)	5 ps
Output filter frequency – f_0 ($f_0 = f_2 + f_3 - f_1$)	194.4×10^{12} Hz (1543 nm)
Filter bandwidth – B_0	140×10^{9} Hz (1 nm)

Table 3.8 The bulk SOA parameters

Parameters	Values
Laser chip length	600×10^{-6} m
Active region width	3.0×10^{-6} m
Active region thickness	40.0×10^{-9} m
Confinement factor	0.07
Group effective index	3.7
Material linewidth enhancement	3.0
Differential refractive index	-1.11×10^{-26} m^3
Linear material gain coefficient	3.0×10^{-20} m^2
Transparency carrier density	1.5×10^{-24} m^{-3}
Nonlinear gain coefficient	1.0×10^{-23} m^3
Nonlinear gain time constant	200.0×10^{-15} s
Carrier capture time constant	70.0×10^{-12} s
Carrier escape time constant	140.0×10^{-12} s
Gain peak frequency	196.0×10^{12} Hz
Gain coefficient spectral width	1.0×10^{13} Hz
Population inversion parameter	2.0
Initial carrier density	1×10^{24} m^{-3}
Injection current	200 mA



(a)



(b)

Figure 3.16 (a) VPI schematic for a 3-input AND gate based on FWM in SOA(b) Three inputs X_1, X_2, X_3 and output Y, respectively, of AND gate operating at the bitrate of 10 Gb/s

The performance of the proposed AND gate based on FWM is investigated by observing its amplitude modulation and the on/off contrast ratio.

A. Amplitude modulation ratio

The interaction of input signals and SOA causes a drop in the SOA carrier density, hence reducing the SOA gain [225]. Therefore, a high-speed bit stream will experience bit-patterning effect in which the output bits are not equally amplified by the same SOA gain [225] resulting in amplitude variation of the output bits. In order to measure the amplitude variation the amplitude modulation (AM) ratio is defined as the ratio of the maximum value over the minimum value of the output bits "1", see Figure 3.17(a), given as:

$$r_{AM} = \frac{P_{1,\max}}{P_{1,\min}}. \tag{3.11}$$

B. On/off contrast ratio

An important performance parameter for the AND-gate operation is the on/off contrast ratio ($r_{on/off}$) that determines the distinctivness between the generated bits "1" and residual bits "0", see Figure 3.17(b). $r_{on/off}$ is defined as the minimum value of output bit "1" and the maximum of output bit "0" and given as:

$$r_{on/off} = \frac{P_{1,\min}}{P_{0,\max}}. \tag{3.12}$$

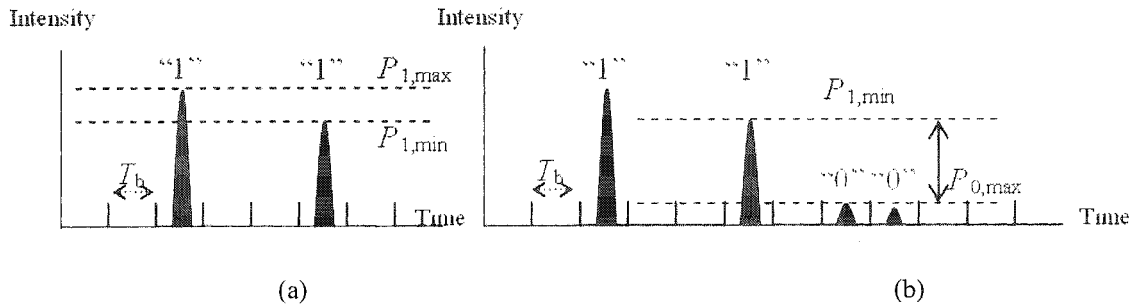


Figure 3.17 (a) AM ratio and (b) on/off contrast ratio

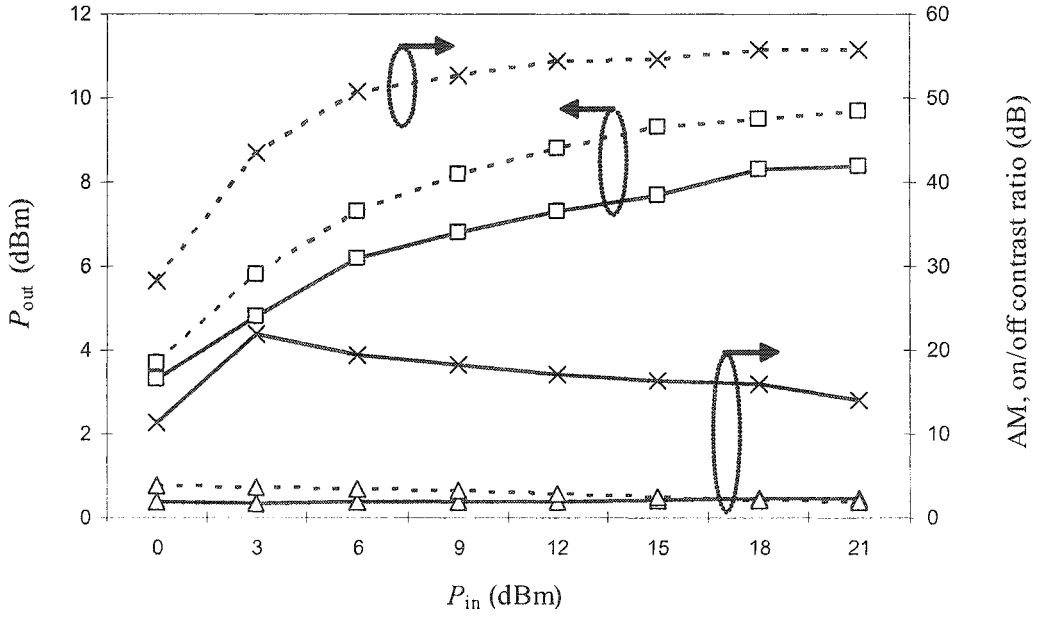
Figure 3.18(a) shows the dynamic range of output signal power P_{out}, r_{AM} and $r_{on/off}$ against the input signal power for two-input and three-input AND gates. Input powers P_{in} are all equally set to 2 mW (3dBm) in both cases. It is observed that the output powers in both cases increase with the input power. However, P_{out} for $M = 2$ is greater than P_{out} for $M = 3$. This is due to the relative conversion efficiency function R which is defined as [205]:

$$R = 10\log_{10}(P_{in} / P_{out}), \tag{3.13}$$

where P_{in} and P_{out} are the input signal power and the output converted signal power, respectively.

R is inversely proportional to detuning spacing parameter, hence reducing the output power [205]. The output powers are saturated at 7.5 and 9.2 dBm when $P_{in} > 100$ mW (20 dBm) for $M = 2$ and 3, respectively, since SOA gain is saturated, thus, no further output gain improvement. The AM ratios for $M = 2$ and 3 are slightly varied within a margin of 2.5 dB in the displayed range of P_{in} values. However, r_{AM} starts to decrease with the increase of P_{in} due to the input bit patterning effect (i.e. random bits 0/1 in a transmitted bit sequence) is no longer considerable when the SOA gain is saturated as the gain is less sensitive to the change of P_{in}. The on/off contrast ratios rapidly increase with the input power as the FWM effect is stronger. However, $r_{on/off}$ starts to saturate for $M = 2$ and reduce for $M = 3$ due to the output powers slowly increasing when $P_{in} > 2$ mW (3dBm) and start saturating. Note that $r_{on/off}$ ($M = 2$) is much better than $r_{on/off}$ ($M = 3$) because there are a lesser amount of interference from the generated frequency components: 2 and 9 tones for 2-input and 3-input AND gate, respectively. It is observed that the highest $r_{on/off}$ ($M = 3$) is achieved over 20 dB for P_{in} of 2 mW (3dBm).

Figure 3.18(b) depicts the performance of the proposed two/three-input AND gates operating at different bit rates of 10, 20 and 40 Gbps. The simulation parameters given in Table 3.7 are the same for all different bit rates. Note that for higher bit rates (i.e. reduced T_b), the time required for SOA gain to recover to its initial gain value is shortened. Therefore, P_{out} decreases resulting in a reduced $r_{on/off}$ and an increased r_{AM} with a margin ~ 4 dB.



(a)

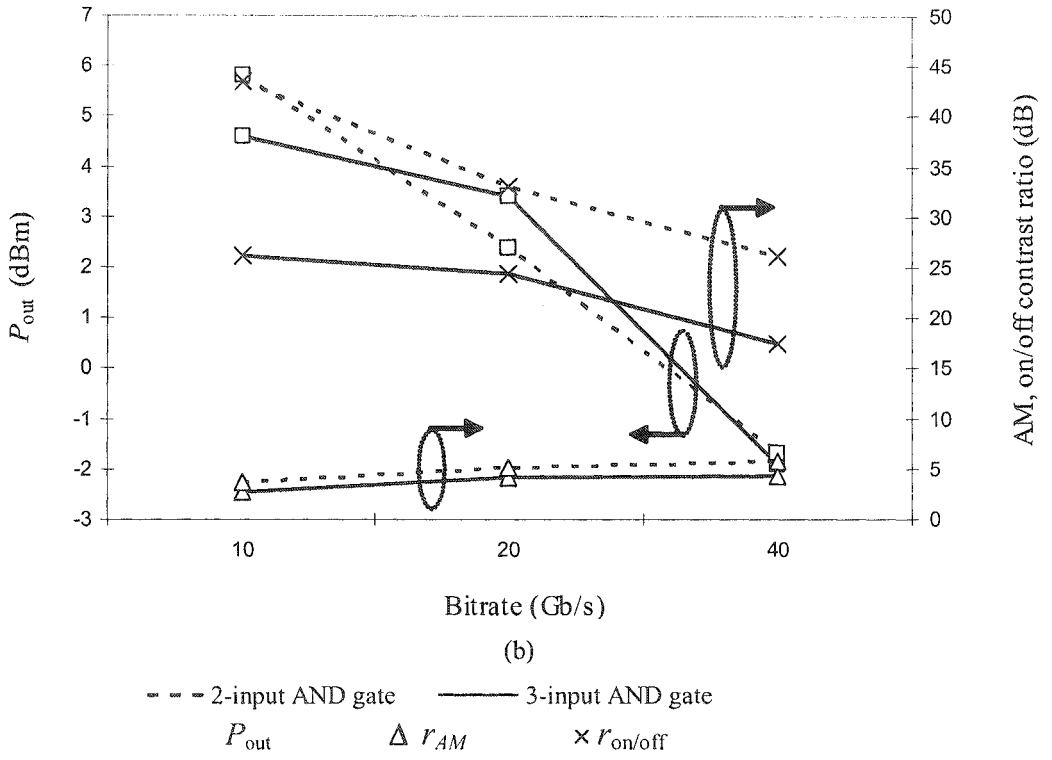


Figure 3.18 Output power, AM and on/off contrast ratio against (a) input power and (b) bit rate

The simulation results show that the FWM-based AND gates offer on/off-contrast ratios larger than 20 dB and an acceptable amplitude modulation margin at high operating bit rates (of 20 and 40 Gb/s), thus making them a good candidate for high-speed all-optical processing applications.

3.8 Summary

All-optical components such as all-optical switches and all-optical logic gates are the building blocks for realising transparent all-optical networks. In this chapter, the nonlinearities of SOA and operation principle of a SMZ were explained. The *CXT* characteristics of an-optical SPC module were investigated illustrating that the

proposed SPC is capable of operating at relatively low control power of ~20 mW to achieve the minimum *CXT* level of -20 dB by carefully optimising the system parameters. By carefully selecting the power of the control pulses of the proposed all-optical 1×2 switch the improvement in the inter-output *CR* of ~ 25 dB was achieved in comparison to a single SMZ switch. The principles of all-optical logic gates based on SMZ (AND, XOR, and NOT gates) were explained with operating time waveforms. Finally, an all-optical 3-inputs AND gate based on the FWM were introduced and simulated, with results showing larger than 20 dB on/off-contrast ratios and an acceptable amplitude modulation margin at operating bit rates of 20 and 40 Gb/s. The proposed components are potential candidates for building complex functionalities in all-optical domain.

All-optical header processing and address correlation are the key functions for realising all-optical packet routings, SMZ-based modules have been used as the fundamental building blocks in the proposed all-optical router. In the next chapter, the node architecture and operation principle of a router with PPM based packet header address format will be introduced.

CHAPTER 4 PPM BASED PACKET HEADER ADDRESS FORMAT

4.1 Introduction

All-optical packet routing is being proposed as an alternative to the existing low-speed packet routing schemes where header processing is implemented in the electrical domain [14, 20]. By replacing the slow O/E/O conversion modules and carrying out header processing in all-optical domain a higher data throughput and lower power consumption can be achieved. An alternative header processing method based on the pulse-position-modulation header processing (PPM-HP) has been proposed in [59, 226], where the incoming optical packet address bits and the routing table entries are both converted into a PPM format before being correlated with each other. However, PPM-HP will require a serial-to-parallel converter (SPC) to extract individual bits from the incoming packet header address, an array of 1×2 switches and the delay lines [226]. For packets with a long header bit pattern, there will be increased switching stages, which will result in deterioration of the extinction ratio of the output PPM address and increased system complexity.

In Section 4.2, a node architecture no longer employing the SPC and an array of 1×2 switches is proposed. By employing the PPM based packet header address format, address conversions are no longer required in each router, thus significantly reducing the system complexity. The optical switch control module which generates successive control pulses for opening a wide switching window is introduced in Section 4.3. Furthermore, the optical signal-to-noise ratio performance in multiple-hop is also discussed in Section 4.4. The affects on the correlated signal and the average packet

power at the output of the router due to the timing-offset of the PPM address are investigated in Section 4.5. Finally, Section 4.6 will summary this chapter.

4.2 All-optical PPM-HP Router

A typical packet is composed of a header (clock and address) and payload bits, see Figure 4.1. The clock information is used for synchronisation within the router. The header address is in PPM frame format composed of 2^N time slots T_s and a short duration (< one time slot) pulse.

4.2.1 PPM

A PPM is a baseband modulation technique most commonly used in optical communications (fibre optics as well as free space optics) because of unparallel power efficiency compared to any other baseband modulation technique. In the PPM, each set of N-bit input word $b = (a_1, a_2, \ldots\ldots\ldots a_M) \in (0,1)^N$ is mapped to one of L–array PPM symbols, where $L = 2^N$. L-PPM symbol $X = (0,\ldots.0,1,000\ldots.0) \in (0,1)^L$ contains a single pulse of one time slot duration $T_s = N/(LR_b)$ and L-1 empty slots, where R_b is the data bit rate. The position of the pulse is indicated by the binary representation of b.

For example, a target address of "0111" with a decimal value of 7 is represented in PPM as a "0000000100000000", see Figure 4.1.

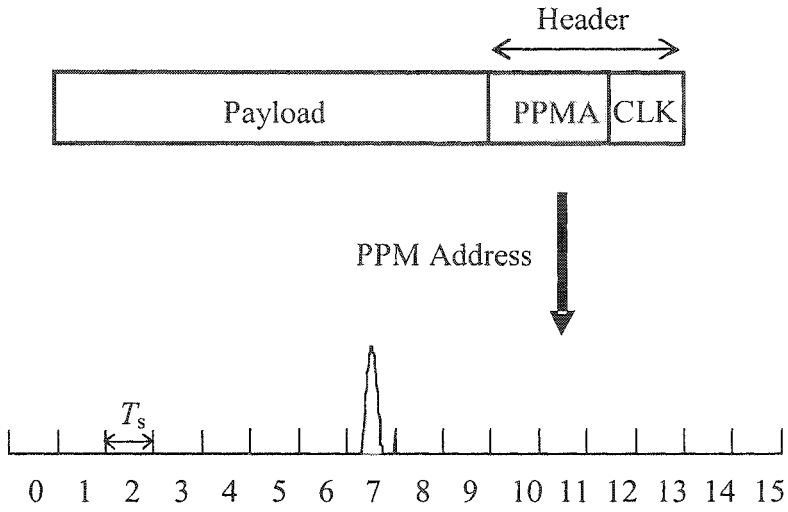


Figure 4.1 An optical packet with a PPM address

PPM has very low duty cycle of L^{-1} and a peak-to-average power ratio of L. A PPM signal can be written as:

$$x(t) = L\overline{P}\sum_{N=0}^{L-1} c_N p(t - \frac{NT_f}{L}), \qquad x(t) \geq 0 \text{ and } \overline{x(t)} \leq \overline{P} \ , \tag{4.1}$$

where $\overline{P} = L^{-1}\sum_j \overline{x_j(t)}$ the average transmitted optical power, T_f is the symbol period, $[c_0, c_1, \ldots\ldots c_{L-1}]$ is the PPM code word. For the same bit rate, PPM requires L/N more bandwidth and a lower average power by a factor of $(0.5LN)^{0.5}$ compared to the on-off keying (OOK).

4.2.2 PPM-HP

Figure 4.2 illustrates architecture of the $1\times M$ PPM-HP router composed of a clock extraction module (CEM), a PPM header address extraction module (PPM-HEM), a pulse position routing table (PPRT), AND gates, a number of fibre delay lines (FDLs), all-optical switches (OS), an OS control module (OSC), and optical splitters.

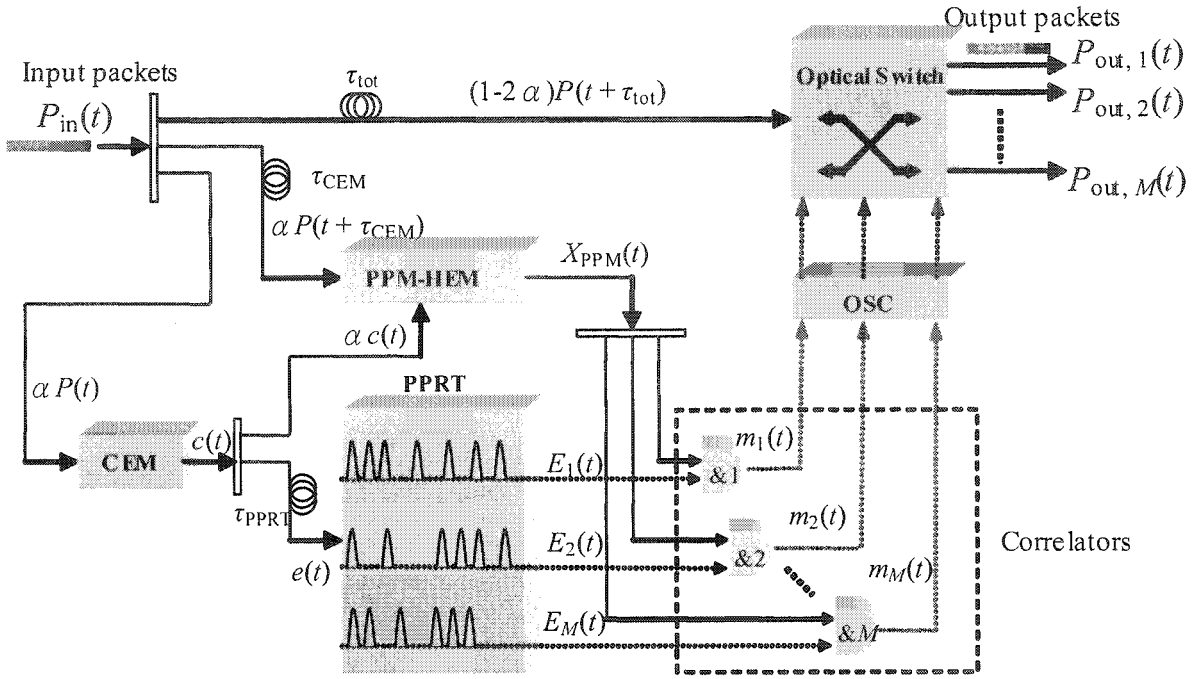


Figure 4.2 A schematic block diagram of a 1×M PPM header processing (PPM-HP) based router

The incoming optical packet $P_{in}(t)$ is split and applied to the CEM, PPM-HEM and OS with the delays of 0, τ_{CEM} (required time for the clock extraction) and τ_{tot} (total required time for PPM address correlation), respectively. CEM is based on two cascading SMZ switches as in [224] offering reduced residual crosstalk, more discussions about the residual crosstalk can be found in Section 3.4. The extracted clock $c(t)$ is applied to the PPM-HEM (based on a single SMZ switch configuration) and PPRT modules with the delays of 0 and τ_{PPRT}, i.e. $\alpha c(t)$ and e(t), respectively, where α is the splitting factor. The recovered PPM address (2^N-bit frame) at the output of the PPM-HEM is applied to a bank of AND gates.

Table 4.1 (a) Conventional routing table with 2^N-entries and (b) its corresponding PPRT with M entries

(a)

Address patterns	Decimal value	Output ports
0000	0	Port 1,2 (multicast)
0001	1	Port 3
0010	2	Port 1,2,3 (broadcast)
0011	3	Port 1
0100	4	Port 1
0101	5	Port 2
0110	6	Port 1
0111	7	Port 1
1000	8	Port 3
1001	9	Port 2
1010	10	Port 3
1011	11	Port 3
1100	12	Port 2
1101	13	Port 1
1110	14	Port 3
1111	15	Port 2

(b)

Address patterns (grouped)	PPRT entries
0000 0010 0011 0100 0110 0111 1101	E_1 {0, 2, 3, 4, 6, 7, 13}
0000 0010 0101 1001 1100 1111	E_2 {0, 2, 5, 9, 12, 15}
0001 0010 1000 1010 1011 1110	E_3 {1, 2, 8, 10, 11, 14}

Table 4.1 illustrates both a conventional routing table (CRT) and the proposed PPRT with 2^N and M entries, respectively. In the CRT each header address is assigned a particular output port, whereas in PPRT a group of header address j is converted into a PPM format, and assigned the same output. Each PPM frame is composed of j pulses of one slot duration with location determined by the decimal metrics of each address, see Figure 4.3.

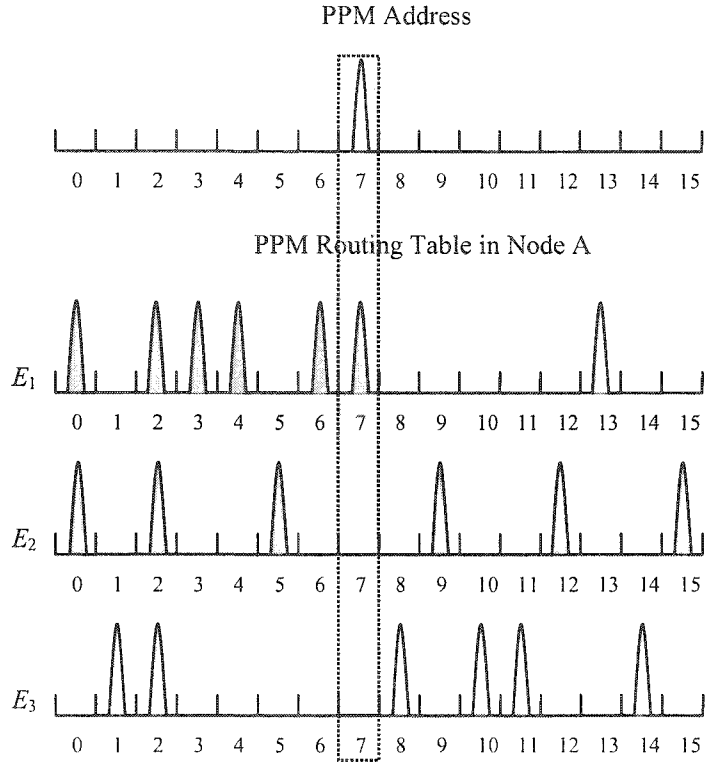


Figure 4.3 Correlation between PPM address and PPRT entries

Note that shown in Table 4.1(b) is the PPRT for node A. Similarly, for nodes B, C, and D, the PPRT entries would be $E_2 \in \{2, 6, 7, 13, 14\}$, $E_2 \in \{2, 7, 8, 12, 15\}$, and $E_3 \in \{0, 4, 5, 7, 9, 13\}$, respectively.

A PPRT is generated by applying a portion of the clock signal 1 - $\alpha c(t)$ (i.e. $e(t)$) through a number of optical switches and delay lines as outlined in Figure 4.6(a), and is given as:

$$E_k(t) = \sum_{d_k} e(t + d_k \times T_s), \qquad \forall\, d_k \in D_k, k \le M, \tag{4.2}$$

where T_s is the PPM time slot, D_k is the k^{th} set containing all decimal values of the header address assigned to the k^{th} output node (where $k = 1,2,\ldots, M$).

Packet destination address identification is carried out by correlating the extracted PPM-header address with the PPRT entries using an array of SMZ based optical AND

gates [227], see Figure 4.3. Since a single bit-wise AND operation is required for each correlation, then the SOA gain recovery time of the AND-gate is no longer an issue regardless of the sizes of the packet header and the routing table. The correlated signal at the output of the k^{th} AND gate can be expressed as:

$$m_k(t) = X_{PPM}(t) \times E_k(t) = \begin{cases} 1 & if \quad d_k = pos(X_{PPM}(t)) \quad \forall k \\ 0 & if \quad d_k \neq pos(X_{PPM}(t)) \quad \forall k \end{cases}, \quad k = 1,2,...,M \qquad d_k \in D_k \tag{4.3}$$

where $X_{PPM}(t)$ is the PPM header frame and $pos(X_{PPM}(t))$ is the pulse position within $X_{PPM}(t)$.

Existence of timing offset τ_{os} (defined by % T_b), no matter how small, between $X_{PPM}(t)$ and E_k will affect the intensity of $m_k(t)$, as will be investigated in Section 4.5. If more than one pulse is located at the same position in more than one PPRT entries, then a packet is classified as the multicasted or broadcasted (same position in all entries) to multiple outputs or all outputs, respectively. $m_k(t)$ is subsequently applied to the OSC module to spawn a number of control pulses for controlling the optical switching window to allow complete packet switching with a negligible gain fluctuation, more details for the OSC module will be discussed in the next section.

The router output signal is given as:

$$P_{out,k}(t) = P_{in}(t) \times m_k(t) = \begin{cases} G_{OS} \times (1-2\alpha) \times P_{in}(t+\tau_{tot}) & if \quad m_k(t) = 1 \\ 0 & if \quad m_k(t) = 0 \end{cases}, \quad k = 1,2,...,M \tag{4.4}$$

where G_{OS} is the gain of the optical switch.

The address correlation time (or header recognition time) of PPRT scheme is determined by the duration of a 2^N-slot PPM-frame as:

$$T_{\text{PPRT}} = 2^N \times T_s . \tag{4.5}$$

In the conventional address correlation scheme, header recognition is carried out by sequentially correlation the address bits with every entry of the CRT. The required header recognition time of the CRT scheme T_{CRT} is defined as:

$$T_{\text{CRT}} = 2^N \times N \times T_{\text{AND}} \times M^{-1}, \tag{4.6}$$

where M is the number of the router's output ports, T_{AND} is the minimum time interval required for two successive AND operations, which is limited by the SOA recovery time. Typically T_{AND} (hundreds of picoseconds) is much greater than T_b (few picoseconds) in high-speed optical networks (bit-rate > 40 Gb/s).

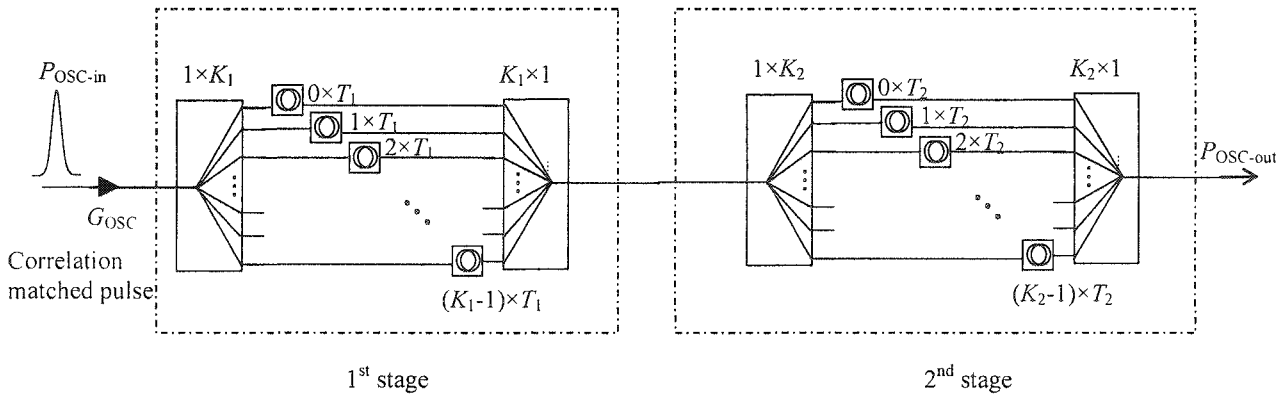
Comparing with using CRT, the correlation-time gain by employing PPRT, R_{PPRT}, is defined as the ratio of the time required for CRT scheme T_{CRT} over the required time for PPRT scheme T_{PPRT} and is given by:

$$R_{\text{PPRT}} = \frac{N \times T_{\text{AND}}}{M \times T_s} . \tag{4.7}$$

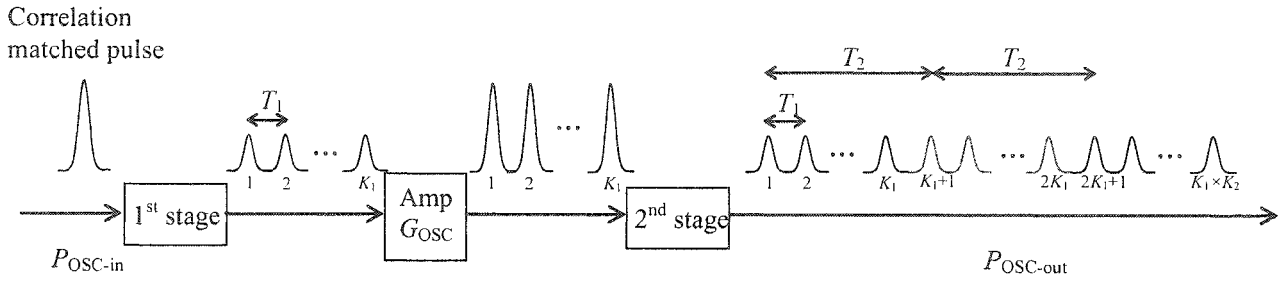
In this simulation ($N = 4$, $M = 3$, $T_{\text{AND}} = 500$ ps [56] (also see APPENDIX – C), $T_s = 6.25$ ps), the correlation-time gain, R_{PPRT} is equal to 106.67.

4.3 Optical Switch Control Module

Basically, the OSC module is a multiple-pulse generator, which generates successive control pulses for opening a wide SW, thus allowing the entire packet to go through. The input signal of the OSC is a single correlation matched pulse from the output signal of the AND gates. Figure 4.4(a) depicted the multiple-pulse generator with a two-stage structure. A single input pulse split into K_1 parts by the $1\times K_1$ splitter, is passed through a number of delay lines before being recombined again by a $K_1\times 1$ combiner. The same process is also taken place in the second stage. This process can be further explained with reference to Figure 4.4(b), where K_1 numbers of pulses with T_1 delay interval are generated after passing through the first stage. The pulses are then amplified by an optical amplifier with the gain of G_{OSC} before being applied to the second stage. As a result, the output of the second stage (i.e. the output of OSC module) will contain $K_1\times K_2$ pulses with T_1 delay interval, where $T_2 = T_1\times K_1$, see Figure 4.4(b).



(a)



(b)

Figure 4.4 (a) The 2-stage structure of the multiple-pulse generator (i.e. OSC), and (b) the process of multiple-pulse stream

Typically this time interval is set to be smaller than the SOA gain recovery time to reduce the switching gain fluctuation, for more details see Figure 7.5.

With the insertion loss of the splitter and combiner are defined as L_{splitter} and L_{combiner}, respectively, the minimum power of the input pulse $P_{\text{OSC-in}}$ required is given as:

$$P_{\text{OSC-in}}(\text{dB}) = P_{\text{OSC-out}} - G_{\text{OSC}} + 10\log_{10}(K_1 \times K_2) + 2L_{\text{splitter}} + 2L_{\text{combiner}}, \quad (4.8)$$

where $P_{\text{OSC-out}}$ is the target peak power of the CP stream, and G_{OSC} is the preamplifier gain.

Moreover, instead of using the above-mentioned multiple-pulse generator to create a wide SW, all-optical flip-flops (AOFFs) [12, 154, 223, 228-234] have been proposed as an alternative solution. AOFFs based OSC modules are more flexible than FDLs based OSC because they are capable of offering controllable time of continues wave for switching variable length of packets. However, AOFFs based OSC modules require additional continuous wave laser sources, thus making it complex and costly.

4.4 Multiple-hop and Optical Signal-to-Noise Ratio

An all-optical network is composed of K edge nodes and L core nodes with $K = 16$ edge nodes, see Figure 1.2. Each edge node has its own specific address. Incoming low-speed electrical packets at a source edge node with the same destination (i.e. the same target edge node) are combined and converted into a high speed optical packet. Optical packets are then routed to the destination via the core-network. When a packet arrives at PPM-HP based router (i.e. a core node), its header is processed and correlated with the entries of the local PPRT in order to switch the packet to the correct output port. Depending on the network configuration and the local PPRTs, packet will go through a number of core routers before reaching its targeted edge node.

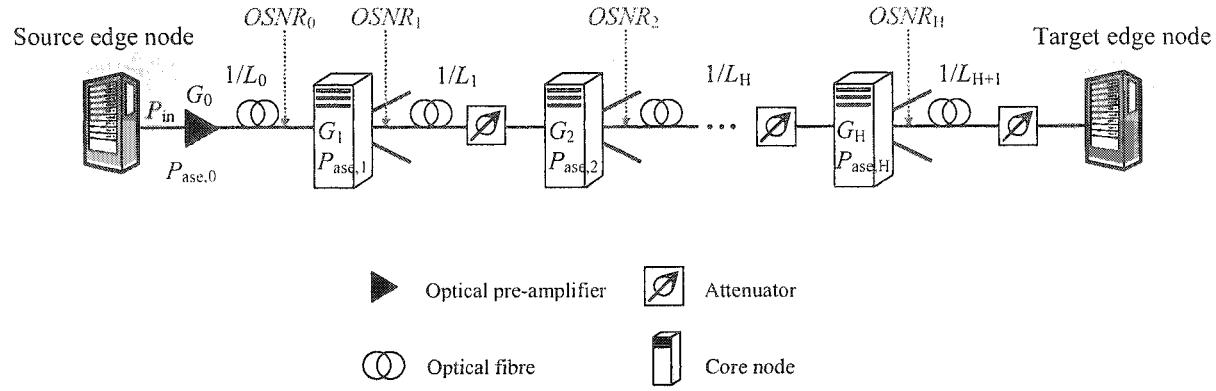


Figure 4.5 Signal and ASE noise power propagation from the source edge node to the target edge node via H core nodes

Figure 4.5 illustrates the path across the optical core network for packets with average power P_{in} from source to the destination. The packet signal is first amplified and passed through a fibre span before being applied to a node.

The SOA unpolarised amplified spontaneous emission (ASE) noise is generally computed by [60]:

$$P_{ase,i} = 2n_{sp,i}hf_0\left(G_{OS,i} - 1\right)B_0 \quad , \quad i = 0,1,...H \, , \tag{4.9}$$

where $n_{sp,i}$ and G_i are the spontaneous-emission factor and the gain, respectively, of the amplifier, where $i = 0$ represents the pre-amplifier and $i > 0$ denotes the SOA in OS modules. hf_0 and B_0 are the product of the Planck constant and the operating optical frequency, and the optical bandwidth of the system (i.e. filter optical bandwidth), respectively and H is the number of core nodes.

The OSNR at the target node is given as [226]:

$$OSNR_0 = \frac{(G_0 / L_0)P_{in}}{(1/L_0)P_{ase,0}}, \tag{4.10}$$

$$OSNR_1 = \frac{(G_0 G_1 / L_0 L_1)P_{in}}{(G_1 / L_0 L_1)P_{ase,0} + (1/L_1)P_{ase,1}}, \tag{4.11}$$

$$OSNR_2 = \frac{(G_0 G_1 G_2 / L_0 L_1)P_{in}}{(G_1 G_2 / L_0 L_1)P_{ase,0} + (G_2 / L_1)P_{ase,1} + P_{ase,2}}, \tag{4.12}$$

$$OSNR_H = \frac{\left(G_H \prod_{h=0}^{H-1}(G_h / L_h)\right)P_{in}}{\sum_{h=0}^{H-1}\left(P_{ase,h}\prod_{k=h+1}^{H}(G_k / L_{k-1})\right) + P_{ase,H}}, \tag{4.13}$$

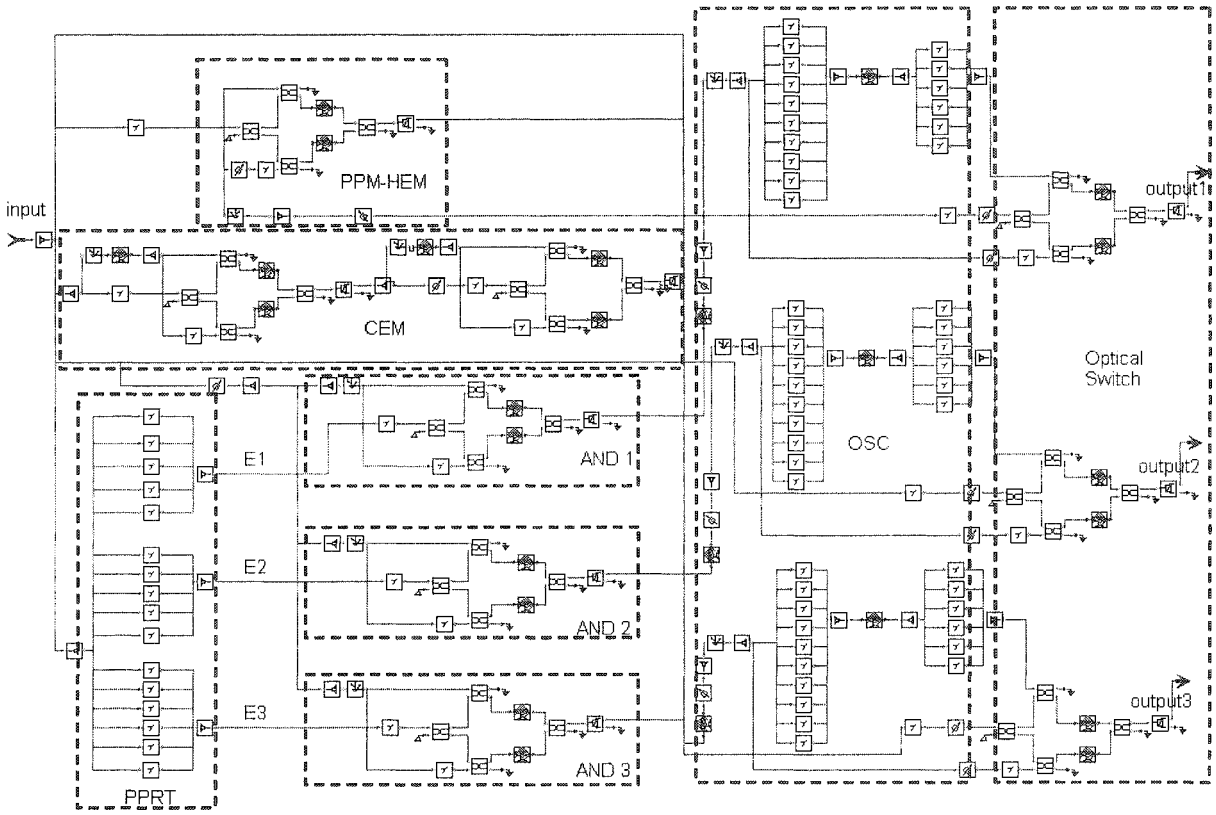
where L_h is the total loss incurred between any two core nodes.

4.5 Simulation Results and System Performance

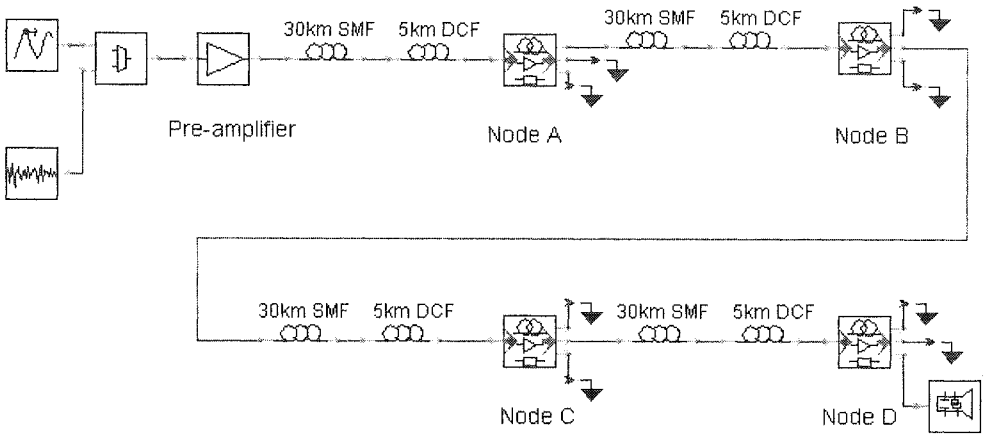
The proposed router is simulated and its performance is investigated by using the Virtual Photonics simulation package (VPI^{TM}), also see APPENDIX – A. Table 4.2 shows the main simulation parameters adopted from [210, 216].

Table 4.2 Simulation parameters

Parameters	Values
Data packet bit rate $R_b = 1/T_b$	160 Gb/s
Packet payload length	53 bytes (424 bits)
Wavelength of data packet	1554 nm (193.1 THz)
Data & control pulse widths (FWHM)	2 ps
PPM slot duration T_s (= T_b)	6.25 ps
Average transmitted packet pulse peak power	1 mW
Average pulse peak power of $C_k(t)$	75 mW
Optical bandwidth B_o	2.4 nm (300 GHz)
G_h (h = 1,2,...H)	20 dB
Total loss of a hop $1/L_h$ (h = 1,2,...H)	-7 dB
Pre-amplifier gain G_0	7 dB
First span loss $1/L_0$	-7 dB
Pre-amplifier n_{sp}	1.4
SOA length	500 μm
SOA n_{sp}	2
Inject current to SOA	150 mA
Splitting factor α	0.25



(a)



(b)

Figure 4.6 The VPI simulation schematic block diagram for (a) a router (node) architecture four-hop routing, and (b) four-hop routing

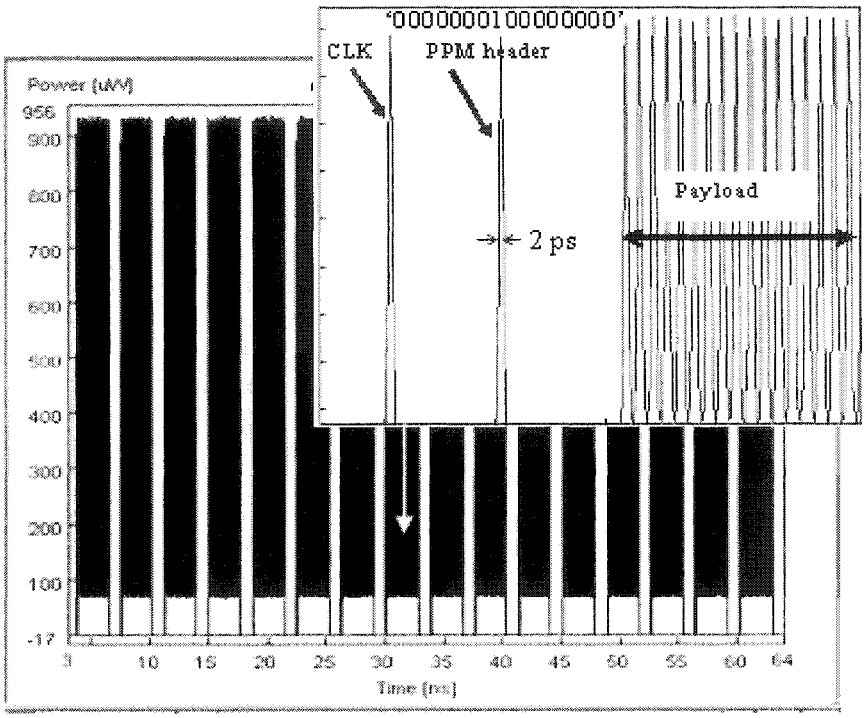
The schematic diagram of the simulation setup for an individual router and multi-hop routing are shown in Figure 4.6(a) and (b), respectively. In Figure 4.7(a), sixteen optical packets are transmitted at 160 Gb/s with 1 ns inter-packet guard time, the value of the packet guard time is chosen to be longer than the SOA gain recovery time, more discussions and investigations can be found in Section 6.4, where each packet contains 1 bit clock for synchronisation, 16 bits PPM address and 53 bytes payload (equal to the size of an ATM cell) [83, 235]. Both CEM and PPM-HEM module will require an input optical pulse sequence with an average power of 1 mW, see Section 7.3 for further explanations. The optical packets are amplified prior to transmission to compensate for the link losses (fibre attenuation and coupling loss). Each fibre span (link) comprises of 30 km of single-mode fibre (SMF) and 5 km of dispersion-compensating fibre (DCF) to compensate for the chromatic dispersion within the SMF [62]. The VPI equivalent of Figure 4.2 is depicted in Figure 4.6(a).

The total processing time of the all-optical PPM-HP based router, τ_{tot} (i.e. the time delay between the input packets and switched packets) in this simulation ($N = 4$, $T_s = T_b = 6.25$ ps) is equal to 112.5 ps, which is calculated as follows:

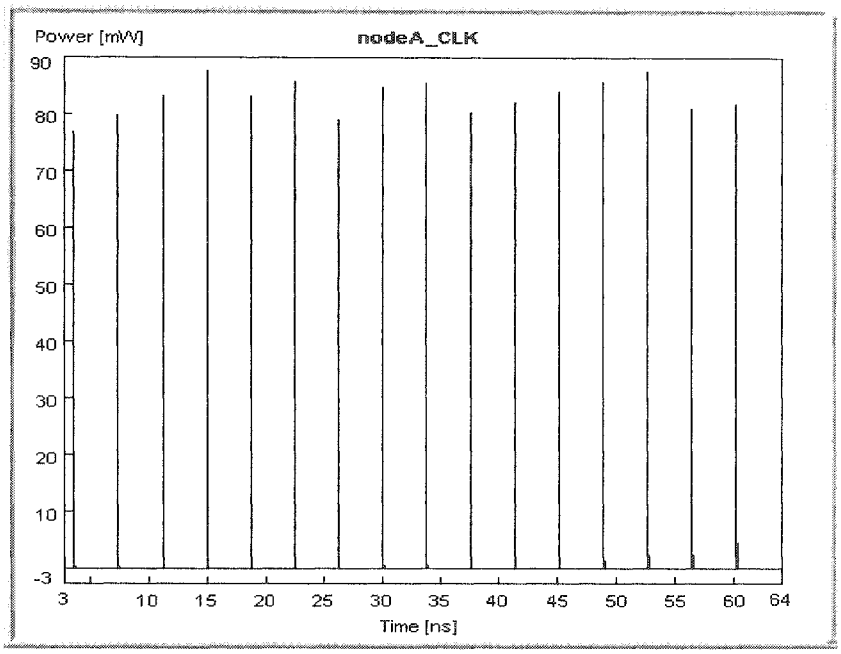
$$\tau_{tot} = 2^N \times T_s + 2T_b, \tag{4.14}$$

where $2^N \times T_s$ is the duration of a 2^N-slot PPM-frame, and $2T_b$ are the required processing time for the CEM module and the AND gate operation.

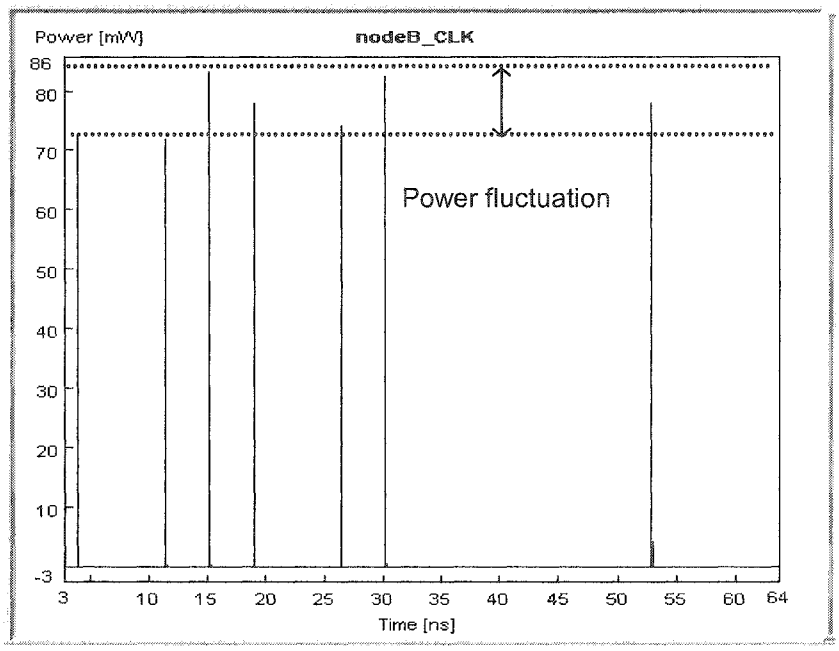
The time waveforms of sixteen input packets and their switched versions at the outputs of four nodes (A, B, C and D) are illustrated in Figure 4.7.



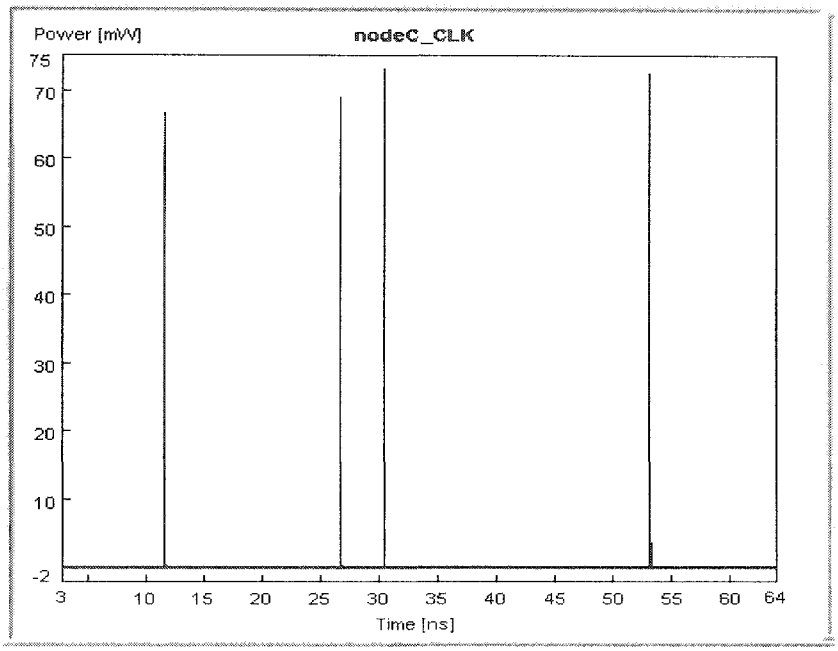
(a)


Power [mW]
nodeA_CLK
90
80
70
60
50
40
30
20
10
-3
3
10
15
20
25
30
35
40
45
50
55
60
64
Time [ns]

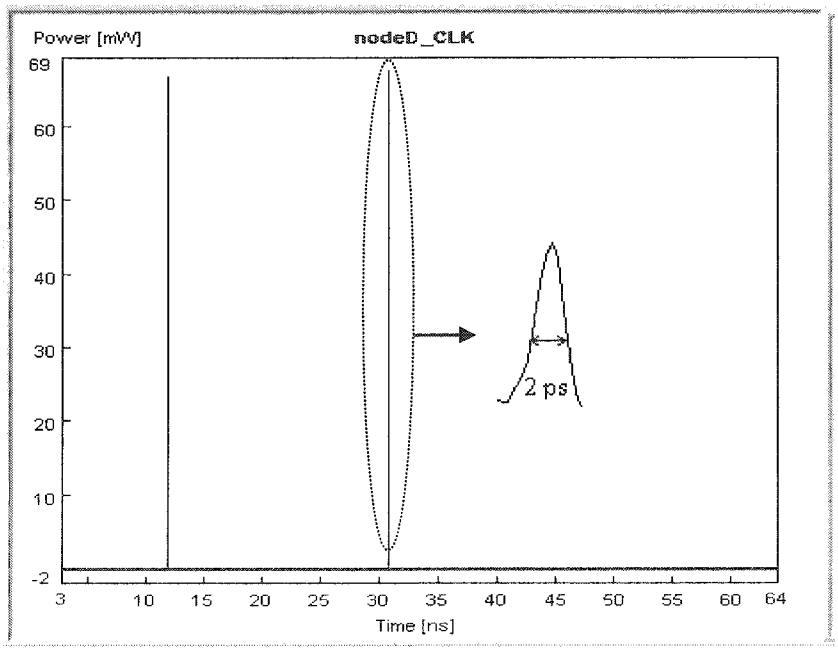
(b)


Power [mW]
nodeB_CLK
86
80
70
60
50
40
30
20
10
-3
Power fluctuation
3
10
15
20
25
30
35
40
45
50
55
60
64
Time [ns]

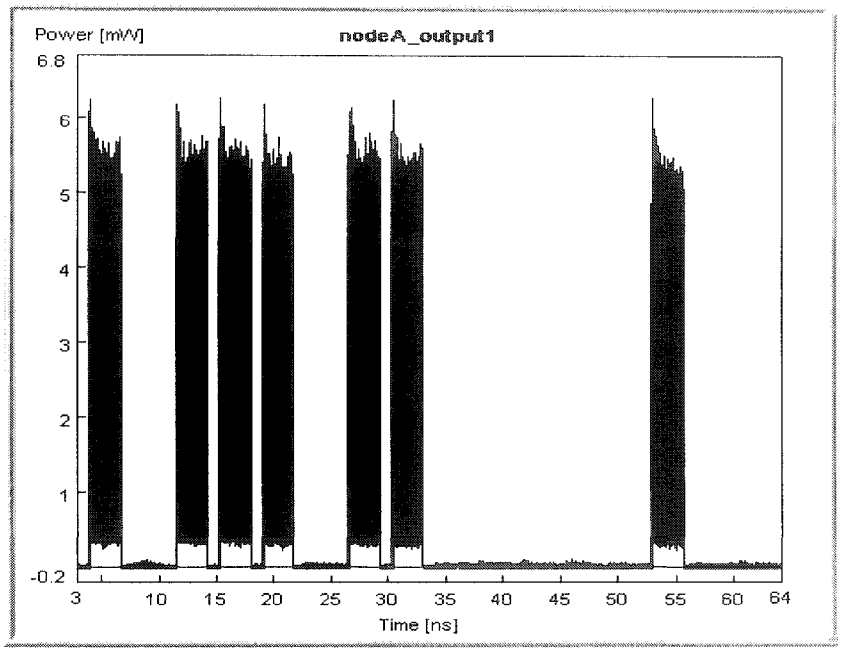
(c)


Power [mW]
nodeC_CLK
75
70
60
50
40
30
20
10
-2
3
10
15
20
25
30
35
40
45
50
55
60
64
Time [ns]

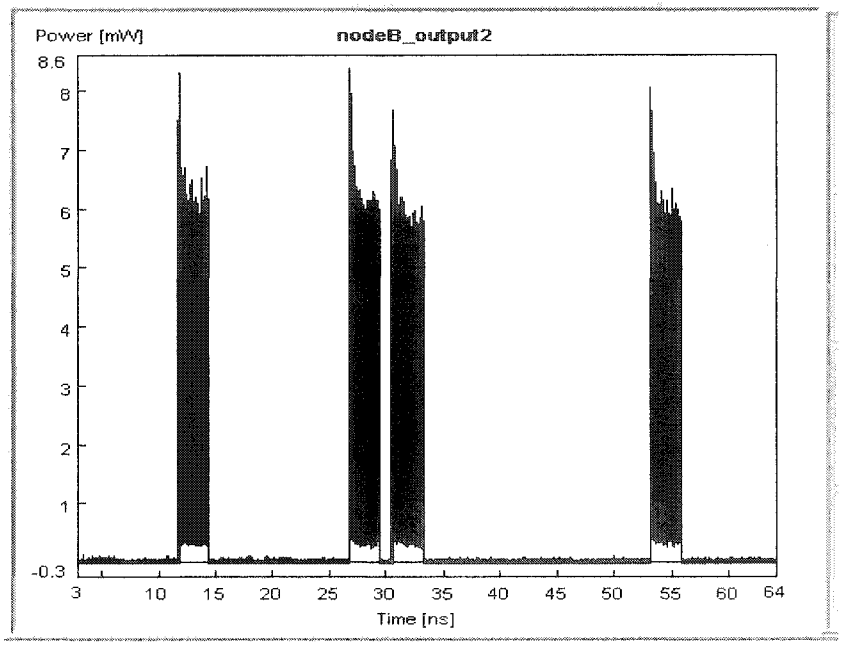
(d)


Power [mW]
nodeD_CLK
69
60
50
40
30
20
10
-2
3
10
15
20
25
30
35
40
45
50
55
60
64
Time [ns]
2 ps

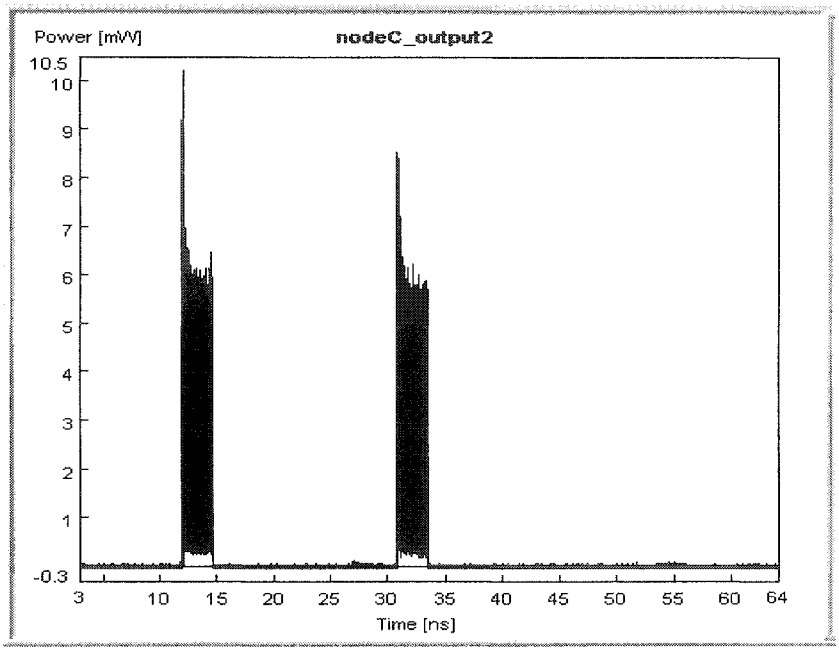
(e)


Power [mW]
nodeA_output1
6.8
6
5
4
3
2
1
-0.2
3
10
15
20
25
30
35
40
45
50
55
60
64
Time [ns]

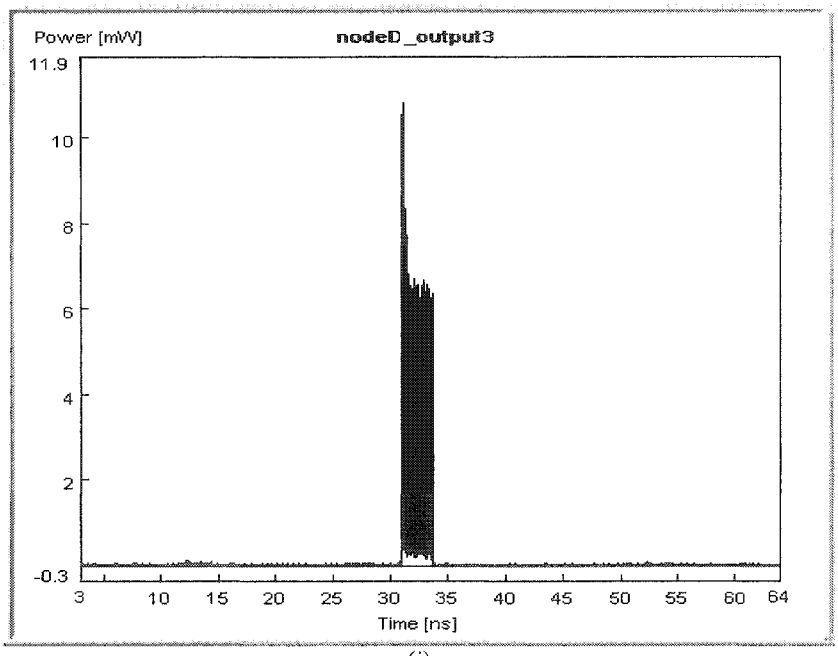
(f)


Power [mW]
nodeB_output2
8.6
8
7
6
5
4
3
2
1
-0.3
3
10
15
20
25
30
35
40
45
50
55
60
64
Time [ns]

(g)



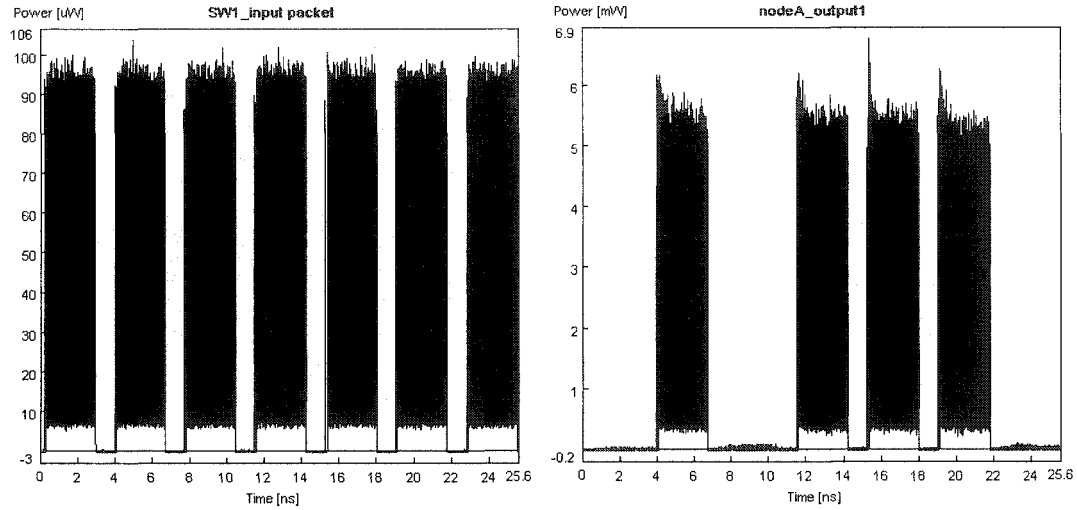
(h)



(i)

Figure 4.7 Time waveforms; (a) input packet packets at node A, (b) extracted clock at node A, (c) extracted clock at node B, (d) extracted clock at node C, (e) extracted clock at node D, (f) switched packets at node A – output1, (g) switched packets at node B – output2, (h) switched packets at node C – output2, and (i) switched packets at node D – output3 (also see the enlarged waveforms)

Figure 4.7(a) shows the input packets with the inset illustrating the zoomed-in PPM address corresponding to a decimal metric of #7. The extracted clock pulses observed at nodes A, B, C and D are presented in Figure 4.7(b)-(e), respectively, showing small intensity variations, power fluctuation of the extracted clock signals will incur different pulse power for the PPRT entries, thus resulting in power fluctuation of the switched packets, see Section 6.4 for more explanations. Packets with a large intensity fluctuation will deteriorate the system performance [149, 236]. At each hop, input packets are switched to their corresponding output ports depending on node's PPRT. Packets with target address of #7 are subsequently switched to the outputs 1, 2, 2 and 3 of nodes A, B, C and D, respectively, Figure 4.7(f), (g), (h) and (i).



(a) (b)

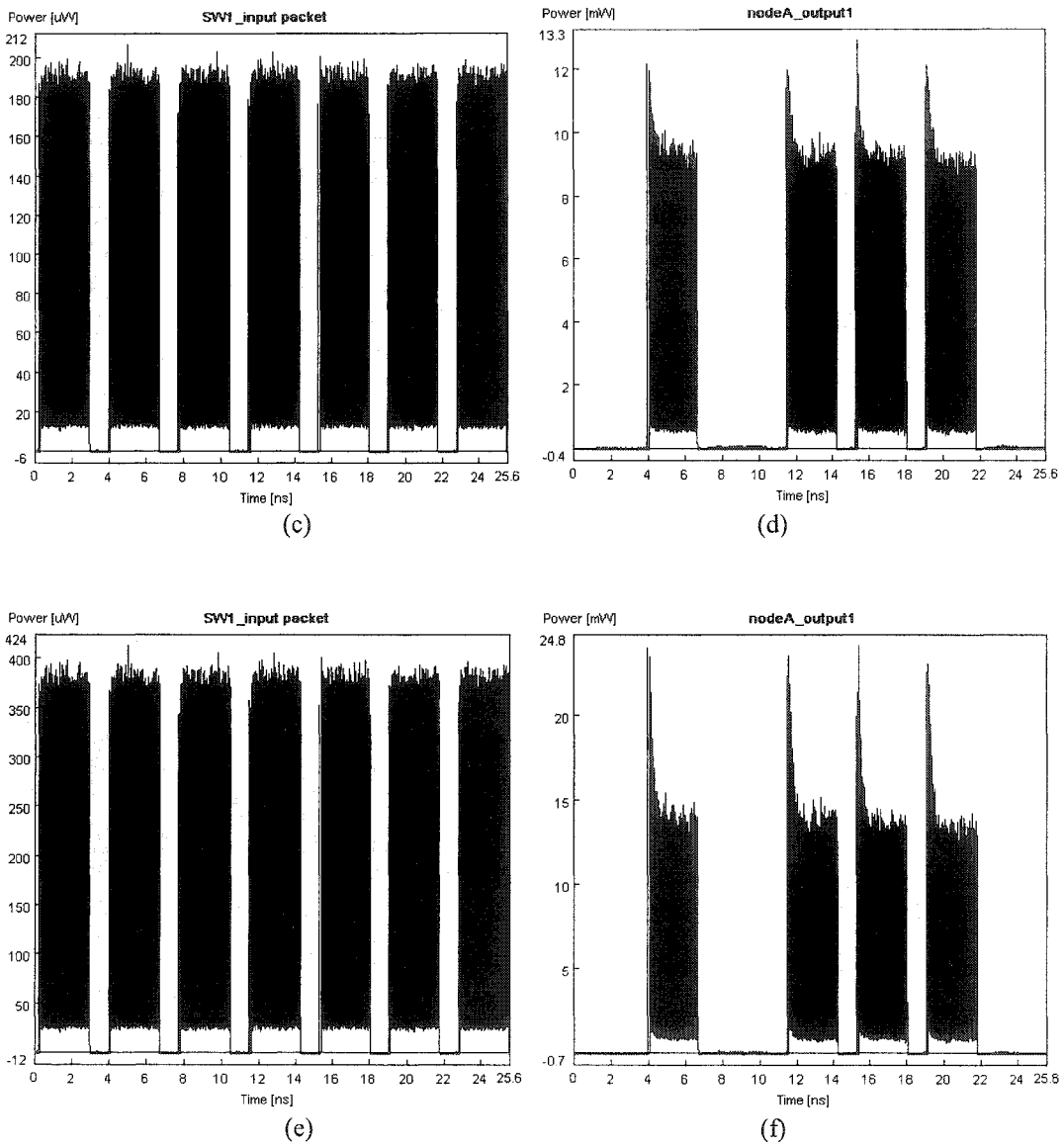
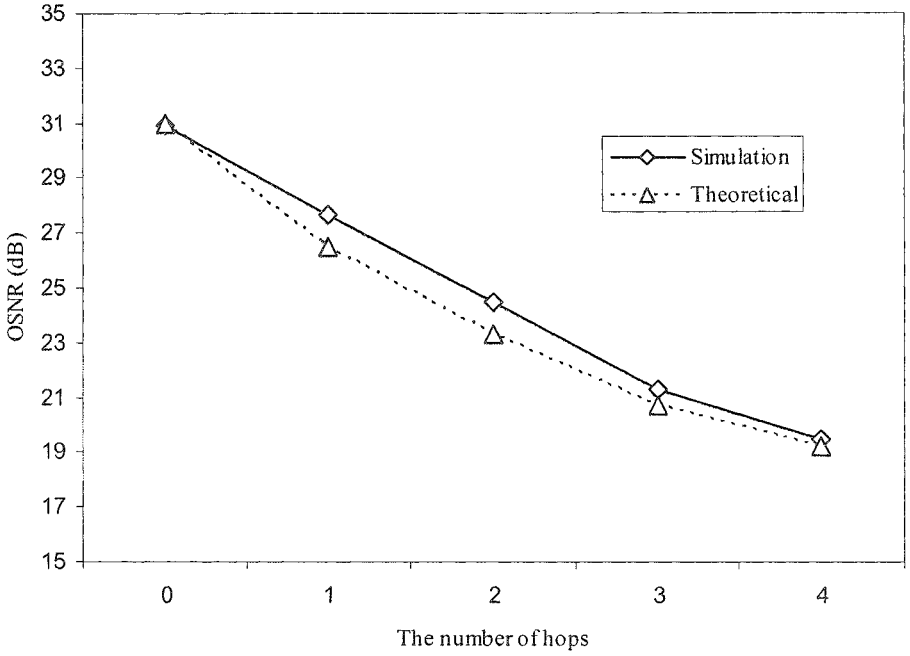
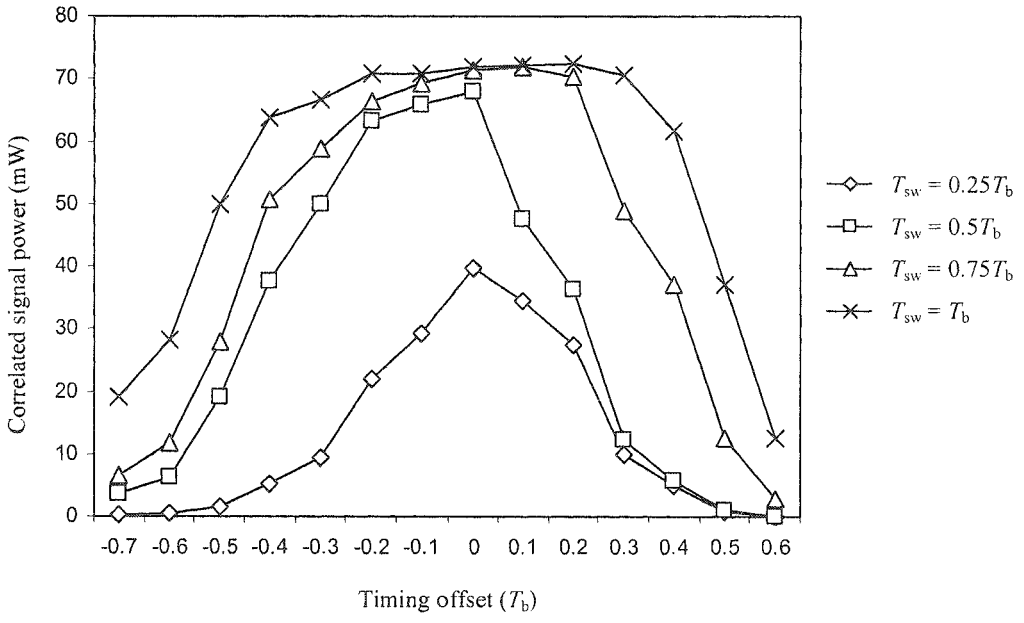


Figure 4.8 Time waveforms; (a) input packet packets at node A - OS1 (average input packet power = 100 μW), (b) switched packets at node A – output1 (average input packet power = 100 μW), (c) input packet packets at node A - OS1 (average input packet power = 200 μW), (d) switched packets at node A – output1 (average input packet power = 200 μW), (e) input packet packets at node A - OS1 (average input packet power = 400 μW), (f) switched packets at node A – output1 (average input packet power = 400 μW)

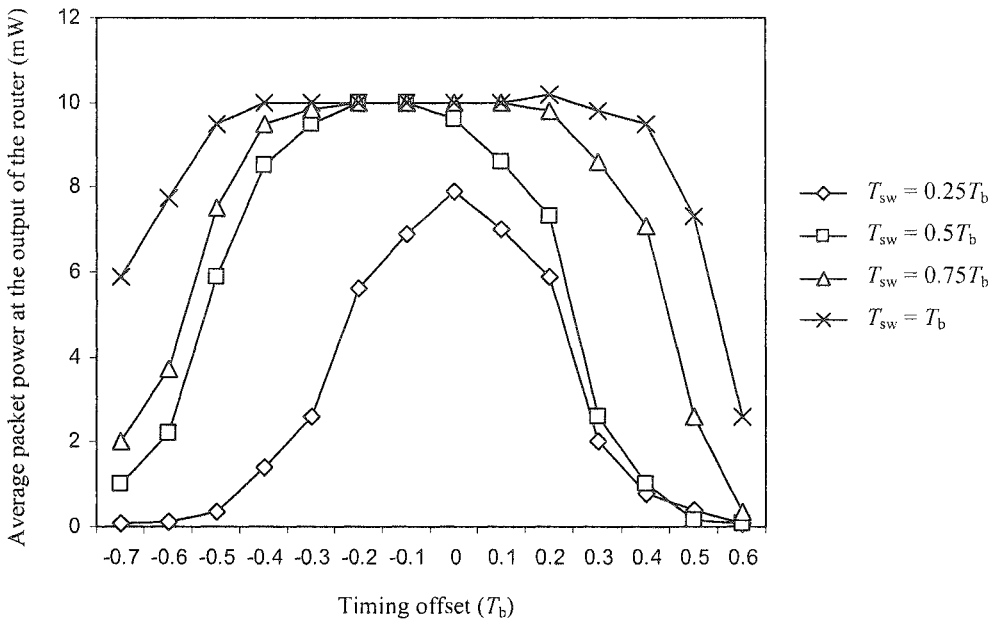
The intensity overshot observed at the start of switched packets is due to the gain saturation of the SOA in OS when injected with a number of input packets, where the proceeding bits will experience a lower amplification gain. This can be minimized by decreasing the power of input packet, see Figure 4.8. There is a trade-off between the intensity overshot and the average power of the switched packets.


35
33
31
29
27
25
23
21
19
17
15
OSNR (dB)
0
1
2
3
4
The number of hops
Simulation
Theoretical

(a)


80
70
60
50
40
30
20
10
0
Correlated signal power (mW)
-0.7 -0.6 -0.5 -0.4 -0.3 -0.2 -0.1 0 0.1 0.2 0.3 0.4 0.5 0.6
Timing offset (T_b)
$T_{sw} = 0.25T_b$
$T_{sw} = 0.5T_b$
$T_{sw} = 0.75T_b$
$T_{sw} = T_b$

(b)



(c)

Figure 4.9 (a) OSNR against the number of hops, (b) power of correlated signal $m_k(t)$, and (c) the average packet power at the output of the router

Figure 4.9(a) depicts the theoretical and simulation optical signal to noise ratio (OSNR) against the number of hops. The small difference between the results is mainly due to the intensity overshoot and power fluctuation of simulated packets, see Figure 4.7. The drop of 3 dB in the OSNR, after each hop, is due to the accumulated ASE noise. The affects of $X_{PPM}(t)$ timing-offset on the correlated signal $m_k(t)$ and the average packet power at the output of the router for a range of T_{sw} are depicted in Figure 4.9(b) and (c), respectively. For all values of T_{sw} maximum power is observed at $\tau_{os} = 0$, i.e. when the target signal is at the centre of the SW. For $T_{sw} = 0.25\ T_b$, the correlated output power is significantly lower over a shorter range of τ_{os}. This is because of a narrow SW only passing through part of the target signal. For $T_{sw} \geq 0.75\ T_b$ the targeted pulse is located within a wider SW, therefore maximum powers are observed over a much wider range of τ_{os}. However, a wider SW will result in switching the non-target signal, i.e. intra-channel crosstalk.

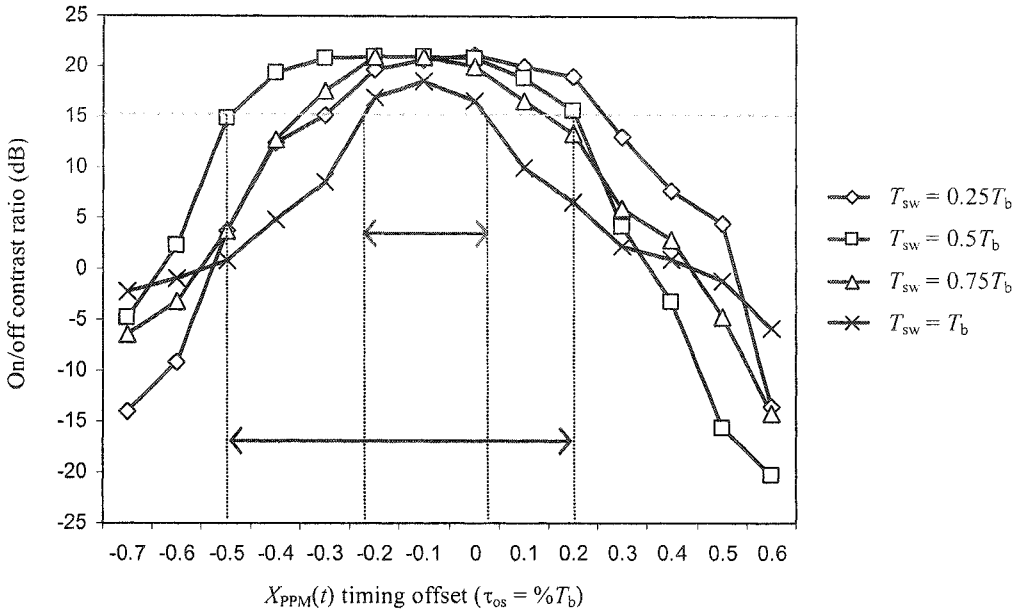


Figure 4.10 The on/off contrast ratio against the timing offset of PPM address

The affect of the timing offset could be evaluated by investigating the on/off contrast ratio $r_{on/off}$, which is defined as $10\log_{10}$ (desired output packet power - undesired output packet power). From Figure 4.10, the peak value of $r_{on/off}$ is ~20 dB over a wide range of timing offset (0.25 T_b, 0.5 T_b and 0.75 T_b). T_{sw} of 0.5 T_b offers the widest offset range of ~0.8 T_b. For $T_{sw} > < 0.5\ T_b$ the power level sharply drops form it maximum value due to switching of incomplete desired and undesired signals, respectively.

4.6 Summary

In this chapter, the PPM based packet header address format was introduced, where address modification (i.e. binary to PPM address conversion) is no longer a requirement in each switching node across the optical core network, thus significantly reducing the system complexity. The node architecture was present in Section 4.2, and the OSC module and OSNR performance are shown in Sections 4.3 and 4.4,

respectively. In Section 4.5, the proposed schemes was simulated and the simulation results obtained showed that the correlated packet header address power and switched signal on/off contrast ratio largely depends the switching window width and the timing offset of the PPM header address. The proposed router offers fast processing time of 112.5 ps (i.e. ~ 100 times faster than router using CRT and reduced system complexity and is capable of operating in the unicast, multicast and broadcast transmission modes.

CHAPTER 5 ULTRA-FAST ALL-OPTICAL PACKET SWITCHED ROUTER WITH MULTIPLE PPRTS

5.1 Introduction

Currently packet header recognition is carried out by sequentially correlating the incoming packet header address with every entry of a local router routing table. For a small size network this is achievable provided the routing table size is small. However, for a large size network requiring a routing table of more than half a million entries, cost and complexity become a real issue. In addition a larger routing table will contribute to an increase in processing time at every router.

In this chapter, an all-optical packet switched router using a new packet header address correlation scheme based on the pulse-position-modulation (PPM) signalling format is proposed. Both the packet header address and all the routing table entries are represented in PPM-format and multiple pulse-position routing tables (multiple PPRTs), respectively. Multiple PPRTs not only downsize the routing table size, but it also offers robust header recognition capability using only a single optical AND operation. In Multiple PPRTs only a subset of the header address is converted into a PPM format, thus resulting in a reduced length of PPRT entries. As a result, the router with multiple PPRTs offers faster header recognition time (i.e. faster router's processing time).

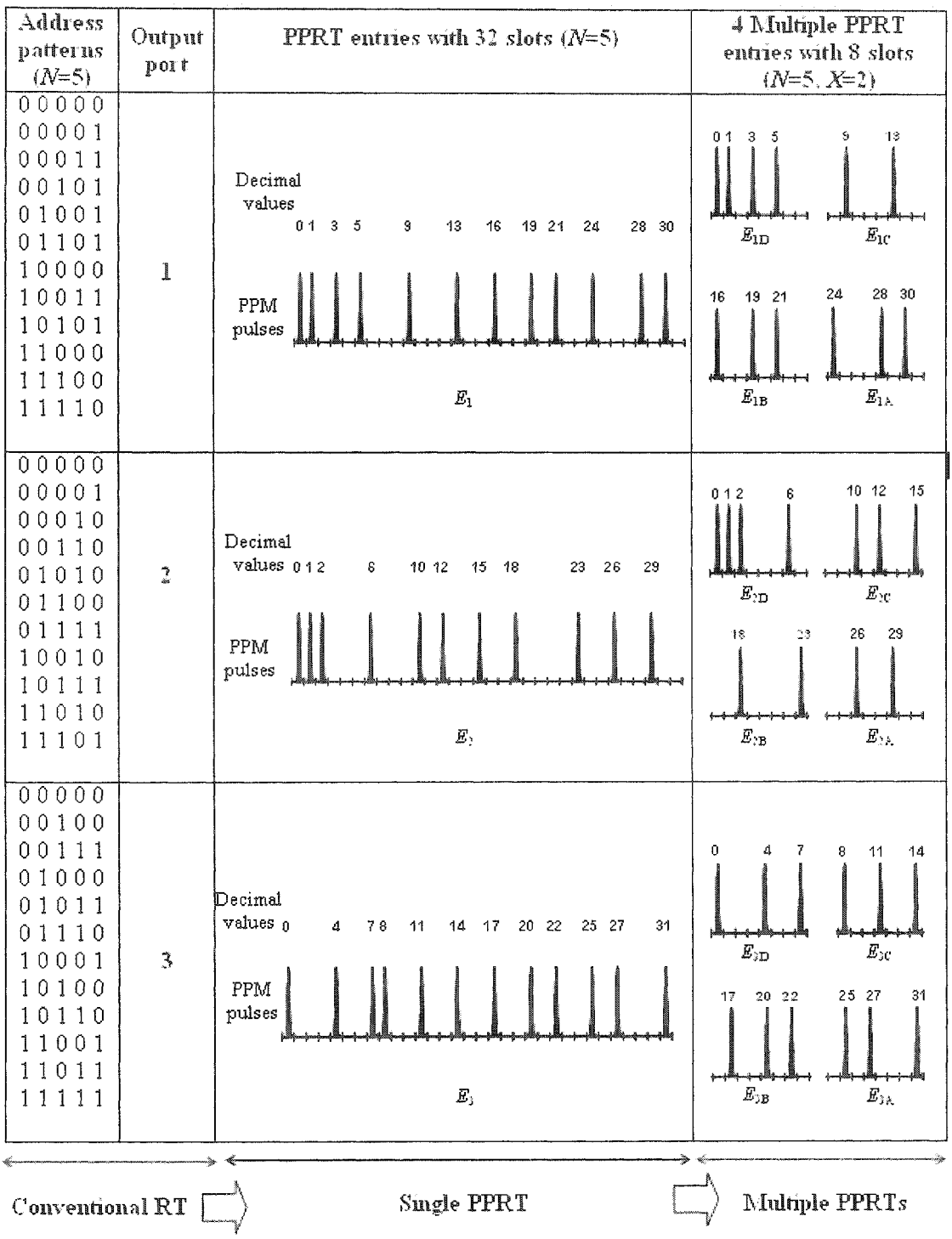
This chapter is organised as follows: The concepts of multiple PPRTs and multiple PPRT generator are explained in Sections 5.2 and 5.3, respectively. The proposed

node architecture is shown in Section 5.4. The simulation results are discussed in Section 5.5. Finally, Section 5.6 will conclude this chapter.

5.2 Multiple-PPRTs

Assuming a packet header with N-bit address [a_{N-1} a_{N-2} ... a_2 a_1 a_0], where a_{N-1} is the most significant bit (MSB), the conventional RT will have a maximum of 2^N entries. A router makes a routing decision by correlating and matching the packet header address with a unique entry in the routing table. In the worst case scenario, i.e. where all possible entries are checked (exhaustive correlation), the router needs to perform 2^N N-bitwise correlations. Table 5.1 illustrates a routing table for N = 5, where 32 possible addresses are grouped into M groups, (M = 3, for example, is the number of node outputs), each has address patterns having the same associated router output. If a packet address matches a pattern in that group, the packet will be switched to its associated output, see the 1st and 2nd columns. In the 3rd column, each group is converted into a single entry PPRT E_i (i = 1,2, 3..) of length $2^N \times T_s$, where T_s is the slot duration and the locations of short pulses corresponding to the decimal values of address patterns in i^{th} group. Note the number of entries is reduced from 32 for conventional RT to 3 for single PPRT.

Table 5.1 The conversion of conventional RT to single PPRT and multiple PPRTs



Further downsizing in PPRT could be made by splitting each PPRT entry into a group of PPRTs E_{ij} (i = 1,2, 3.., and j = A,B, C ..) with a reduced entry length of $2^{N-X} \times T_s$ (where N–X is the number of bits in the subset of packet header address being

converted to PPM address), see the 4th column in Table 5.1 For example for $N = 5$, the PPRT entry length is reduced from $32 \times T_s$ to only $8 \times T_s$ when $X = 2$. A, B, C and D represent address patterns with the decimal metrics in the range of (24-31), (16-23), (8-15) and (0-7), respectively.

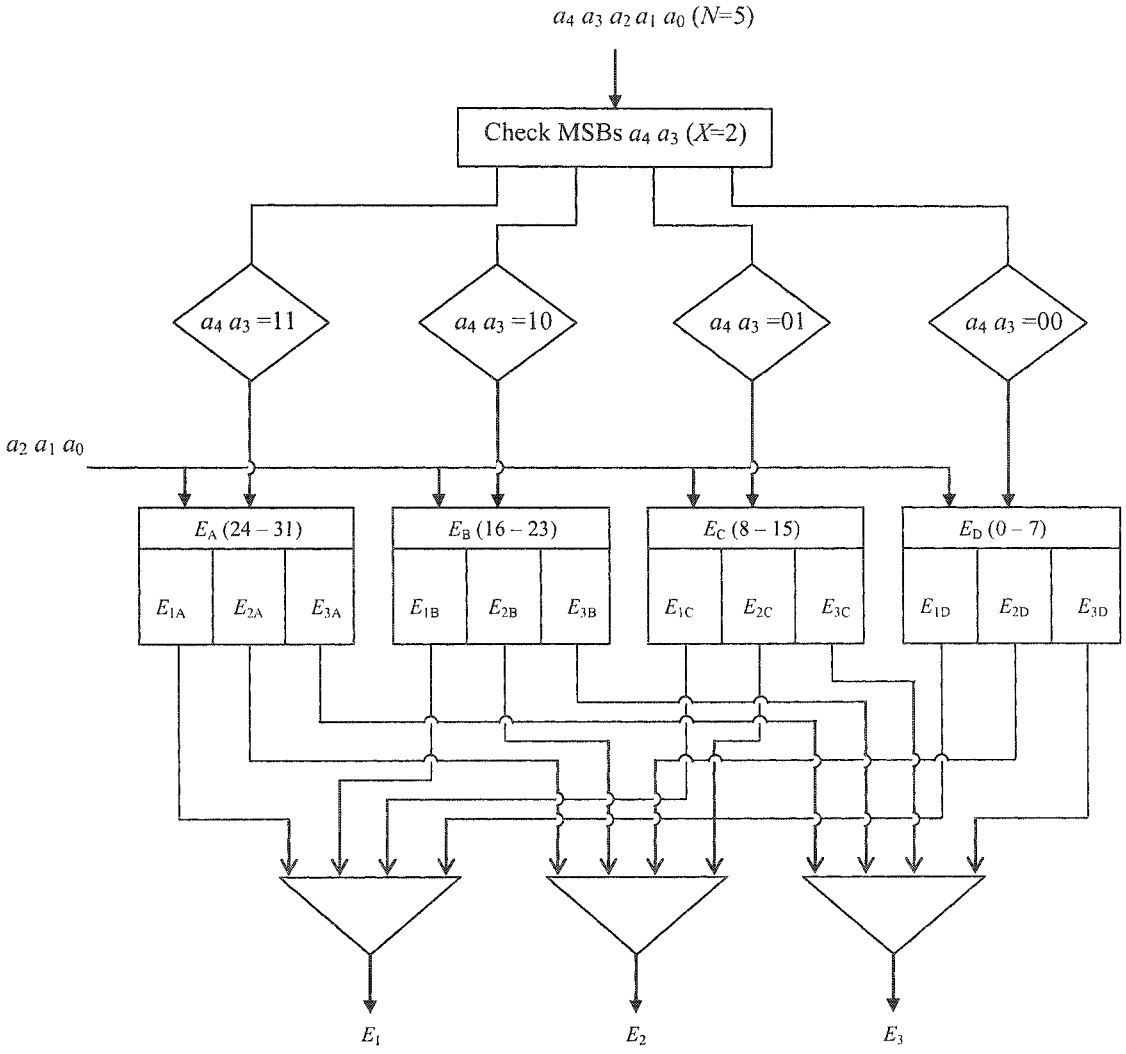


Figure 5.1 A block diagram of multiple PPRT (E_{1A}, E_{2A}, E_{3A}, …, E_{3D}) for 5-bit packet header address

The process is best explained with reference to Figure 5.1 ($N = 5$, $X = 2$) where the two MSBs a_4 and a_3 of 5-bit header address are checked to identify the PPRT entry. Based on the combination of (a_4, a_3), E_{ij} is generated from the remaining $a_2a_1a_0$. The outputs of multiple E_{ij} are combined to generate E_1, E_2 and E_3, which are then applied

to the AND gates to carry out header address correlation. The architecture of the multiple PPRT generators will be discussed in the following sections.

5.3 Multiple-PPRT Generator

The multiple PPRT entries (pulses) are generated from the extracted clock pulse of the input packet. The architecture of the multiple PPRT generator is illustrated in Figure 5.2. A multiple PPRT generator (for X=2) is composed of three 1×2 high CR switches, four $1\times2^{N-2}$ splitters, up to 2^N delay units and M ($N_m\times1$) combiners, where N_m is the total number of pulses in E_m.

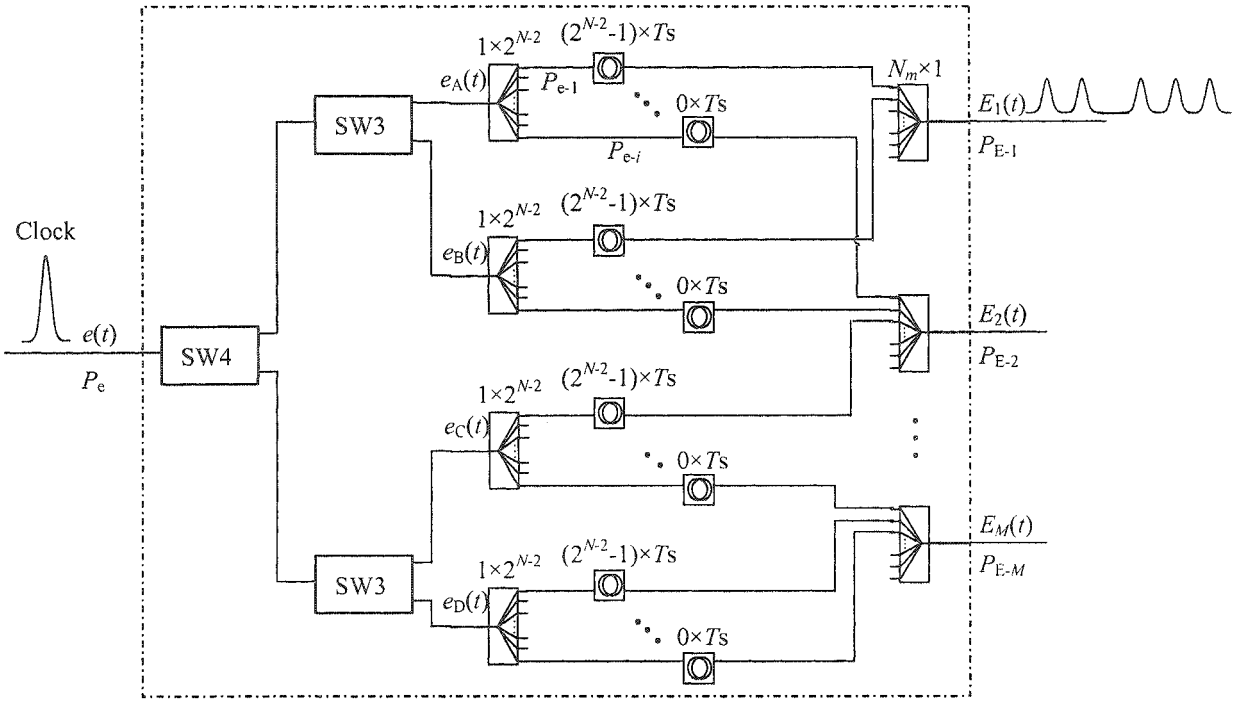


Figure 5.2 Multiple PPRT generator (for X=2)

To generate the multiple PPRT entries, the input pulse $e(t)$ is passed through two stages of amplification (i.e. SW4 and SW3). The output pulse of SW3 $e_{A,B,C,D}(t)$ (depending on the values of the two MSBs of the incoming packet address) is then

passed through the $1\times2^{N-2}$ splitter, the output of which is delayed before being recombined. A maximum number $N_{m,\text{tot}}$ of 2^N delay paths is required for multiple PPRT generation when the conventional routing table contains all 2^N possible entries. Assuming that the input power is P_e, the power of the i^{th} delay path $P_{e\text{-}i}$ (in dB) is given as:

$$P_{e-i}(\text{dB}) = 10\log_{10}(P_e) + G_4 + G_3 - L_{\text{splitter}} - L_{\text{combiner}} - 10\log_{10}(N_{m,\text{tot}}), \qquad (5.1)$$

where G_4 and G_3 are the amplification gain from SW4 and SW3, respectively. The insertion loss of the splitter and combiner are L_{splitter} and L_{combiner}, respectively.

Assuming that the combiner output E_m has N_m dedicated bit "1"s (i.e. $N_{m,\text{tot}} = \sum_{m=1}^{M} N_m$), the output power $P_{E\text{-}m}$ is given as:

$$P_{E-m}(\text{dB}) = 10\log_{10}(P_{e-i}) - L_{\text{splitter}} - L_{\text{combiner}}. \qquad (5.2)$$

Substituting for $P_{e\text{-}i}$ from (5.1) results in:

$$P_{E-m}(\text{dB}) = P_e(\text{dB}) - L_{\text{MPPRT}}, \qquad (5.3)$$

where the total power loss due to multiple PPRT generator L_{MPPRT} (in dB) is determined by:

$$L_{\text{MPPRT}} = 2L_{\text{splitter}} + 2L_{\text{combiner}} - G_4 - G_3 + 10\log_{10}(N_{m,\text{tot}}). \qquad (5.4)$$

Note that as the number of the packet address N increases, a higher input power P_e or a higher gain of 1×2 high CR switches are required to compensate for the power loss of the multiple PPRT pulses.

5.4 Node Architecture

The router based on multiple PPRT with M-output ports is composed of a number of main modules including a clock extraction module (CEM), a PPM address conversion module (PPM-ACM), a serial-to-parallel converter (SPC), a multiple PPRT generator, AND gates, all-optical switches (OS), an OS control module (OSC), and a number of 1×2 high extinction ratio all-optical switches (SW) [237], see Figure 5.3. The incoming packet $P(t)$ is split and applied to the CEM, SPC and OS with the delays of 0, τ_{CEM} (required time for clock extraction) and τ_{tot} (total required time for PPM header processing), respectively. The extracted clock pulse $c(t)$ from the CEM based on two cascading SMZ switches [224] is applied to the SPC [238], PPM-ACM and SW4 with the delays of 0, τ_{AC} and τ_{PPRT}, respectively, for extracting address bits, converting address bits to PPM format and generating multiple PPRTs, respectively. At the input of the PPM-ACM the signal $x(t)$ is $\alpha c(t + \tau_{AC})$ where α is the splitting factor. N-bit packet header address extracted from the delayed packet $\alpha P(t + \tau_{CEM})$ by the SPC is applied to the PPM-ACM with the output defined by:

$$x_{PPM}(t) = x\left(t + \sum_{i=0}^{N-3} a_i \times 2^i \times T_s\right), \qquad a_i \in \{0,1\}. \tag{5.5}$$

A fraction of the extracted single clock pulse $c(t)$ is input into SW4 switch and a pair of SW3 switches, to check the status of a_4 and a_3, respectively. SW4 is controlled by a_4 and its outputs are sequentially applied to both SW3 controlled by a_3. The input pulse will emerge at one of four outputs of SW3s as single pulse e_A, e_B, e_C or e_D to generate corresponding E_{ij}. PPRTs with the same i^{th} index will be combined together and applied to the optical AND gates for address correlation. Note that, only one

multiple PPRT is used for correlation with an incoming packet header address. The outputs of PPRT entries (with $X = 2$, see Table 5.1) are given by:

$$E_{kA}(t) = \begin{cases} \sum_{d_k} e_A\left(t + (d_k - 2^{N-1} - 2^{N-2}) \times T_s\right), & if \quad (a_{N-2}, a_{N-1}) = (1,1) \\ 0, & otherwise \end{cases} \quad , \forall\, d_k \in \left\{(2^{N-1} + 2^{N-2}) \sim (2^N - 1)\right\}$$

$$E_{kB}(t) = \begin{cases} \sum_{d_k} e_B\left(t + (d_k - 2^{N-1}) \times T_s\right), & if \quad (a_{N-2}, a_{N-1}) = (0,1) \\ 0, & otherwise \end{cases} \quad , \forall\, d_k \in \left\{2^{N-1} \sim (2^{N-1} + 2^{N-2} - 1)\right\}$$

$$E_{kC}(t) = \begin{cases} \sum_{d_k} e_C\left(t + (d_k - 2^{N-2}) \times T_s\right), & if \quad (a_{N-2}, a_{N-1}) = (1,0) \\ 0, & otherwise \end{cases} \quad , \forall\, d_k \in \left\{2^{N-2} \sim (2^{N-1} - 1)\right\}$$

$$E_{kD}(t) = \begin{cases} \sum_{d_k} e_D\left(t + d_k \times T_s\right), & if \quad (a_{N-2}, a_{N-1}) = (0,0) \\ 0, & otherwise \end{cases} \quad , \forall\, d_k \in \left\{0 \sim (2^{N-2} - 1)\right\}.$$

(5.6)

The outputs of the multiple PPRTs, see Figure 5.1 and Figure 5.3, are given as:

$$E_k(t) = E_{kA}(t) + E_{kB}(t) + E_{kC}(t) + E_{kD}(t), \tag{5.7}$$

where each d_k element corresponds to the decimal values of header address bits assigned to the node output k^{th} ($k = 1, 2, \ldots, M$).

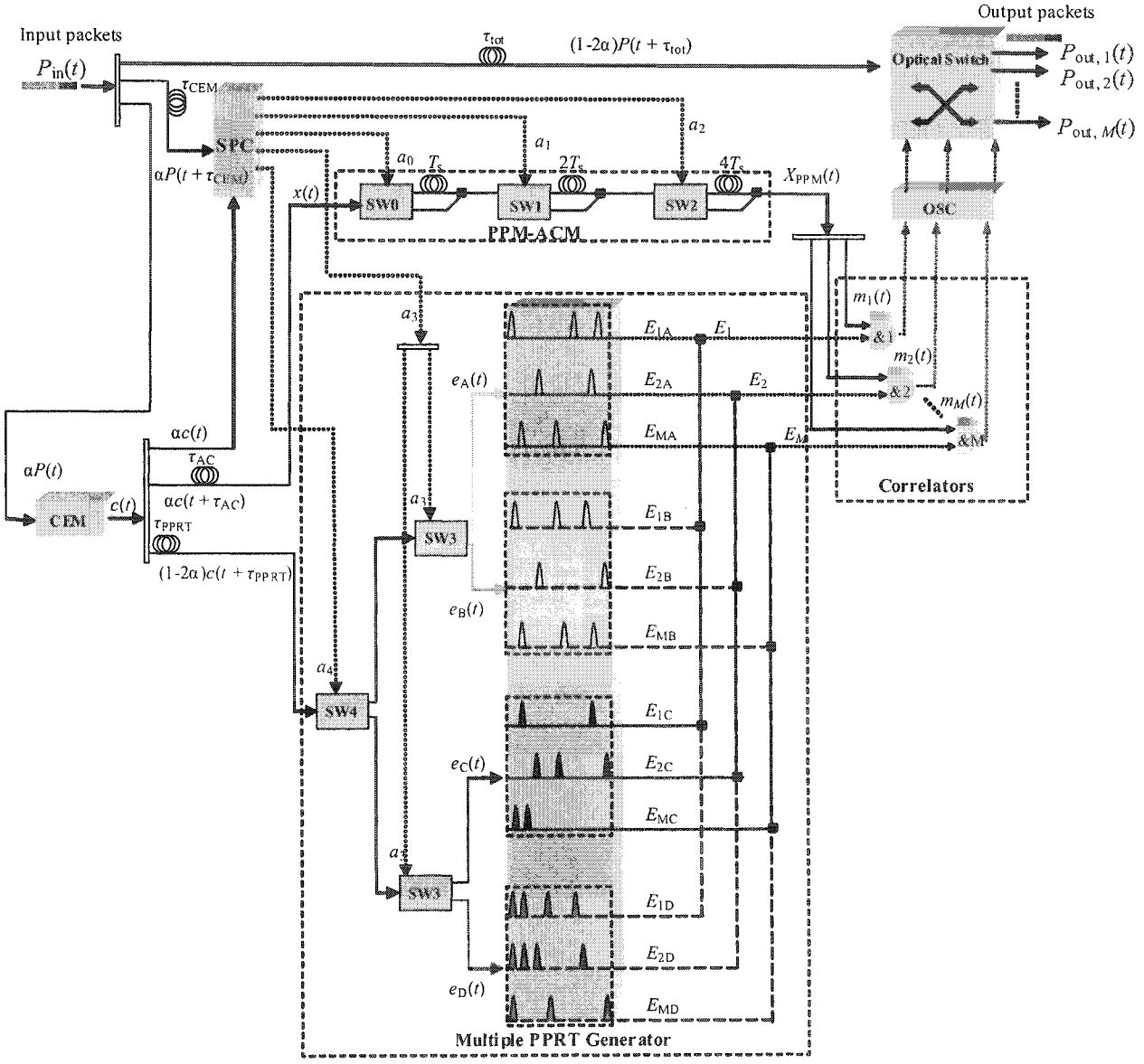


Figure 5.3 A schematic block diagram of node structure with multiple PPRTs for 5-bit packet header address ($N = 5, X = 2$)

The header address recognition is carried out by correlating the PPM address (converted from only three bits $a_2a_1a_0$ in this case) with one of the multiple PPRTs (depending on the combination of a_4a_3) using a single AND gate, see Figure 5.4. For example a header address of "11**100**" converted into a PPM format shows a pulse located at the 4th position (i.e. decimal value of "100") in an 8-slot PPM address. The two MSBs ("11") are used to select one of the multiple PPRTs for correlation. The

optical AND gates are based on the SMZ switches [227] with the logical outputs given by:

$$m_k(t) = x_{PPM}(t) \times E_k(t) = \begin{cases} 1 & if \quad d_k = \sum_{i=0}^{N-1} a_i \times 2^i \quad \forall k \\ 0 & if \quad d_k \neq \sum_{i=0}^{N-1} a_i \times 2^i \quad \forall k \end{cases}, \tag{5.8}$$

$$k = 1,2,...,M \qquad d_k \in \{0 \sim (2^N - 1)\}.$$

The matching pulse $m_k(t)$ is subsequently applied to the OSC module to ensure that packets are switched to the correct output ports. The signal at the output of switch is given as:

$$P_{out,k}(t) = P_{in}(t) \times m_k(t) = \begin{cases} G_{OS} \times (1 - 2\alpha) \times P_{in}(t + \tau_{tot}) & if \quad m_k(t) = 1 \\ 0 & if \quad m_k(t) = 0 \end{cases}, \tag{5.9}$$

$$k = 1,2,...,M$$

where G_{OS} is the optical switch gain.

If more than one pulse is located at the same position in more than one or in all PPRT entries, then a packet is broadcasted to multiple outputs (i.e. multicast) or all outputs (i.e. broadcast), respectively.

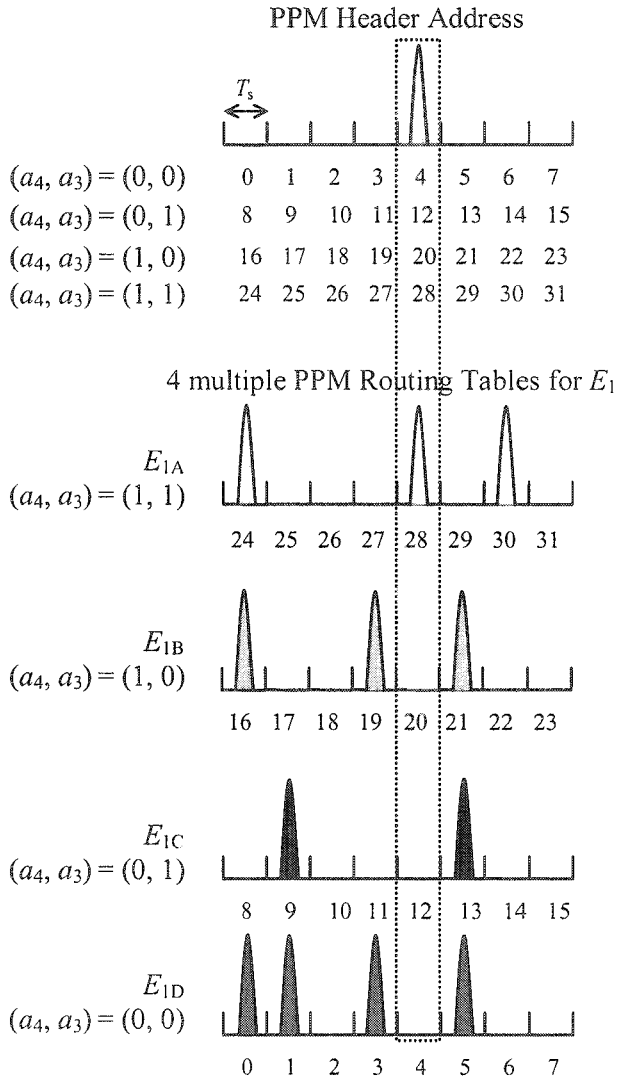


Figure 5.4 Correlation between PPM address with one of 4 multiple PPRT entries

The address correlation time (or header recognition time) of the multiple PPRTs scheme is determined by the duration of a 2^{N-2}-slot PPM-frame as:

$$T_{\text{MPPRT}} = 2^{N-2} \times T_s . \tag{5.10}$$

In the conventional address correlation scheme, header recognition is carried out by sequentially correlation the address bits with every entry of the CRT. The required header recognition time of the CRT scheme T_{CRT} is defined as:

$$T_{CRT} = 2^N \times N \times T_{AND} \times M^{-1}, \tag{5.11}$$

where M is the number of the router's output ports, T_{AND} is the minimum time interval required for two successive AND operations, which is limited by the SOA recovery time. Typically T_{AND} (hundreds of picoseconds) is much greater than T_b (few picoseconds) in high-speed optical networks (bit rate > 40 Gb/s).

Comparing this with the CRT, the correlation-time gain by employing Multiple PPRTs R_{MPPRT} is defined as the ratio of the time required for CRT scheme T_{CRT} over the required time for multiple PPRTs scheme T_{MPPRT}, and is given by:

$$R_{MPPRT} = \frac{4N \times T_{AND}}{M \times T_s}. \tag{5.12}$$

In this simulation (N = 5, M = 3, T_{AND} = 500 ps [56] (also see APPENDIX – C), T_s = 12.5 ps), the correlation-time gain, R_{MPPRT} is equal to 266.67.

5.5 Simulation Results

The proposed router is simulated and its system performance is investigated by using the Virtual Photonics simulation package (VPI^{TM}). Table 5.2 shows the main simulation parameters [210, 216] and Figure 5.5 depicts the simulation setup diagrams for multi-hop routing and an individual router.

Table 5.2 Simulation parameters

Parameters	Values
Data packet bit rate $R_b = 1/T_b$	80 Gb/s
Packet payload length	53 bytes (424 bits)
Wavelength of data packet	1554 nm (193.1 THz)
Data & control pulse widths (FWHM)	2 ps
PPM slot duration T_s (= T_b)	12.5 ps
Average transmitted packet peak pulse power P_{in}	3.5 mW
Average pulse peak power of $C_k(t)$	165 mW
Optical bandwidth B_o	300 GHz (2.4 nm)
G_h (h = 1,2,...H)	20 dB
Total loss of a hop $1/L_h$ (h = 1,2,...H)	-7 dB
Pre-amplifier gain G_0	7 dB
First span loss $1/L_0$	-7 dB
Pre-amplifier n_{sp}	2
SOA length	500 μm
SOA n_{sp}	2
Inject current to SOA	150 mA
Splitting factor α	0.4

Six optical packets with addresses of #0, #1, #4, #12, #20 and #28 (decimal values) are transmitted sequentially at 80 Gb/s with 1 ns inter-packet guard interval. Each packet is composed of a 1-bit clock, a 5-bit address, and a 53-byte payload (ATM cell size) [83, 235]. The input packet, with an average power of 3.5 mW, is amplified to compensate for the link loss (fibre attenuation and coupling losses). Each fibre span (link) comprises of 30 km single-mode fibre (SMF) and 5 km dispersion-compensating fibre (DCF). Note that PPRT for of the node A is given in Table 5.1. Similarly, for nodes B, C, and D, the PPRT entries are $E_1 \in \{\mathbf{0}, \mathbf{1}, 2, 6, 10, \mathbf{12}, 15, 18, 23, 26, 29\}$, $E_2 \in \{\mathbf{0}, \mathbf{1}, 3, 5, 9, 13, 16, 19, 21, 24, 28, 30\}$, and $E_3 \in \{\mathbf{0}, 4, 7, 8, 11, 14, 17, 20, 22, 25, 27, 31\}$, respectively.

The total processing time of the all-optical router with multiple PPRTs, τ_{tot} (i.e. the time delay between the input packets and switched packets) in this simulation ($N = 5$, $T_s = T_b = 12.5$ ps) is equal to 187.5 ps, which is calculated as follows:

$$\tau_{tot} = 2^{N-2} \times T_s + N \times T_b + 2T_b, \tag{5.13}$$

where $2^{N-2} \times T_s$ is the duration of a 2^{N-2}-slot PPM-frame, $N \times T_b$ is the required processing time for the SPC module, and $2T_b$ is the required processing time for the CEM module and the AND gate operation.

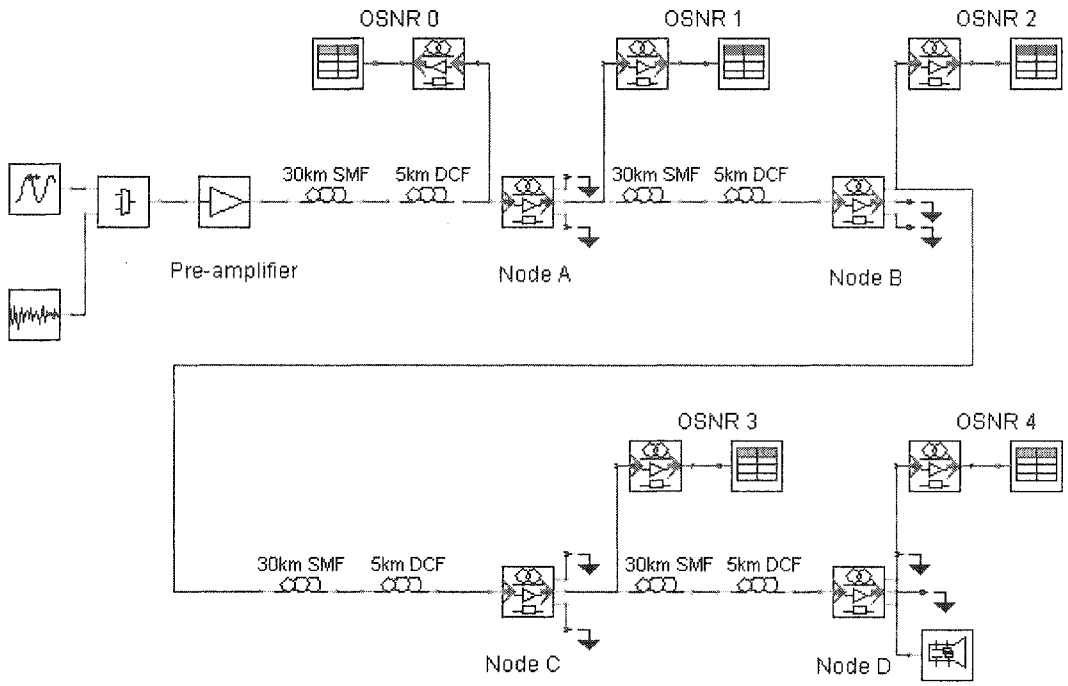
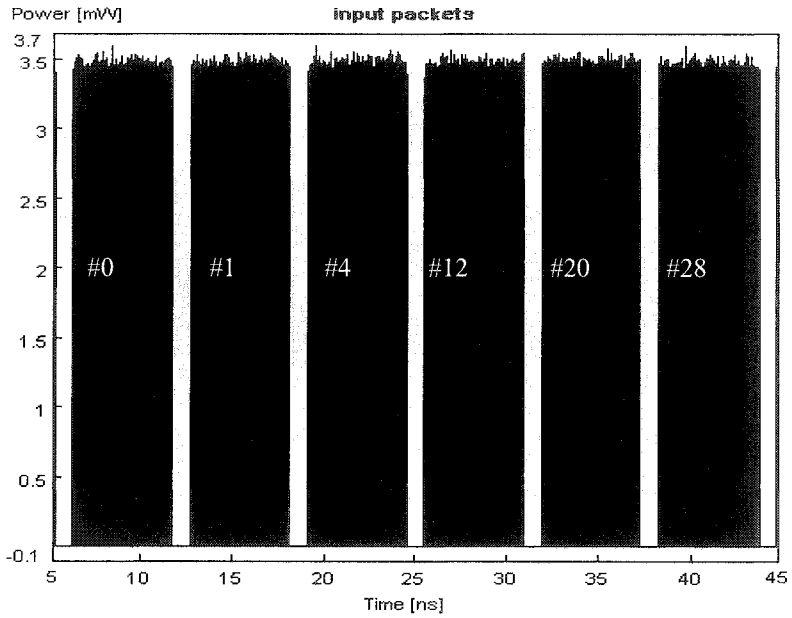


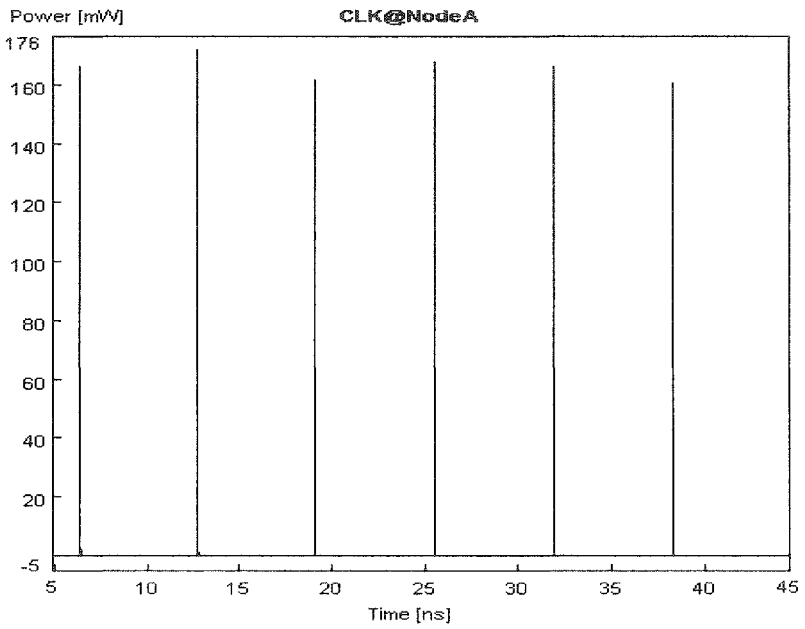
Figure 5.5 The VPI simulation setup for four-hop routing

The time waveforms of six input packets and their switched versions at the outputs of four nodes (A, B, C and D) are illustrated in Figure 5.6. Figure 5.6(a) shows the input packets, whereas the extracted clock pulses observed at nodes A, B, C and D are presented in Figure 5.6(b)-(e), respectively, showing small intensity variations. In

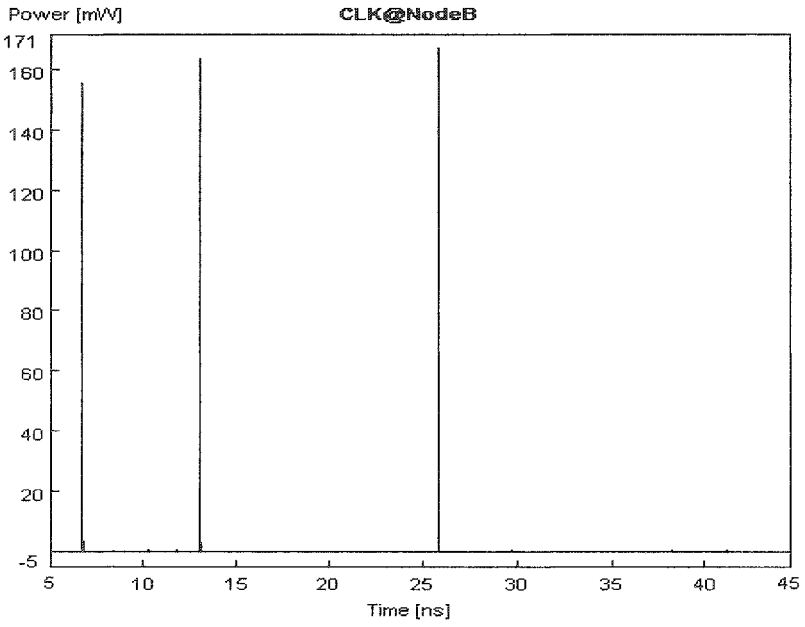
simulation inclusion of an additional noise source, see Figure 5.5, introduces small intensity variation to the input packets, thus resulting in the extracted clock signals displaying intensity fluctuation due to the amplification after being passed through the CEM module. The affects of the intensity variation will be further discussed in Section 6.4. At each hop, depending on the node's PPRT, the input packets are switched to their corresponding output ports. Packets with the target address of #0 are subsequently switched to the output ports of 2, 1, 2 and 3 of nodes A, B, C and D, respectively, as shown in Figure 5.6(f), (g), (h) and (i). The intensity overshot observed at the start of switched packets is due to the gain saturation of the SOA within the OS when injected with a number of input packets, where the proceeding bits will experience a lower amplification gain. This can be minimized by decreasing the power of the input packet.



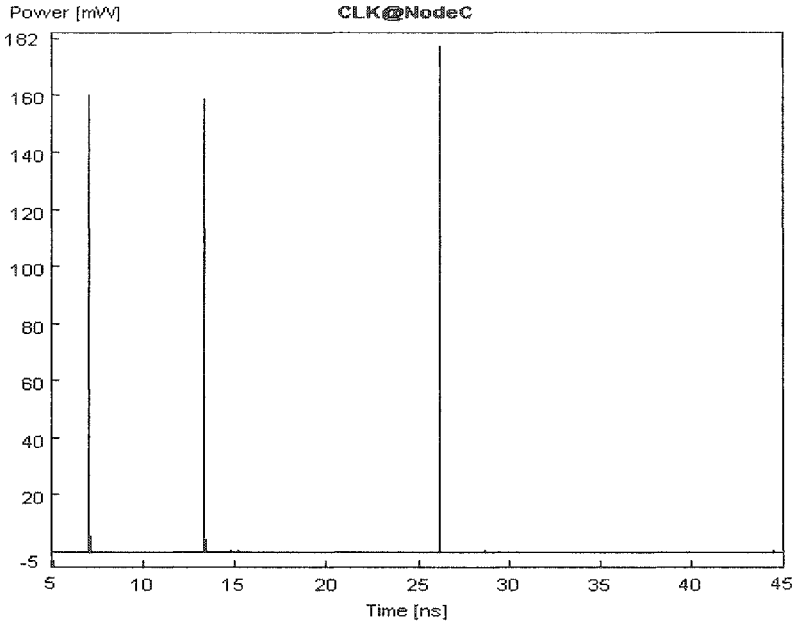
(a)


Power [mW]
CLK@NodeA
176
160
140
120
100
80
60
40
20
-5
5
10
15
20
25
30
35
40
45
Time [ns]

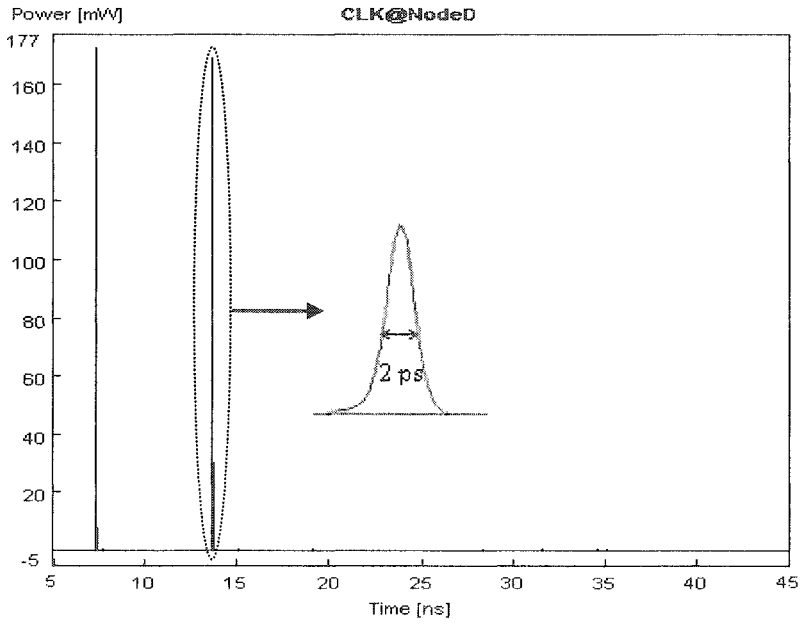
(b)


Power [mW]
CLK@NodeB
171
160
140
120
100
80
60
40
20
-5
5
10
15
20
25
30
35
40
45
Time [ns]

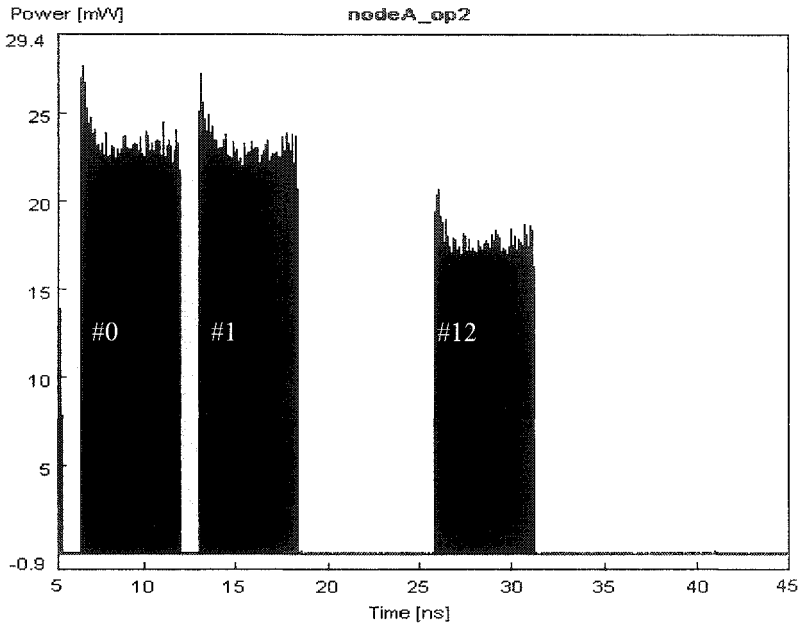
(c)


Power [mW]
CLK@NodeC
182
160
140
120
100
80
60
40
20
-5
5
10
15
20
25
30
35
40
45
Time [ns]

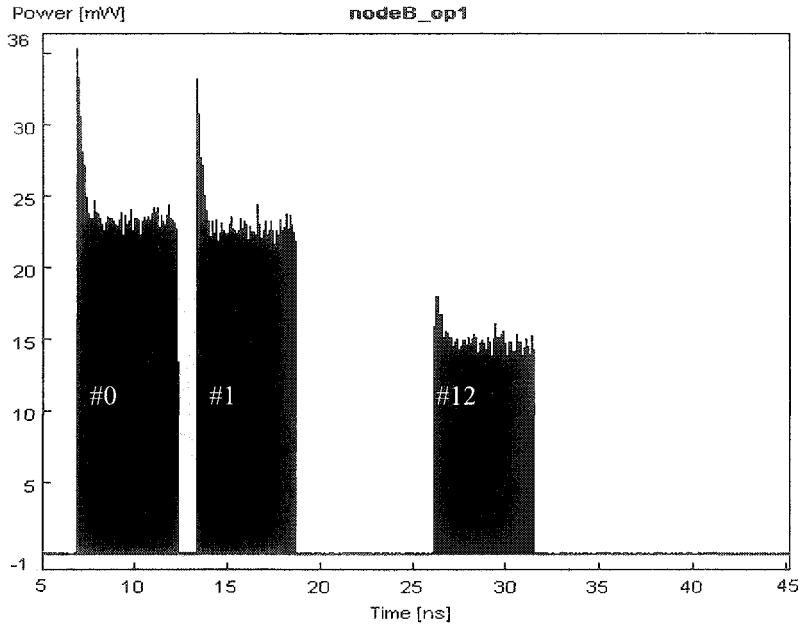
(d)


Power [mW]
CLK@NodeD
177
160
140
120
100
80
60
40
20
-5
2 ps
5
10
15
20
25
30
35
40
45
Time [ns]

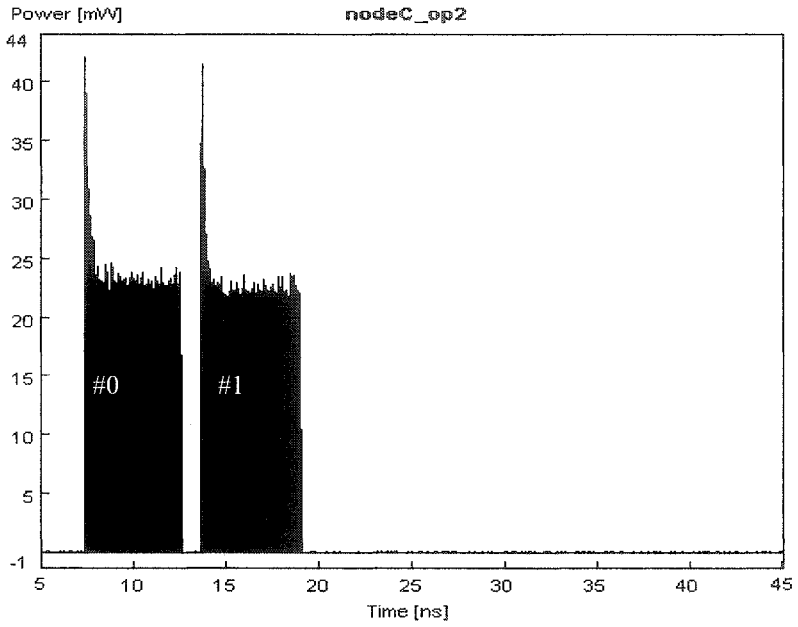
(e)


Power [mW]
nodeA_op2
29.4
25
20
15
10
5
-0.9
#0
#1
#12
5
10
15
20
25
30
35
40
45
Time [ns]

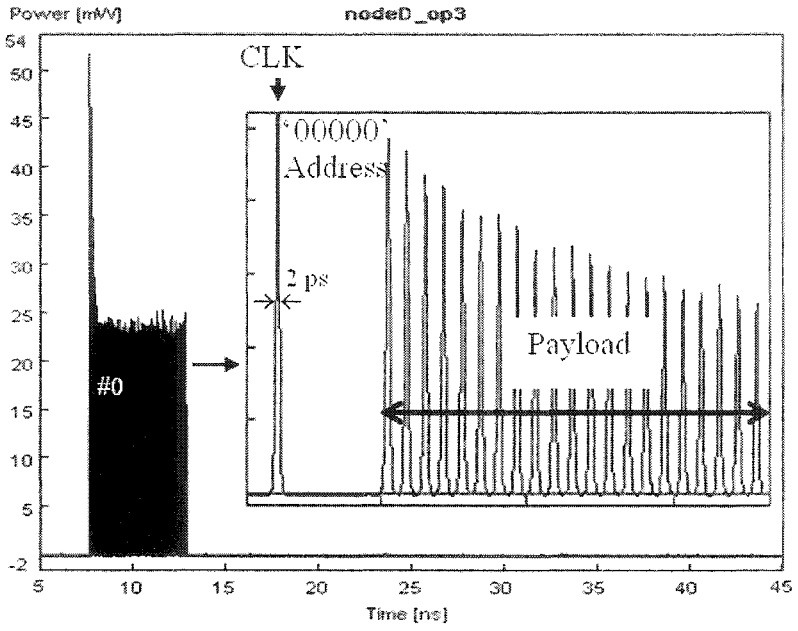
(f)


Power [mW]
nodeB_op1
36
30
25
20
15
10
5
-1
#0
#1
#12
5
10
15
20
25
30
35
40
45
Time [ns]

(g)



(h)



(i)

Figure 5.6 Time waveforms; (a) input packet at node A, (b)-(e) extracted clock at nodes A, B, C, and D, and (f)-(i) switched packets at nodes A – output2, B – output1, C – output2, and D – output3 (also see the enlarged waveforms)

Figure 5.7 depicts the theoretical and simulation for the OSNR against the number of hops. The theoretical analysis of SOA ASE noise and OSNR at the target node are given in equations (4.9) and (4.13), respectively. The disparities between the predicted and simulated results is mainly due to the intensity overshoot and power fluctuation of simulated packets in the simulation model, see Figure 5.6. It is shown that a ~2 dB drop on the OSNR, after each hop is due to the accumulated ASE noise.

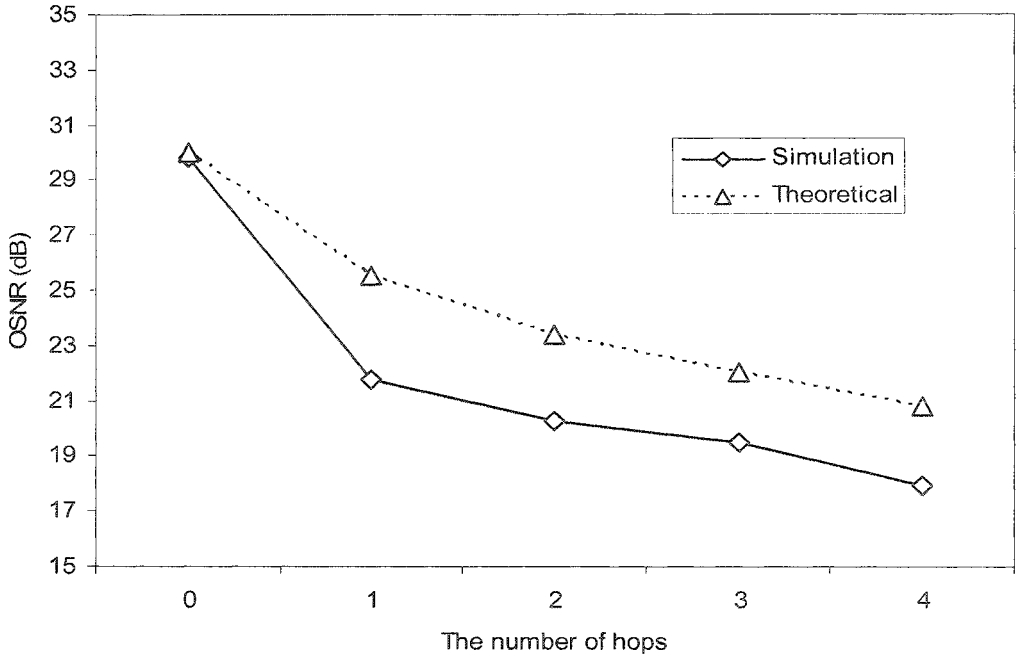


Figure 5.7 Predicted and simulated OSNR performance against the number of hops

5.6 Summary

In this chapter, the multiple PPRTs and the multiple PPRT generator have been proposed in Sections 5.2 and 5.3, respectively. The router architecture was presented in Section 5.4. The simulation time waveforms and the OSNR performance in multi-hops were also discussed in Section 5.5. In multiple PPRTs, the number and the length of entries are shorter than the conventional RTs and PPM based RTs,

respectively. As a result, the proposed router offers a faster processing time of 187.5 ps (i.e. ~ 250 times faster than router using CRT). The correlation-gain is high especially for packets with a long header address sequence. It was shown that predicted and simulated OSNR decreases by ~ 2dB after each hop, thus limiting the size network in which the packets could propagate to reach its destination. In the next chapter, a hybrid header address format is further proposed to reduce the complexity of router with multiple PPRTs.

CHAPTER 6 ALL-OPTICAL PACKET-SWITCHED ROUTER WITH A HYBRID HEADER ADDRESS FORMAT

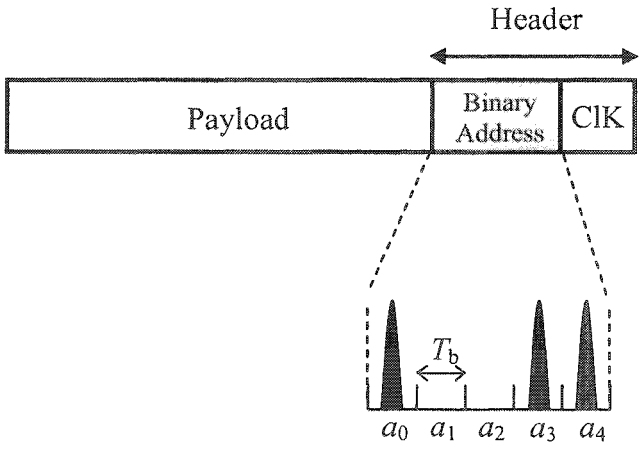
6.1 Introduction

In CHAPTER 5, it was shown that packet header address correlation time can be significantly reduced by employing the multiple pulse position routing tables (multiple PPRTs), where only a subset of the header address is converted into a pulse-position-modulation (PPM) format. In the previous routing scheme, a serial-to-parallel converter (SPC), an array of 1×2 optical switches, and a number of fibre delay lines (FDLs) are required to convert the binary format address to a PPM format in every switching node. However, for packets with a long header address, a large number of optical switches and delay lines are required, thus resulting in deterioration of the extinction ratio in the PPM-converted address [226].

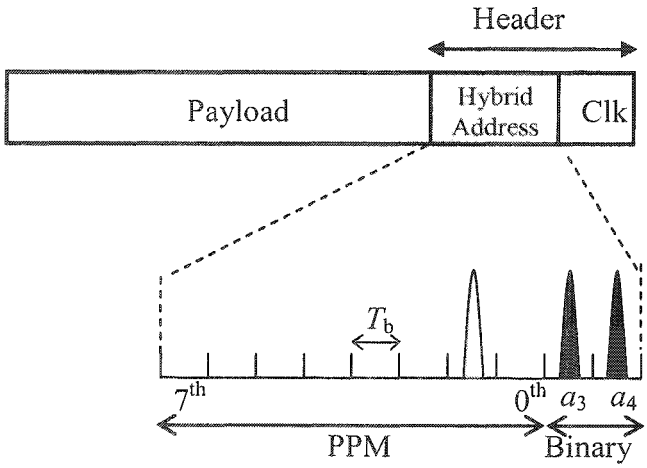
In this chapter, a hybrid header address routing scheme with no PPM address conversion module is proposed. This new routing scheme offers a number of advantages including (i) significantly reduced routing table entries, (ii) considerably reduced correlation processing time by employing multiple PPRTs, (iii) using merely a single bitwise AND gate instead of a large number of gates with a low response-time, and (iv) unicast, multi-cast and broadcast transmission modes embedded in the optical layer. The proposed scheme offers reduced complexity compared with a previous routing scheme due to exclusion of the PPM address conversion module [239].

6.2 Hybrid Header Address

A typical packet is composed of a header (clock and address) and a payload. The clock signal, normally the first bit within the packet header, is used for synchronisation within the router. In contrast to the conventional binary header address format (see Figure 6.1(a)), here a hybrid binary and PPM formats (shown in Figure 6.1(b)) is adopted, which is composed of 3-element and is defined by a set $S = \{S_C, S_A, S_P\}$.



(a)



(b)

Figure 6.1 (a) An optical packet with *N*-bit conventional binary address pattern (*N* = 5), (b) an optical packet with a hybrid header address format equivalent to *N*-bit conventional address pattern (*N* = 5), T_b is the bit duration

Where the elements representing the clock, address, and payload, respectively is given as:

$$S_C = 1,\ S_A = \{S_{A1}, S_{A2}\}, \tag{6.1}$$

S_{A1} and S_{A2} represent the most significant bits and a PPM format given as:

$$S_{A1} = \{a_{N-1}, a_{N-2}, \ldots, a_{N-X}\},\ \forall S_{A1} \in \{0,1\} \tag{6.2}$$

$$S_{A2} = \{b_0, b_1, \ldots b_d \ldots, b_{(2^{N-X}-1)}\}, \tag{6.3}$$

$\exists b_d = 1$ representing a PPM pulse and the rest of elements are equal to "0", where the decimal value of the binary address bits is given as:

$$d = \sum_{i=0}^{N-X-1} a_i \times 2^i, \tag{6.4}$$

N and X represent the conventional header length and its two MSBs, respectively.

$$S_P = \{p_0, p_1, p_2, \ldots, p_{l-1}\},\ \forall S_P \in \{0,1\}, \tag{6.5}$$

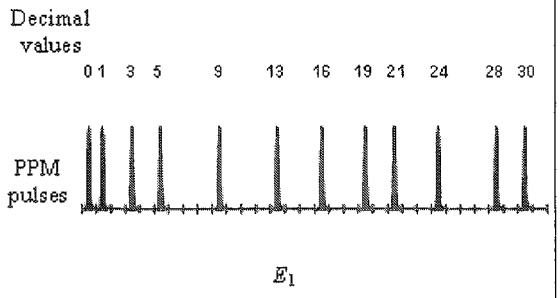
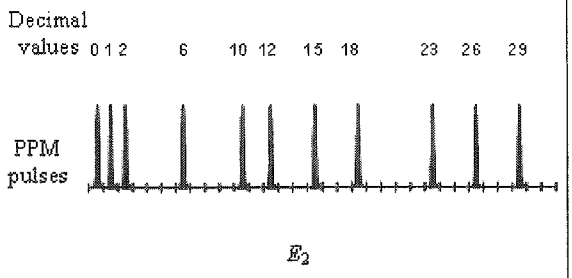
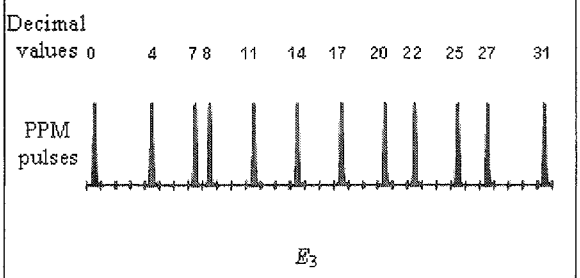
where l is the payload bit resolution.

For example, an N-bit binary address $\{a_4\ a_3\ a_2\ a_1\ a_0\}$ of $\{11001\}$ in the hybrid format is "1101000000", where the first two bits correspond to X and the remaining bits represent a PPM frame of length 2^{N-X} with a pulse located in position 2 corresponding to the decimal value of $\{a_2\ a_1\ a_0\}$, see Figure 6.1.

For a packet with N-bit header address $\{a_{N-1}\ a_{N-2} \ldots\ a_2\ a_1\ a_0\}$, where a_{N-1} is the most significant bit (MSB), the conventional routing table (CRT) will have a maximum of 2^N entries. In the worst case scenario, i.e. checking all entries, the router will perform 2^N N-bitwise correlations. Table 6.1 illustrates a routing table for N = 5 and its equivalent PPM versions. For each output of the node, there exists a single PPRT entry with 2^N slots. In this example, the standard PPRT has three entries E_i (i = 1,2, 3)

of length 32 slots with duration T_s. Here T_s is set to be equal to the bit duration T_b of 6.25 ps. The locations of the short pulses in each entry correspond to the decimal values of conventional binary address patterns in i^{th} group.

Table 6.1 The conversion of conventional RT to single PPRT

Address patterns (N=5)	Output port	PPRT entries with 32 slots (N=5)
0 0 0 0 0 0 0 0 0 1 0 0 0 1 1 0 0 1 0 1 0 1 0 0 1 0 1 1 0 1 1 0 0 0 0 1 0 0 1 1 1 0 1 0 1 1 1 0 0 0 1 1 1 0 0 1 1 1 1 0	1	
0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 1 1 0 0 1 0 1 0 0 1 1 0 0 0 1 1 1 1 1 0 0 1 0 1 0 1 1 1 1 1 0 1 0 1 1 1 0 1	2	
0 0 0 0 0 0 0 1 0 0 0 0 1 1 1 0 1 0 0 0 0 1 0 1 1 0 1 1 1 0 1 0 0 0 1 1 0 1 0 0 1 0 1 1 0 1 1 0 0 1 1 1 0 1 1 1 1 1 1 1	3	

In multiple PPRTs, each entry length could be reduced from $32T_s$ to $2^{N-X}\times T_s$ by splitting each PPRT entry into sub-groups of E_{ij} (i = 1, 2, 3, and j = *A, B, C, D*), see Table 6.2. *A*, *B*, *C* and *D* represent address patterns with decimal metrics in ranges of (24-31), (16-23), (8-15) and (0-7), respectively. For X = 2 and N = 5 the PPRT entry length is reduced from $32T_s$ to $8T_s$.

Table 6.2 The conversion of conventional RT to multiple PPRTs

	Address patterns (N=5)	PPRT entry	4 Multiple PPRT entries with 8 slots (N=5, X=2)
E_{1D}	0 0 0 0 0	E_1	0 1 3 5 9 13 16 19 21 24 28 30
	0 0 0 0 1		
	0 0 0 1 1		
	0 0 1 0 1		
E_{1C}	0 1 0 0 1		
	0 1 1 0 1		
E_{1B}	1 0 0 0 0		
	1 0 0 1 1		
	1 0 1 0 1		
E_{1A}	1 1 0 0 0		
	1 1 1 0 0		
	1 1 1 1 0		
E_{2D}	0 0 0 0 0	E_2	0 1 2 6 10 12 15 18 23 26 29
	0 0 0 0 1		
	0 0 0 1 0		
	0 0 1 1 0		
E_{2C}	0 1 0 1 0		
	0 1 1 0 0		
	0 1 1 1 1		
E_{2B}	1 0 0 1 0		
	1 0 1 1 1		
E_{2A}	1 1 0 1 0		
	1 1 1 0 1		
E_{3D}	0 0 0 0 0	E_3	0 4 7 8 11 14 17 20 22 25 27 31
	0 0 1 0 0		
	0 0 1 1 1		
E_{3C}	0 1 0 0 0		
	0 1 0 1 1		
	0 1 1 1 0		
E_{3B}	1 0 0 0 1		
	1 0 1 0 0		
	1 0 1 1 0		
E_{3A}	1 1 0 0 1		
	1 1 0 1 1		
	1 1 1 1 1		

6.3 Node Architecture

The proposed router with a multiple PPRTs and M-output ports is composed of a number of main modules including a clock extraction module (CEM), a header address extraction module (HEM), a multiple PPRT generator, AND gates, $1\times M$ all-optical switch, an optical switch control module (OSC), and a number of 1×2 high extinction ratio optical switches (SW) [237], see Figure 6.2.

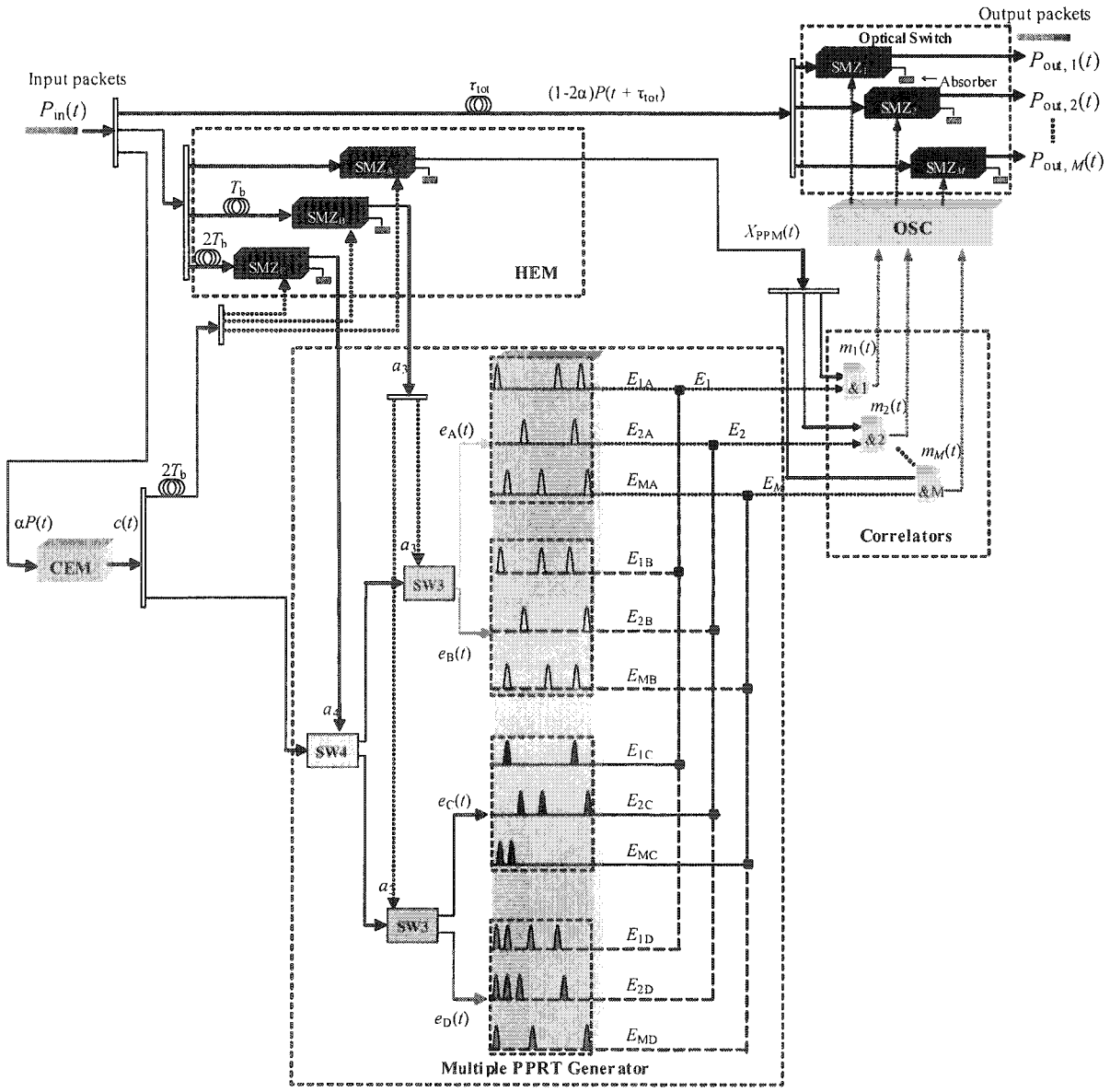


Figure 6.2 A schematic block diagram of node architecture for packets with hybrid header address (where N=5, X=2)

The received packet $P_{in}(t)$ after splitting is applied to the CEM, HEM and optical switch modules, respectively. The extracted clock pulse $c(t)$ having been delayed by $2T_b$ and 0 is applied to the HEM and SW4, respectively, whereas the outputs of HEM are applied to the SWs 3&4 and the AND gates. The two MSB bits (a_4 and a_3) are checked by SWs 4&3 to select the first two groups E_A and E_B, and E_C or E_D of multiple PPRTs, respectively for address correlation. PPRTs with the same i^{th} index are combined together and applied to the optical AND gates for address correlation. Note that, only one multiple PPRT is used for correlation with an incoming packet header address $X_{PPM}(t)$. The outputs of the multiple PPRTs, see Figure 6.2, are given as [239]:

$$E_k(t) = E_{kA}(t) + E_{kB}(t) + E_{kC}(t) + E_{kD}(t), \tag{6.6}$$

where each d_k element corresponds to the decimal values of the header address bits assigned to the node output k^{th} ($k = 1, 2, \ldots M$).

The SMZ based optical AND gates outputs are given by:

$$m_k(t) = X_{PPM}(t) \times E_k(t) = \begin{cases} 1 & if \quad d_k = \sum_{i=0}^{N-1} a_i \times 2^i \quad \forall k \\ 0 & if \quad d_k \neq \sum_{i=0}^{N-1} a_i \times 2^i \quad \forall k \end{cases}, \tag{6.7}$$

$$k = 1,2,\ldots,M \qquad d_k \in \{0 \sim (2^N - 1)\}.$$

$m_k(t)$ are applied to the OSC module to ensure that incoming packets $P_{in}(t)$ delayed by τ_{tot} (total required time for header address correlation) are switched to the correct output ports. The switched packet is given as:

$$P_{out,k}(t) = P_{in}(t) \times m_k(t) = \begin{cases} G_{OS} \times (1 - 2\alpha) \times P_{in}(t + \tau_{tot}) & if \quad m_k(t) = 1 \\ 0 & if \quad m_k(t) = 0 \end{cases}, \tag{6.8}$$

$$k = 1,2,\ldots,M$$

where G_{OS} is the optical switch gain.

If more than one pulse is located at the same position in more than one (or all) PPRT entries, then packet is broadcasted to multiple outputs (i.e. multicast) or all outputs (i.e. broadcast), respectively.

In a hybrid header address format, two MSBs (i.e. the binary address) are used for selecting the sub-group of multiple PPRTs, and the rest of address bits (i.e. the PPM address) are directly used to correlate with the multiple PPRT entries. The address correlation time of this scheme is shown in equation (5.10). Comparing with using the CRT, the correlation-time gain in this scheme is defined in equation (5.12).

6.4 Simulation Results

The router shown in Figure 6.2 is simulated using the Virtual Photonics simulation software (VPI^{TM}). By taking advantage of the hybrid address format, the new node architecture could be constructed with reduced complexity due to exclusion of the PPM address conversion module [239] within the router. Table 6.3 illustrates all the main simulation parameters adopted [210, 216].

Table 6.3 Simulation parameters

Parameters	Values
Data packet bit rate $R_b = 1/T_b$	160 Gb/s
Packet payload length	53 bytes (424 bits)
Wavelength of data packets	1554 nm (193.1 THz)
Data pulse width (FWHM)	2 ps
PPM slot duration T_s (= T_b)	6.25 ps
Average transmitted packet pulse peak power P_{in}	5 mW
Average pulse peak power of $C_k(t)$	270 mW
Optical bandwidth	2.4 nm (300 GHz)
Splitting factor α	0.2
Inject current to SOA	150 mA
SOA length	500 μm
SOA width	3×10^{-6} m
SOA height	80×10^{-9} m
SOA n_{sp}	2
Confinement factor	0.15
Enhancement factor	5
Differential gain	2.78×10^{-20} m^2
Internal loss	40×10^{2} m^{-1}
Recombination constant A	1.43×10^{8} s^{-1}
Recombination constant B	1.0×10^{-16} m^3s^{-1}
Recombination constant C	3.0×10^{-41} m^6s^{-1}
Carrier density transparency	1.4×10^{24} m^{-3}
Initial carrier density	3×10^{24} m^{-3}

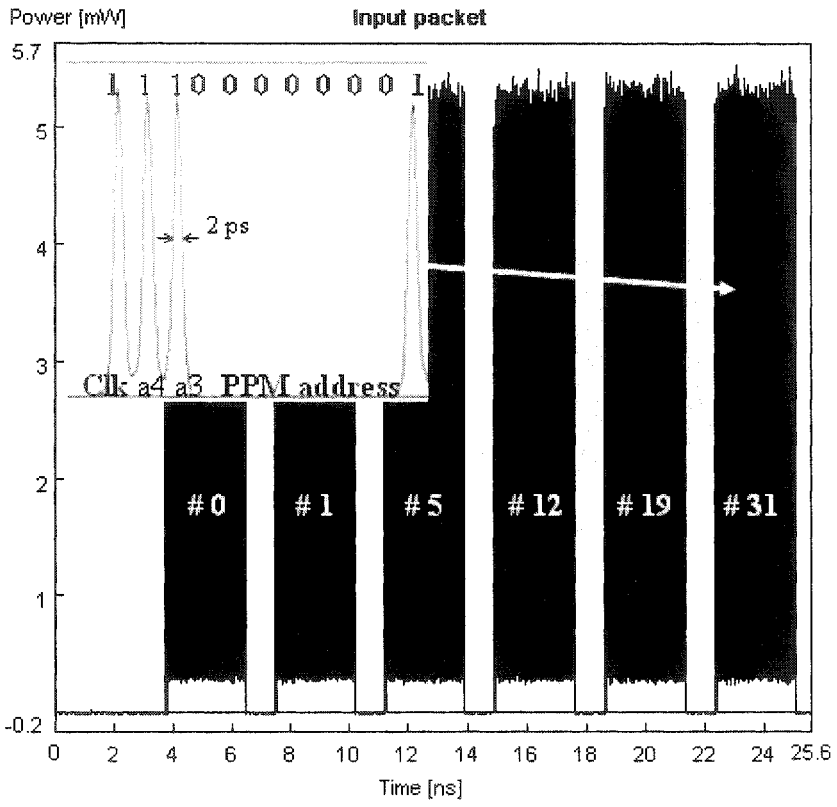
Six optical packets with addresses of #0, #1, #5, #12, #19 and #31 (decimal values) are transmitted sequentially at 160 Gb/s with 1 ns inter-packet guard time. Each packet contains a 1-bit clock, a 10-bit hybrid address and a 53-byte payload (ATM cell size) [83, 235].

The total processing time of the all-optical router with hybrid header address format, τ_{tot} (i.e. the time delay between the input packets and switched packets) in this simulation ($N = 5$, $X = 2$, $T_s = T_b = 6.25$ ps) is equal to 75 ps, which is calculated as follows:

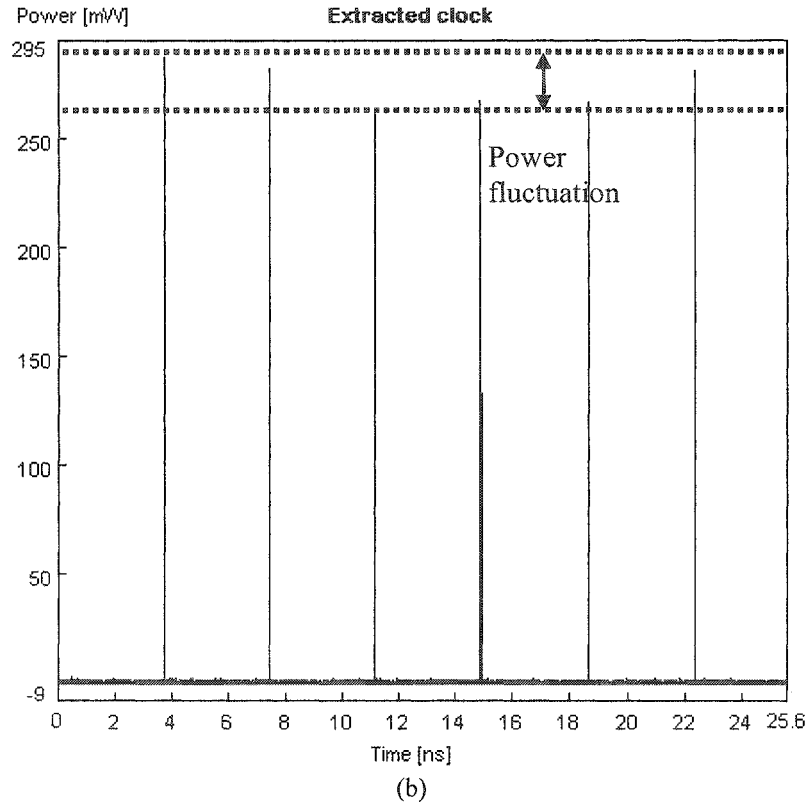
$$\tau_{tot} = 2^{N-2} \times T_s + X \times T_b + 2T_b, \tag{6.9}$$

where $2^{N-2} \times T_s$ is the duration of a 2^{N-2}-slot PPM-frame, $X \times T_b$ is the required processing time for the HEM module, and $2T_b$ are the required processing time for the CEM module and the AND gate operation.

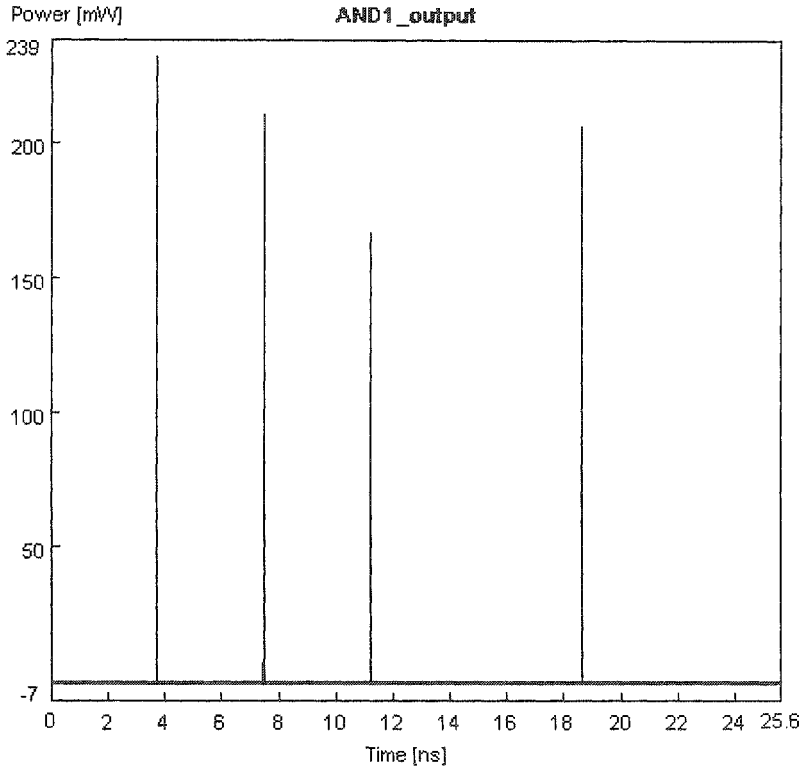
Figure 6.3(a) depicts the time waveforms of the six input packets with the inset illustrating the zoomed-in packet hybrid header with an address decimal metric of #31. The extracted clock pulses are presented in Figure 6.3(b). Figure 6.3(c), (d), and (e) illustrate the time waveforms observed at the outputs of AND gates 1, 2, and 3, respectively. Time waveforms of signals at the output ports 1, 2, and 3 of the router are depicted in Figure 6.3(f), (g), and (h), respectively, confirming that the incoming packets with header addresses of #0, #1, #5, #12, #19 and #31 are switched to outputs 1 & 2, 1, 2, 1, and 3, respectively, based on the routing information given in Table 6.1 and Table 6.2. In addition, unicast, multicast and broadcast transmitting capabilities of the router are also demonstrated as packets with addresses of #5, #12, #19, and #31 are switched to one output port of the router, whereas the packets with #1 and #0 addresses are switched to two and all output ports of the router, respectively.


Power [mW]
Input packet
5.7
5
4
3
2
1
-0.2
1 1 1 0 0 0 0 0 0 1
2 ps
Clk a4 a3 PPM address
0
1
5
12
19
31
0 2 4 6 8 10 12 14 16 18 20 22 24 25.6
Time [ns]

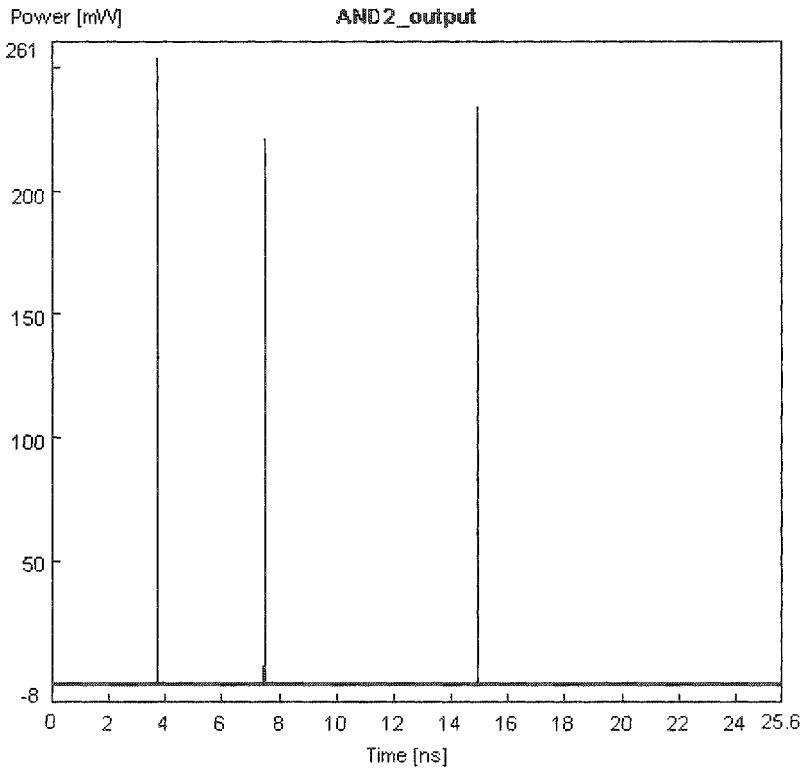
(a)


Power [mW]
Extracted clock
295
250
200
150
100
50
-9
Power
fluctuation
0 2 4 6 8 10 12 14 16 18 20 22 24 25.6
Time [ns]

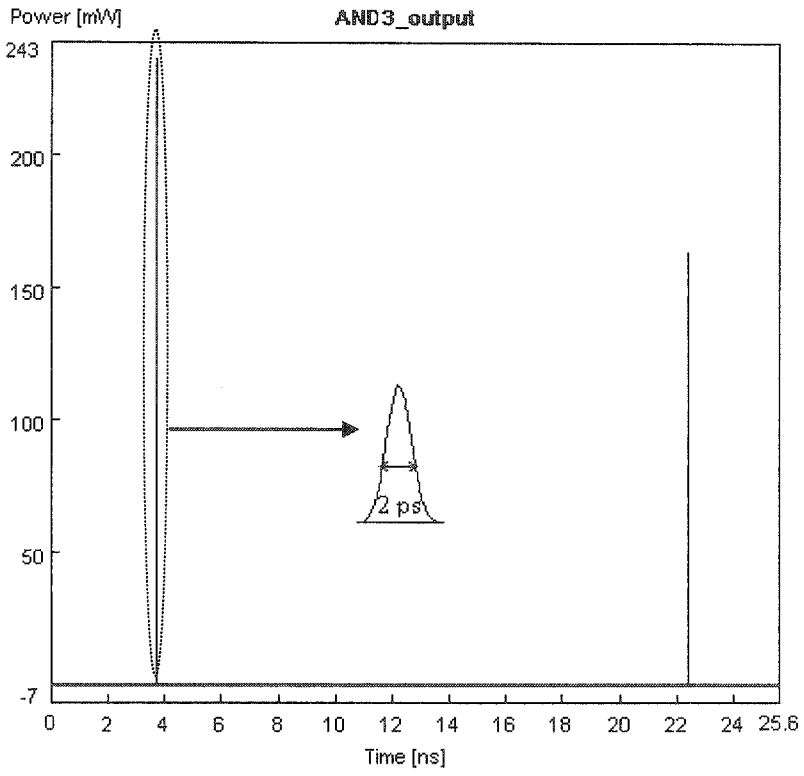
(b)


Power [mW]
AND1_output
239
200
150
100
50
-7
0
2
4
6
8
10
12
14
16
18
20
22
24
25.6
Time [ns]

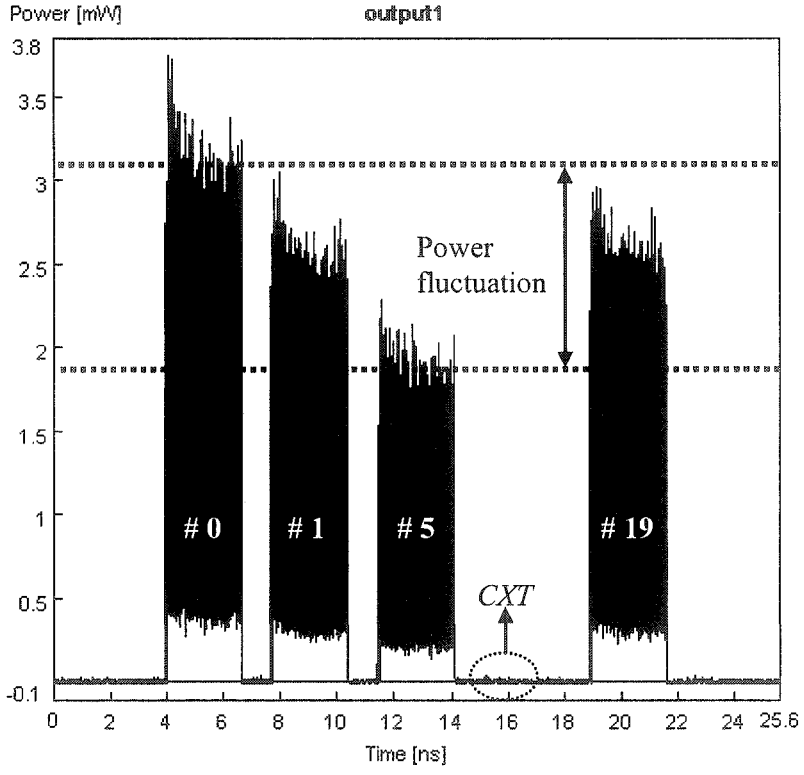
(c)


Power [mW]
AND2_output
261
200
150
100
50
-8
0
2
4
6
8
10
12
14
16
18
20
22
24
25.6
Time [ns]

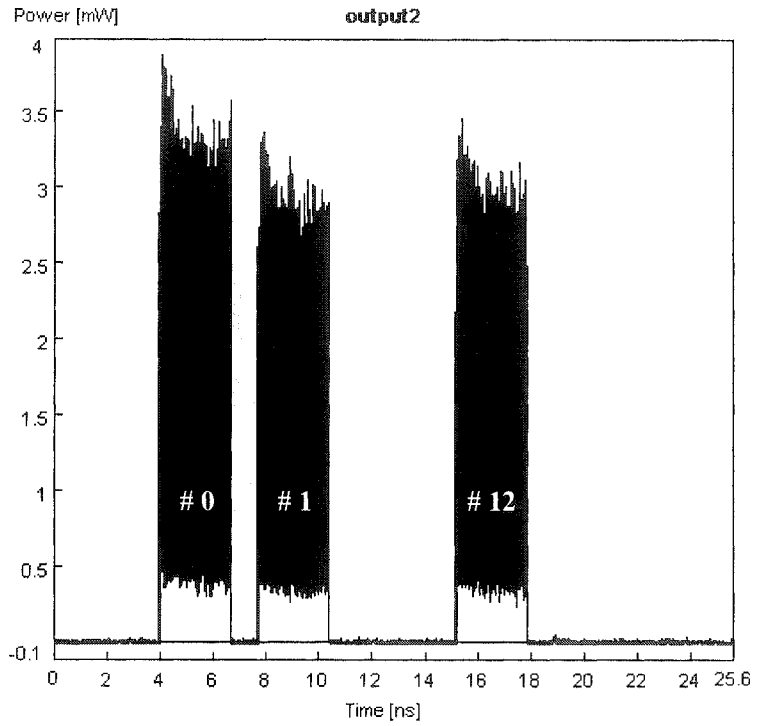
(d)


Power [mW]
AND3_output
243
200
150
100
50
-7
2 ps
0 2 4 6 8 10 12 14 16 18 20 22 24 25.6
Time [ns]

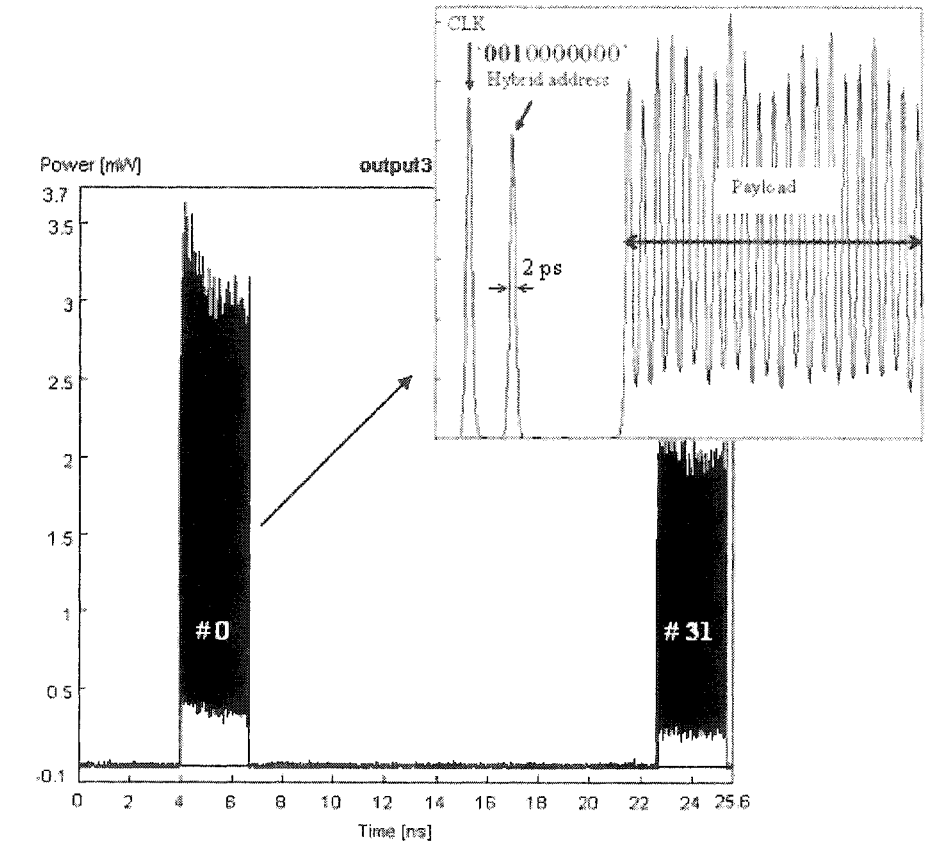
(e)


Power [mW]
output1
3.8
3.5
3
2.5
2
1.5
1
0.5
-0.1
Power
fluctuation
0
1
5
19
CXT
0 2 4 6 8 10 12 14 16 18 20 22 24 25.6
Time [ns]

(f)



(g)



(h)

Figure 6.3 Time waveforms of (a) input packets, (b) extracted clock signals, (c) matched signals at AND gate 1, (d) matched signals at AND gate 2, (e) matched signals at AND gate 3, (f) switched packets at router's output 1, (g) switched packets at router's output 2, and (h) switched packets at router's output 3 (also see the enlarged waveforms)

Figure 6.4 investigates the output intra-channel *CXT* and power fluctuation against the different packet guard time observed at the output 1. Crosstalk is an important issue which will lead to transmission and node functionality impairment [67]. More investigations on *CXT* will be outlined in Section 7.3. Additionally, packets with a large power fluctuation may deteriorate the system BER performance [149, 236].

The intra-channel *CXT* is defined as:

$$CXT = 10\log_{10}\left(P_{nt} / P_t\right), \tag{6.10}$$

where P_{nt} is the peak output signal power of the undesired packet and P_t is the average output signal power of the lowest target desired packet.

The undesired *CXT* is due to the in-completed cut-off edge of the switching window profile induced by the slow gain recovery of the SOA [240]. *CXT* is high for lower values of the packet guard time, improving significantly by increasing the guard time, reaching ~ -18 dB beyond the packet guard time of 1.2 ns. This improvement is due to the switching window being completely closed. However as the guard time increases beyond 1.2 ns, no further improvement is achieved. This is because the *CXT* is solely due to the extinction ratio of matched signal $m(t)$, see Figure 6.2.

The power fluctuation of the extracted clock signals and the output packets are defined by the differences between the highest and lowest intensity in decibel, see Figure 6.3(b) and (f), respectively. Figure 6.4 displays the minimum power fluctuations of the clock signal and the output packets that are 0.3 dB and 2 dB, respectively. The observed power fluctuation of the switched packets is mainly due to the unequal output power of the AND gates, see Figure 6.3(c)-(e). This is because

power fluctuation of the extracted clock signals (see Figure 6.3(b)) increases after passing through two amplification stages (i.e. SW4 and SW3), thus resulting in an unequal input power at the input of the AND gates. Thus, the need for a wider packet guard time of greater than 1 ns).

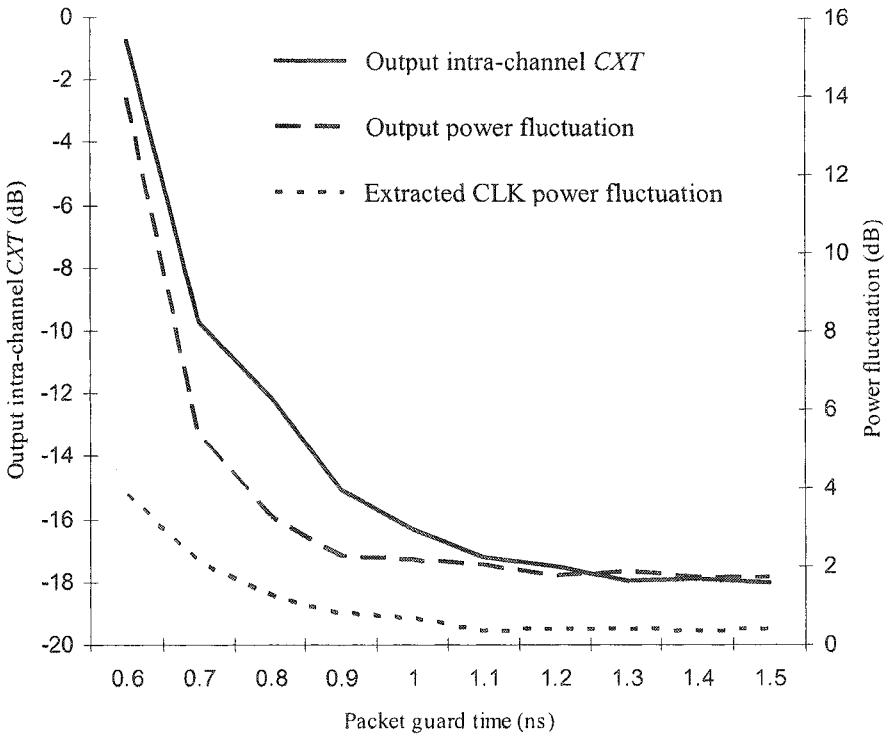


Figure 6.4 Packet guard time against the output intra-channel *CXT* (left x-axis), output packet power fluctuation (right x-axis) and the extracted clock power fluctuation (right x-axis)

6.5 Summary

The chapter has presented an all-optical packet-switched routing scheme with a hybrid header address format. $1\times M$ router architecture employing the multiple PPRTs and hybrid header address was introduced offering reduced system design complexity and avoided the speed limitation imposed by the non-linear element based optical AND gates. Packet header processing and packet routing were investigated by means

of simulation. Results obtained showed that this router is capable of operating at a data rate of 160 Gb/s with the output intra-channel crosstalk (*CXT*) of up to -18 dB and the margin of output packet power fluctuation is 2 dB largely dependent on the inter packet guard time.

CHAPTER 7 MULTIPLE WAVELENGTH ROUTER FOR WDM SYSTEM

7.1 Introduction

PPM header processing (PPM-HP) scheme has been used to convert both the packet header address and routing table entries from a return-to-zero (RZ) format to a pulse-position-modulation (PPM) format for single wavelength routing schemes. In this chapter, a WDM based all-optical router employing the PPM-HP is proposed. The advantages of this scheme are (i) significantly reduced routing table entries, where each entry contains more than one PPM based header address, (ii) considerably reduced correlation processing time by using merely a single bitwise AND gate instead of a large number of gates with a low response-time, (iii) offering multiple transmitting modes (unicast, multi-cast and broadcast) embedded in the optical layer, (iv) reduced complexity due to exclusion of the PPM address conversion module [241], and (v) uses fewer components compared to the existing all-optical routing employing wavelength conversions [133, 137, 242] and all-optical flip-flops [229, 231].

This chapter is organised as follows: Section 7.2 introduces the architecture of the PPM-HPs based WDM router. The simulation results, output packet intensity fluctuation and inter-channel crosstalk performance, and the output transfer function of the PPM-HP module versus different values of input power are also investigated and discussed in Section 7.3. Finally, Section 7.4 will give a summary of this chapter.

7.2 Router Architecture

Figure 7.1 shows a PPM based packet address format. For example, a traditional 4-bit binary address of "0011" with a decimal value of 3 is represented in a PPM format as "0001000000000000", where a single pulse is located at the 3rd position of the frame. In CHAPTER 4, it has been shown that PPM based routing scheme improves packet header address correlation time compared to the conventional routing tables (CRT).

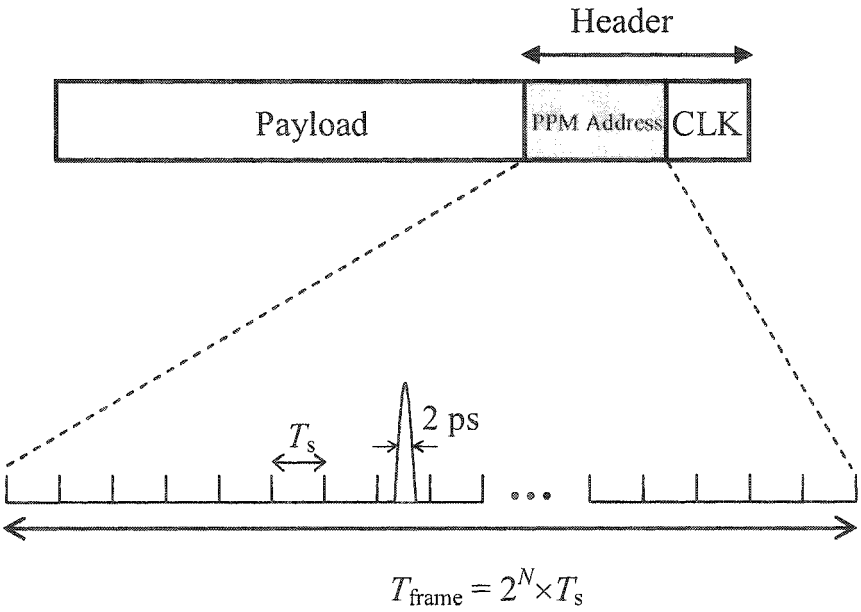


Figure 7.1 An optical packet with the PPM header address

Table 7.1 illustrates a routing table for a traditional 4-bit binary address, where 16 possible addresses are grouped into M groups based on the intended target output ports. Here $M = 3$ representing the number of output ports. The 3rd column shows the PPRT entries E_m (m = 1,2,...M) of length $2^N \times T_s$ for each group. Note that the number of entries is reduced from 16 to 3 compared to the CRT, thus resulting in a reduced header address correlation time, see Table 7.1. A packet with header address matching one or more patterns in a group can be switched to more than one output ports. At a

very high bit rate R_b (in this case 160 Gb/s) generating a PPM pulse with an ultra short T_s is a challenging task, therefore here we have kept T_s to be equal to T_b = 6.25 ps.

Table 7.1 The conventional and PPM based routing tables

Address patterns (N=4)	Output Port (M=3)	PPRT entries with 16 slots
0 0 0 0 0 0 0 1 0 1 0 0 1 0 0 1 1 0 1 1 1 1 1 1	1	E_1 Decimal values 0 1 4 9 11 15 PPM pulses
0 0 0 0 0 0 1 0 0 1 1 0 0 1 1 1 1 1 0 1 1 1 1 0	2	E_2 Decimal values 0 2 6 7 13 14 PPM pulses
0 0 0 0 0 0 0 1 0 0 1 1 0 1 0 1 1 0 0 0 1 0 1 0 1 1 0 0	3	E_3 Decimal values 0 1 3 5 8 10 12 PPM pulses

Figure 7.2 depicts a block diagram of a 1×M WDM router architecture, which is composed of a 1×L demultiplexer, L PPM-HPs, and M L×1 multiplexers, where L is the number of wavelengths. At the input, WDM packets at multiple-wavelengths (λ_1, λ_2 … and λ_L) are fed into a bank of PPM-HP modules via a WDM demultiplexer. Packets with the PPM format header address at specific wavelengths are processed at

the PPM-HP modules before being broadcasted to all $L\times1$ multiplexers. In contrast to existing schemes this architecture uses fewer number of laser sources because there is no need for wavelength conversion modules.

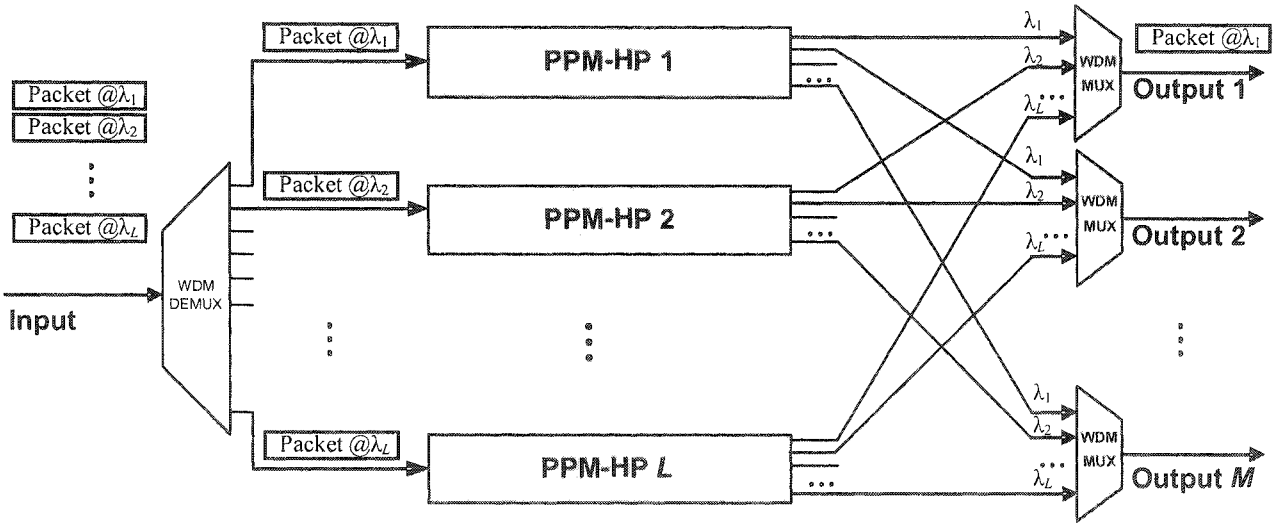


Figure 7.2 The WDM router architecture for L = 2 and M =3

Figure 7.3 illustrates a schematic block diagram of $1\times M$ PPM-HP module. It is composed of an asynchronous clock extraction module (CEM), a PPM header address extraction module (PPM-HEM), a PPM routing table (PPRT), AND gates, a number of fibre delay lines (FDLs), a number of symmetric Mach-Zehnder based all-optical switches (OS), and an OS control module (OSC). The incoming optical packet $P_{in}(t)_{\lambda i}$ is applied via 1×3 splitter to the CEM, PPM-HEM and OS with the delays of 0, τ_{CEM} (required time for the clock extraction) and τ_{tot} (total required time for PPM address correlation), respectively. τ_{CEM} and τ_{tot} are the delayed required for clock extraction and PPM address correlation, respectively. The CEM, PPM-HEM and PPRT modules configurations are the same as those adopted in CHAPTER 4. The extracted clock

signal $c(t)$ and its delayed version $\alpha c(t - \tau_{PPRT})$ are applied to the PPM-HEM and PPRT, respectively. α is the 1×3 splitting coefficient. A PPRT is constructed by applying the delayed clock signal through a number of FDLs as in [226]. The packet header address, in PPM format, at the output of the PPM-HEM is correlated with the PPRT entries using a bank of all-optical AND gates. The correlated output pulses are applied to the OS via OSC to ensure the input packet is delivered to the intended output port. If more than one PPM pulse is located at the same position in more than one (or all) PPRT entries, then the input packet is broadcasted to multiple outputs (i.e. multicast) or all outputs (i.e. broadcast), respectively.

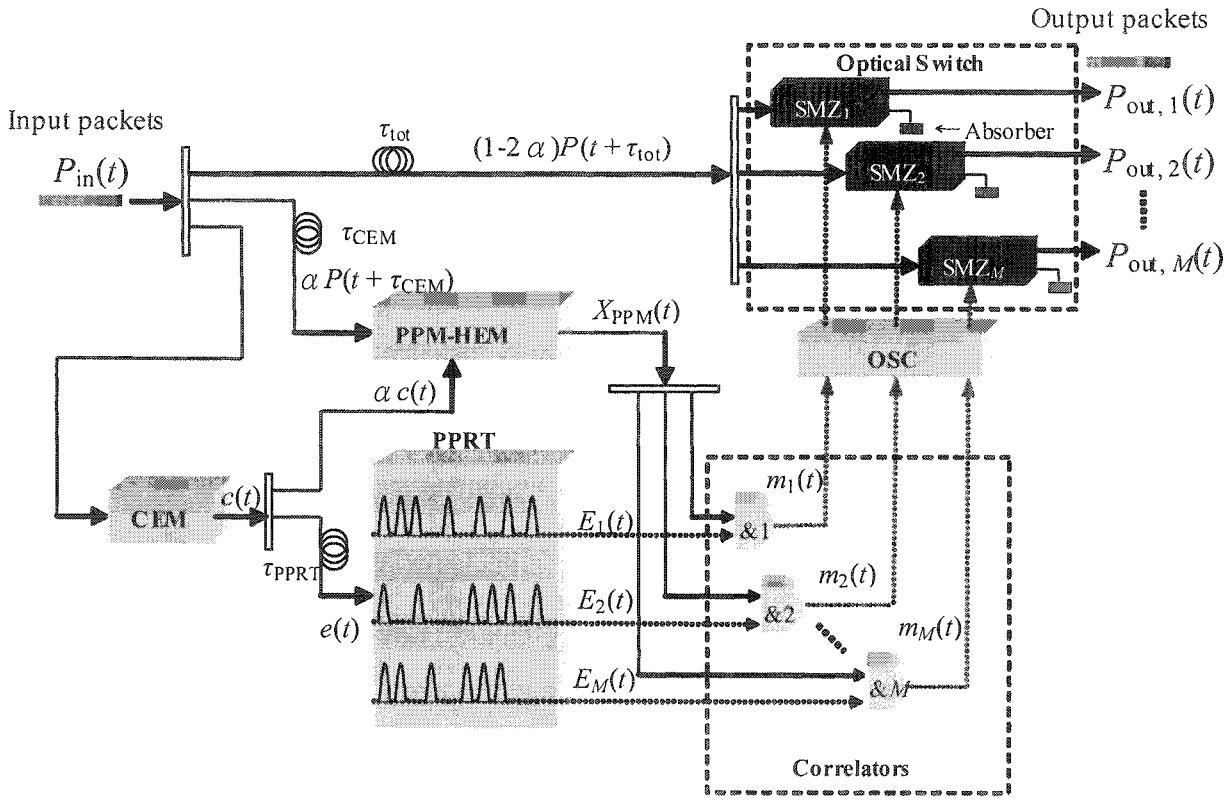


Figure 7.3 The schematic diagram of PPM-HP

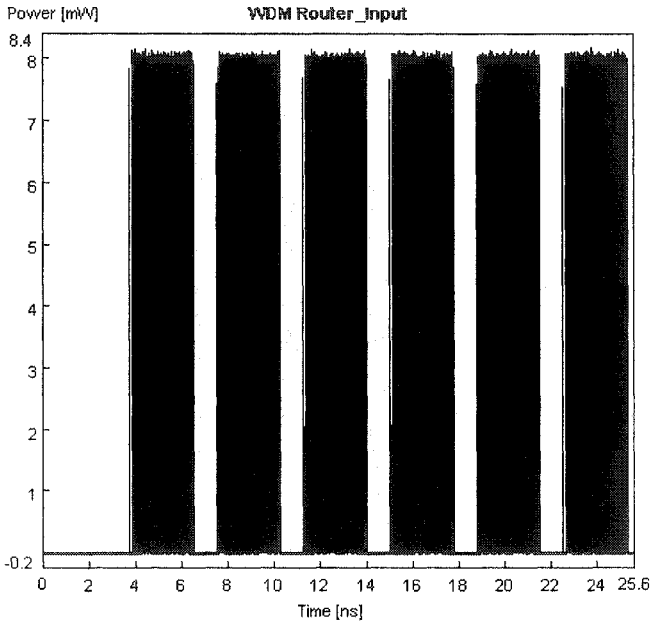
7.3 Simulation Results

The proposed WDM router is simulated by using the Virtual Photonics simulation package (VPI^{TM}). Table 7.2 shows the all main simulation parameters [210, 216]. Twelve WDM optical packets with addresses of #0, #1, #3, #6, #9, #14 (in decimal), and #0, #4, #7, #10, #13, #15 are transmitted at wavelengths of λ_1 and λ_2, respectively. Packets are sequentially transmitted at 160 Gb/s with 1 ns inter-packet guard interval. Each packet is composed of a 1-bit clock, a 16-bit PPM address, and a 53-byte payload (ATM cell size) [83, 235].

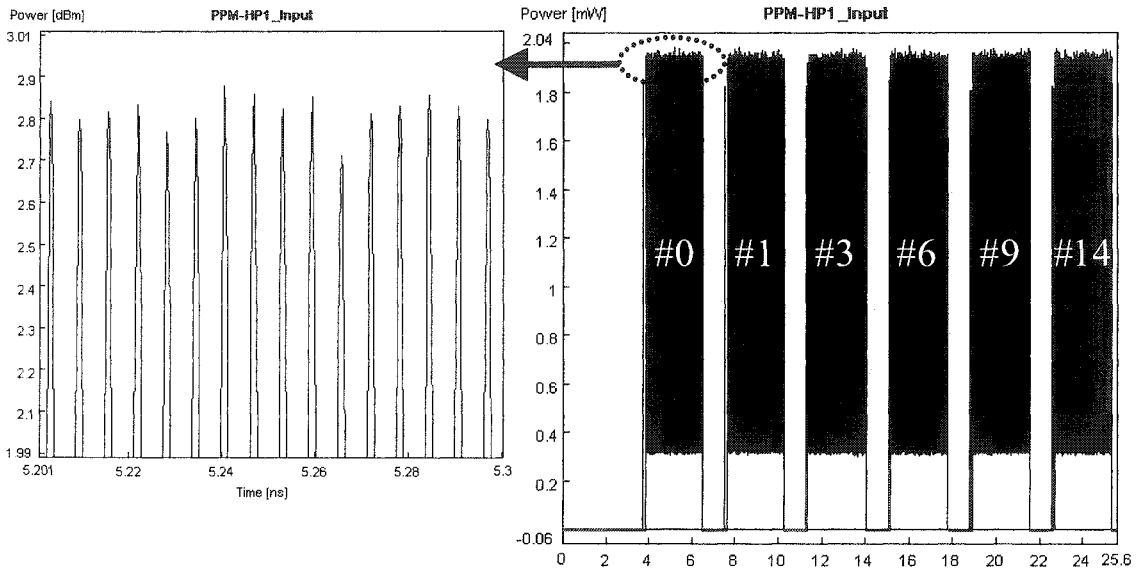
Table 7.2 Simulation parameters

Parameters	Values
Data packet bit rate $R_b = 1/T_b$	160 Gb/s
Packet payload length	53 bytes (424 bits)
Wavelength 1 (f_1)	1554 nm (193.1 THz)
Wavelength 2 (f_2)	1546 nm (194.1 THz)
Data pulse widths (FWHM)	2 ps
PPM slot duration T_s (= T_b)	6.25 ps
Average transmitted packet pulse peak power P_{in}	2 mW
Optical bandwidth of the WDM (de)multiplexers (Bandpass filter with order 1 of Gaussian transfer function)	4 nm (500 GHz)
Splitting factor α	0.25
Number of control pulses	60
Average control pulse power	10 mW
SOA injection current	150 mA
SOA active region length	500×10^{-6} m
SOA active region width	3×10^{-6} m
SOA active region height	80×10^{-9} m
SOA n_{sp}	2
Confinement factor	0.15
Enhancement factor	5
Differential gain	2.78×10^{-20} m^2
Internal loss	40×10^{2} m^{-1}
Recombine constant A	1.43×10^{8} s^{-1}
Recombine constant B	1×10^{-16} m^{3}s^{-1}
Recombine constant C	3×10^{-41} m^{6}s^{-1}
Carrier density at transparency	1.4×10^{24} m^{-3}
Initial carrier density	3×10^{24} m^{-3}

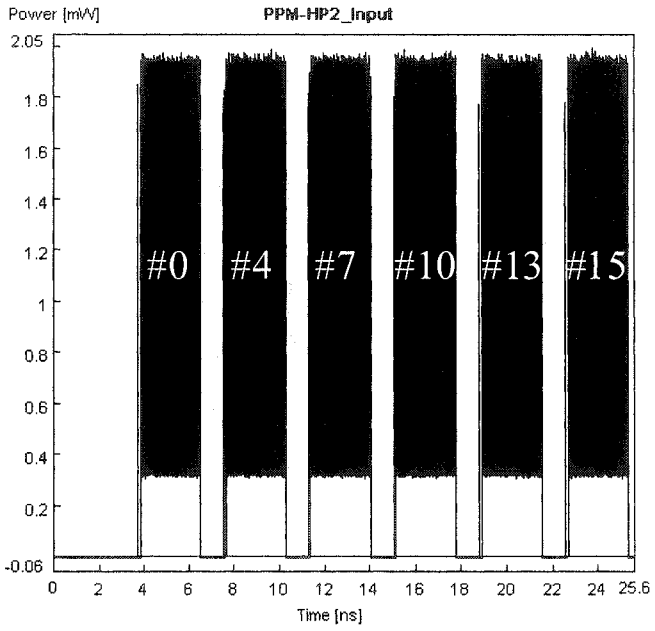
The time waveforms of 6-input WDM packets and their switched versions at the outputs are depicted in Figure 7.4. Figure 7.4(a)-(c) shows the multiplexed and demultiplexed packets waveforms at the input of the WDM router and PPM-HP1 & 2, respectively. The reason for pulses lower intensity being above the minimum level is due to a very narrow FWHM of 2 ps overlapping within a bit period of 6.25 ps. The overlap can be avoided by reducing the FWHM or the bit rate. Packets are switched to their corresponding output ports according to the PPRT in Table 7.1. Packets at specific wavelengths observed at the outputs of the PPM-HP1&2 and the WDM ports are displayed in Figure 7.4(d)-(i). The intensity overshot observed at the start of switched packets is due to the gain saturation of the SOA within the OS when injected with a packet stream, where the proceeding bits will experience a lower amplification gain. This can be minimized by decreasing the power of the input packet. There is a small intensity fluctuation of less than 0.3 dB with the packet stream as shown in the insets of Figure 7.4(b) and (e). The reason for this has been discussed in Section 4.5. Note that in Figure 7.4(d)-(i), packets with addresses #0 are switched to multiple outputs (i.e. multicast).


Power [mW]
WDM Router_Input
8.4
8
7
6
5
4
3
2
1
-0.2
0
2
4
6
8
10
12
14
16
18
20
22
24
25.6
Time [ns]

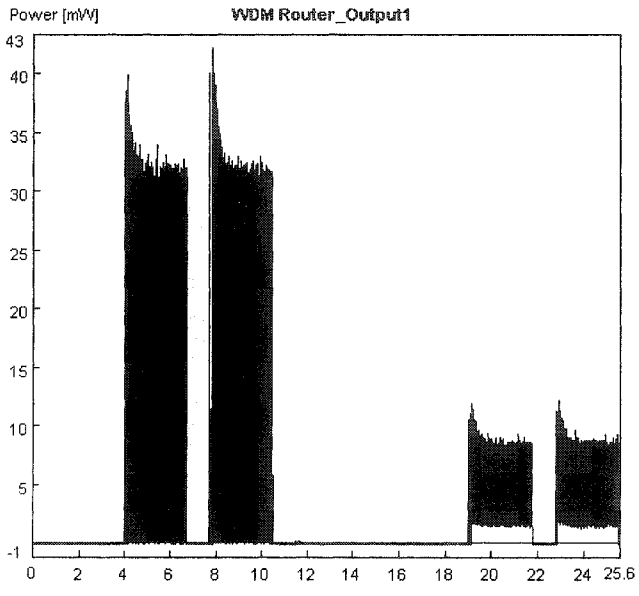
(a)


Power [dBm]
PPM-HP1_Input
3.01
2.9
2.8
2.7
2.6
2.5
2.4
2.3
2.2
2.1
1.99
5.201
5.22
5.24
5.26
5.28
5.3
Time [ns]
Power [mW]
PPM-HP1_Input
2.04
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
-0.06
#0
#1
#3
#6
#9
#14
0
2
4
6
8
10
12
14
16
18
20
22
24
25.6

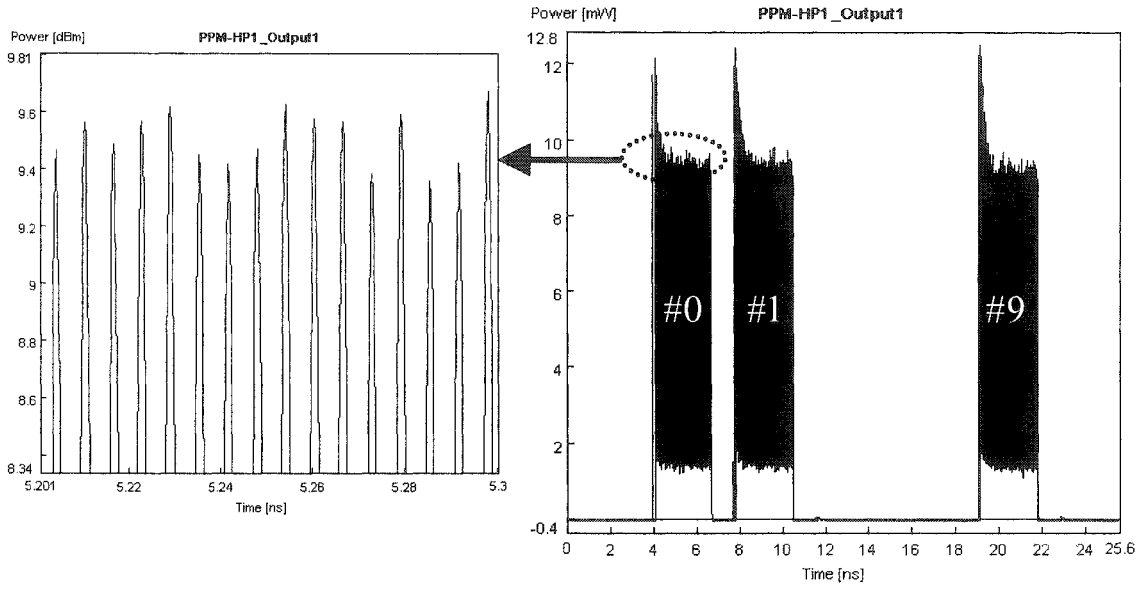
(b)


Power [mW]
PPM-HP2_Input
2.05
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
-0.06
#0
#4
#7
#10
#13
#15
0
2
4
6
8
10
12
14
16
18
20
22
24
25.6
Time [ns]

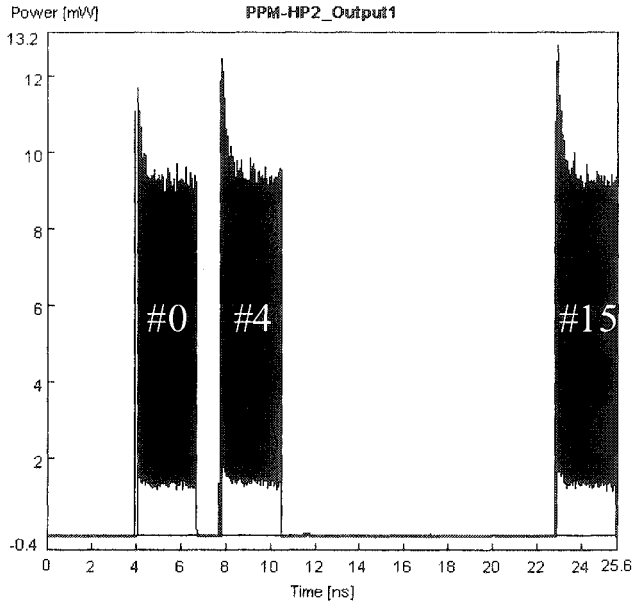
(c)


Power [mW]
WDM Router_Output1
43
40
35
30
25
20
15
10
5
-1
0
2
4
6
8
10
12
14
16
18
20
22
24
25.6

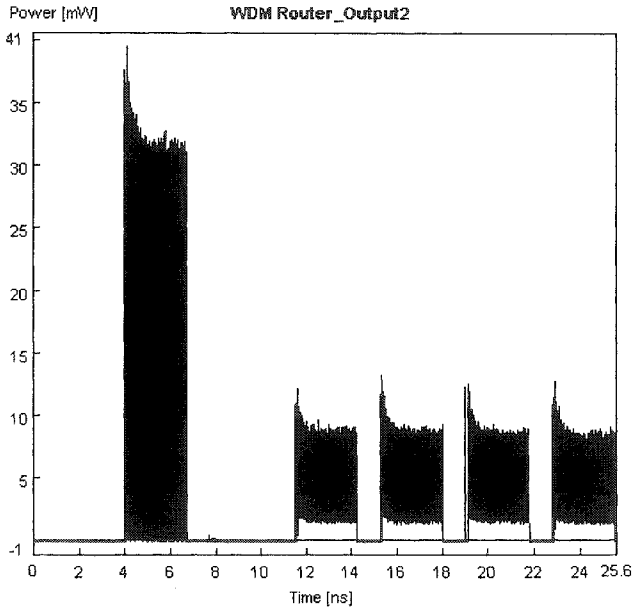
(d)


Power [dBm]
PPM-HP1_Output1
Time [ns]
Power [mW]
PPM-HP1_Output1
#0
#1
#9
Time [ns]

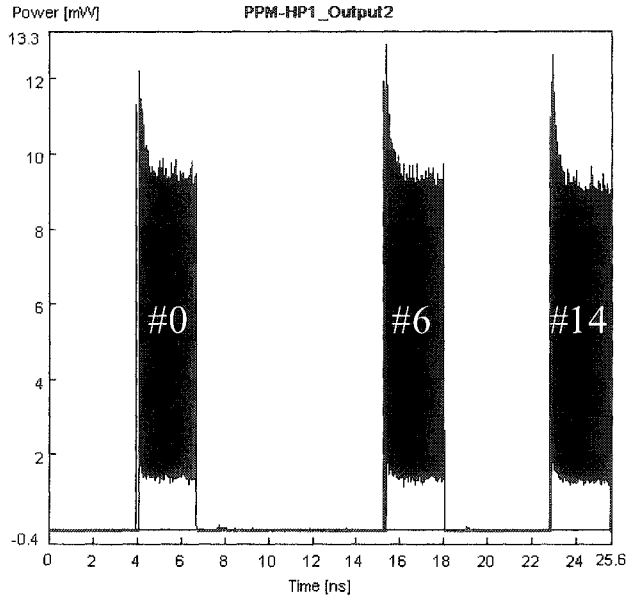
(e)


Power [mW]
PPM-HP2_Output1
#0
#4
#15
Time [ns]

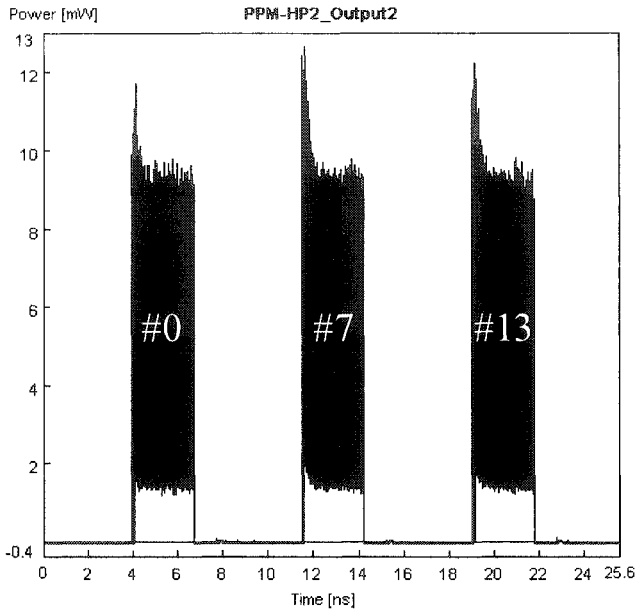
(f)


Power [mW]
WDM Router_Output2
41
35
30
25
20
15
10
5
-1
0 2 4 6 8 10 12 14 16 18 20 22 24 25.6
Time [ns]

(g)


Power [mW]
PPM-HP1_Output2
13.3
12
10
8
6
4
2
-0.4
#0
#6
#14
0 2 4 6 8 10 12 14 16 18 20 22 24 25.6
Time [ns]

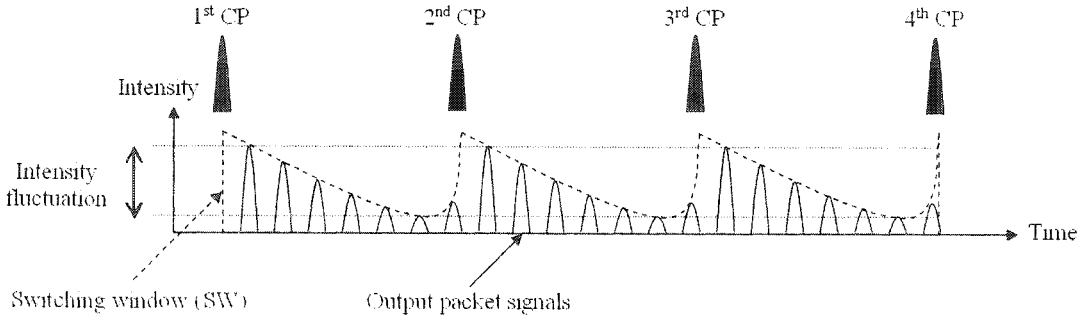
(h)



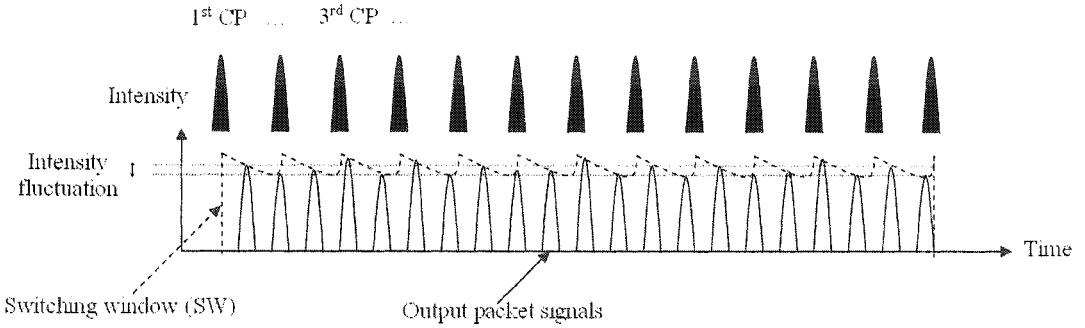
(i)

Figure 7.4 Packets observed at (a) the input of the WDM router, (b) the input of the PPM-HP1 (the inset shows the power fluctuation observed at the input of PPM-HP1), (c) the input of the PPM-HP2, (d) the output 1 of the WDM router, (e) the output 1 of the PPM-HP1 (the inset shows the power fluctuation observed at the output 1 of PPM-HP1), (f) the output 1 of the PPM-HP2, (g) the output 2 of the WDM router, (h) the output 2 of the PPM-HP1, and (i) the output 2 of the PPM-HP2

Packet waveform with a larger intensity fluctuation will be difficult for the conventional receiver employing a fixed threshold detector to determine the optimum threshold level, thus having problem to regenerate the signals at the receiver side [149, 243]. The intensity fluctuation can be further reduced by applying a series of control pulses to the OS to keep the switching window (SW) wide open to allow the entire packet to go through. This can be explained in Figure 7.5, after the first CP is applied to the upper arm SOA in the OS (i.e. a SMZ switch), the SW of the OS (shown as the dash line in Figure 7.5) is closed slowly due to the SOA gain recovery [56, 244]. In order to keep the SW open again, the following CPs are applied subsequently. As a result, the intensity fluctuation of the output packets can be reduced by applying more CPs during the same time period.



(a)



(b)

Figure 7.5 The output packet intensity fluctuation (a) is large as applying less CPs, and (b) the intensity fluctuation is reduced as applying more CPs

Inter-channel crosstalk (*CXT*) is an important issue in DWDM core networks that will result in transmission and node functionality impairment [67], and is defined as:

$$CXT = 10\log_{10}\left(P_{nt}/P_{t}\right), \tag{7.1}$$

where P_{nt} is the peak output signal power of all non-target channels (undesired wavelength) and P_t is the average output signal power of the target channel (desired wavelength). For evaluation of the router inter-channel *CXT* performance, two packets at λ_1 (packet 1 with address #4) and λ_2 (packet 2 with address #4) are sequentially applied to the input of the WDM router, see Figure 7.6.

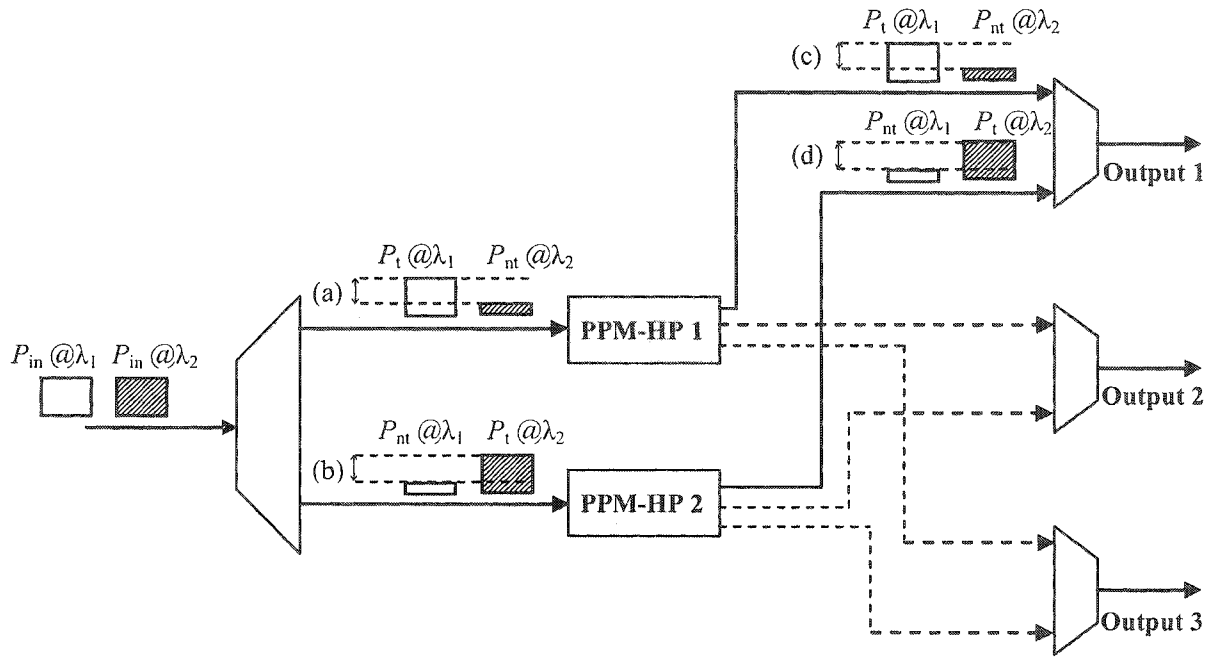


Figure 7.6 (a) The inter-channel *CXT* observed at input of PPM-HP1, (b) *CXT* observed at input of PPM-HP2, *CXT* observed at output1 of PPM-HP1, and (d) *CXT* observed at output1 of PPM-HP2

The inter-channel *CXT* observed at the input and output1 ports of PPM-HP1&2 for a range of channel spacing $\Delta f = f_2 - f_1$ is depicted in Figure 7.7. The CXT_{output} level is constant at -27 dB for 0.4 THz < Δf < 1 THz and it increases exponentially when Δf < 0.4 THz. In the Δf range of 0.8 THz to 1 THz, CXT_{input} is much lower than the CXT_{output} and increasing linearly if Δf < 0.8 THz. Minimum level of CXT_{output} is limited by the contrast ratio of the extracted clock signals from the CEM [224]. Note that the CXT_{output} is much lower than the CXT_{input} for 0.4 THz < Δf < 0.8 THz. The improvement in the *CXT* at the outputs of the PPM-HP is explained as follows: Signal emerging from the demultiplexer (i.e. the input signal of PPM-HP) at wavelengths other than the desired wavelength displays a very low input power (< 0.9 mW), as a result, no matched signals could be generated at the output of the AND gates. Packet is therefore directed to the non-target output port (i.e. the absorber port) of the optical switch.

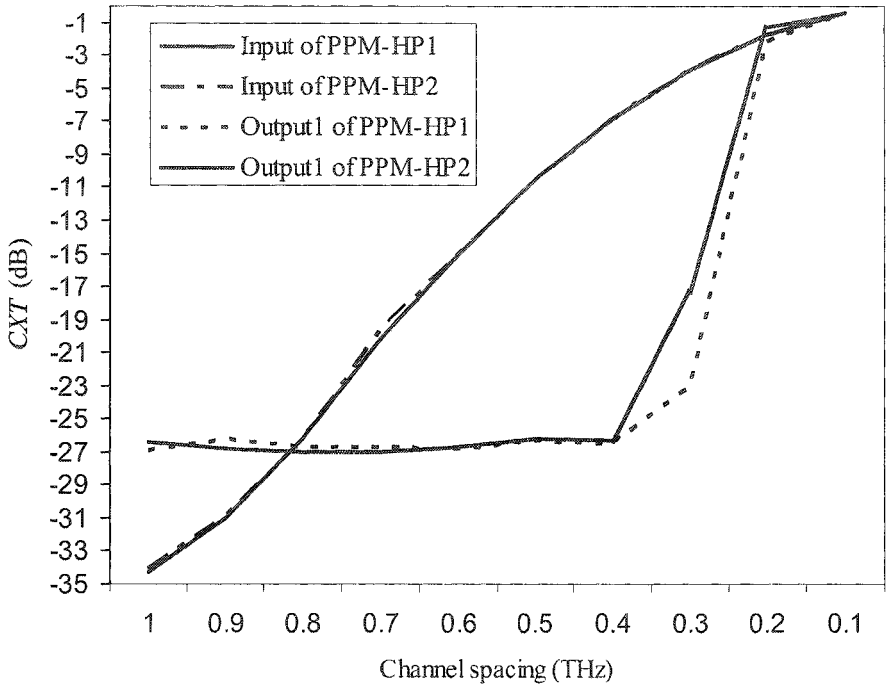


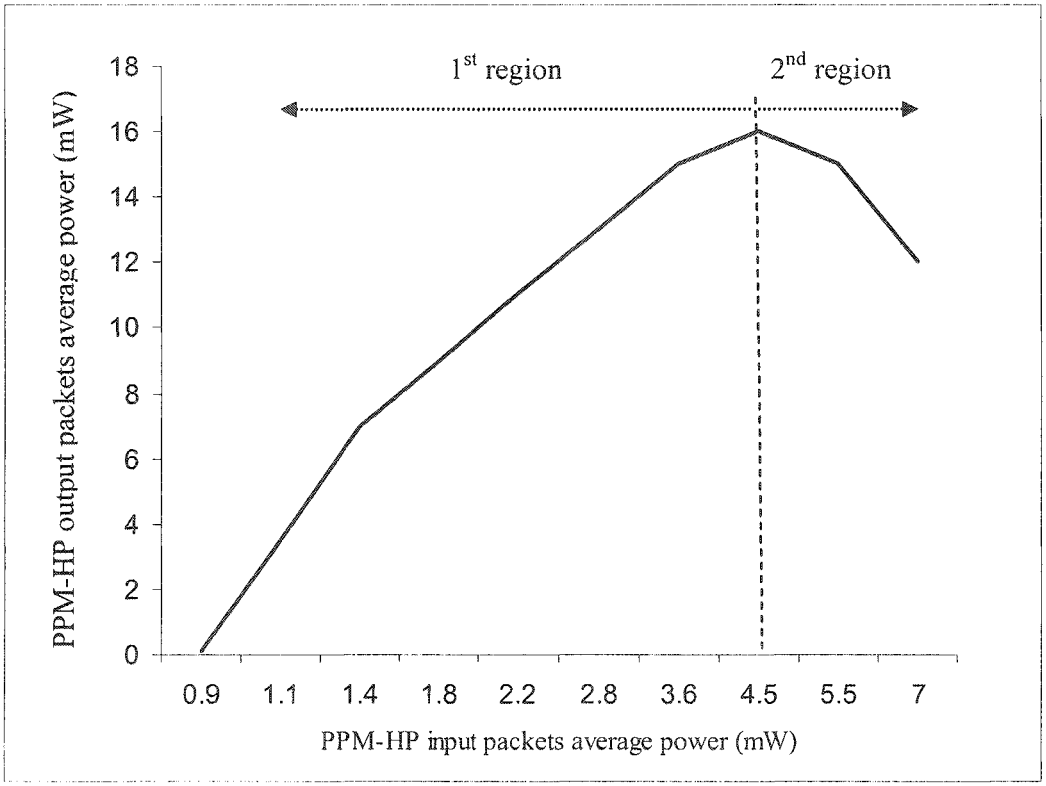
Figure 7.7 The inter-channel crosstalk (*CXT*) observed at input of PPM-HP1&2 and output1 of PPM-HP1 & 2 against the channel spacing (the bandwidth of the WDM multiplexers and demultiplexer is 500 GHz)

The average power of packets observed at the output2 and the input of PPM-HP1 module is illustrated in Figure 7.8(a), showing a linear relationship up to the input power of 3.6 mW, dropping at the input power of > 4.5 mW. The average output power of the PPM-HP module increases with the average input power of the PPM-HP reaching a maximum levels ~16 mW. The gain of PPM-HP module is coming from the gain of optical switches, see Figure 7.3. Note that, it is shown that the input packets average power in the first region before reaching the maximum value should be used, because the packets overshoot are severe (see Figure 4.8) and with lower output average power in the second region.

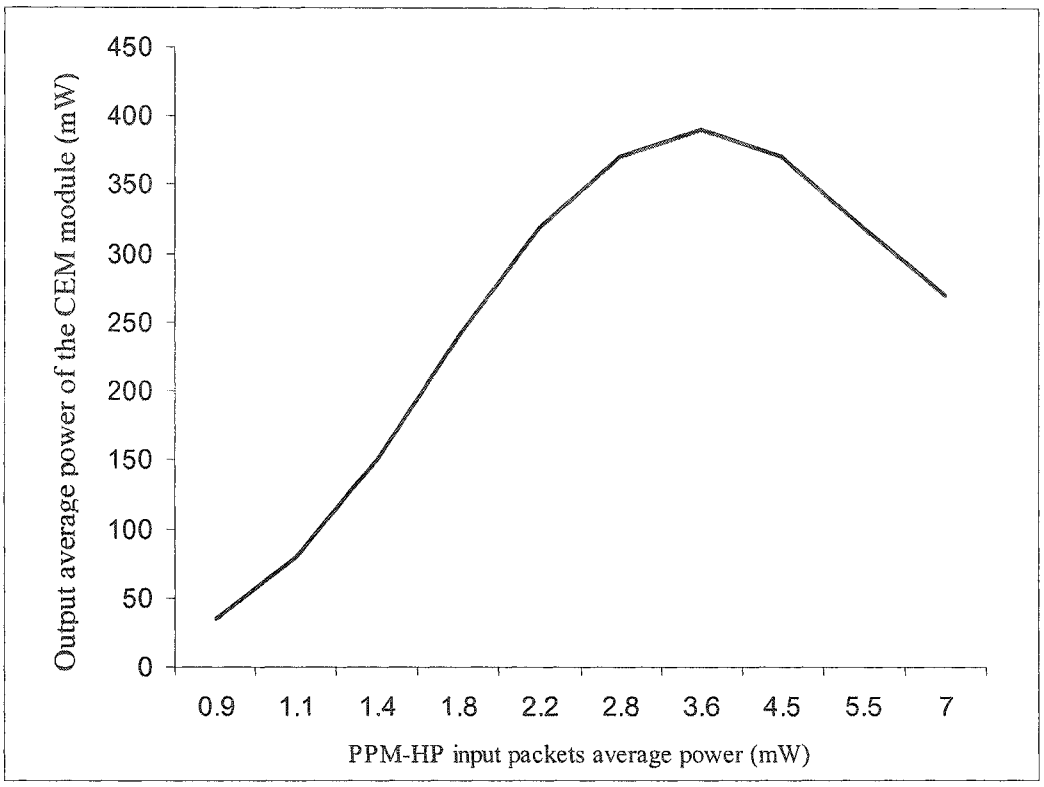
The drop of the PPM-HP output packets average power is mainly due to the drop of the extracted clock signals $c(t)$, this could be explained from Figure 7.8: The average

output power of $c(t)$ increases with the average input power of the PPM-HP reaching a maximum levels ~ 400 mW, dropping at the input power of > 3.6 mW. The drop of the output average power of $c(t)$ is because of the two-stage SMZ configuration of the CEM module [224], high input packet power leads to high CPs inside the CEM module, and eventually makes the phase difference between the upper and lower arm of SMZ lager than π, thus decreasing the output gain of the CEM module.

Packets with low input power lead to low extracted clock signals power, thus generating low power pulse sequences at the PPRT entries and the extracted PPM address. This leads to pulses with reduced power at the output of AND gates and therefore packets with lower power level at the output of the PPM-HP module.



(a)



(b)

Figure 7.8 PPM-HP input packets average power versus (a) PPM-HP output packets average power, and (b) output average power of the CEM module

7.4 Summary

In this chapter, an all-optical $1\times M$ router architecture for a WDM core network has been presented in Section 7.2. The PPM format adopted for the packet header address and the routing table entries offers fast correlation time and avoids the speed limitation imposed by the non-linear element based optical AND gates. Simulation results obtained in Section 7.3 have shown that this router can operate at 160 Gb/s with 0.3 dB of bit sequence power fluctuations of every packet observed at the output ports and a inter-channel *CXT* of ~ -27 dB at a channel spacing of greater than 0.4 THz and a demultiplexer bandwidth of 500 GHz. The output transfer function of the

PPM-HP module showed that input packets average power values below to 4.5 mW were suggested to adopt for achieving output packets with higher average power and lower packet overshoot.

CHAPTER 8 CONCLUSIONS AND FUTURE WORK

The important findings of the proposed all-optical router architectures and routing schemes are summarised in this chapter. The recommended extended research work based on the proposed schemes is also introduced. The challenges for realising a truly "transparent" all-optical networks and the future prospects of the next generation all-optical networks will also be discussed in this chapter.

8.1 Conclusions

All-optical clock extraction, header recognition/processing, address correlation, and switching are the main functionalities to realise an all-optical router for high-speed packet switching networks. The evolution history and the topology of today's optical networks were introduced together with different switching techniques such as OCDM, OCS, OBS, and OPS. The fundamental router architecture and the drawbacks of a number of different schemes for optical packet header processing were discussed. In almost all existing schemes packet header address identification at each node is carried out by correlating the packet header address with a routing table. For a large size network the size of routing table could be greater than half a million entries, thus leading to a very long processing time. In this research work, new routers employing PPM address correlation schemes based on single and multiple PPRTs were proposed and investigated offering fast address correlation time comparing to existing schemes. Additionally, by transmitting packet header address in PPM and/or hybrid format,

there is no need for address conversion modules in every router, thus leading to a less complex node architecture.

The fundamental building block adopted in the proposed all-optical router is the SMZ switch (with SOAs) that offers a short and square switching window, compact size, thermal stability and low-power operation. SMZ operation principle was outlined and its application in all-optical serial-to-parallel converter (SPC), all-optical logic gates and high contrast ratio (*CR*) 1×2 all-optical switch was investigated theoretically and by means of computer simulation. In practice, it is not simple to maintain an exact phase shift of 180° in SOAs. Therefore, in most cases, only the output port 1 of SMZs are used for switching purpose due to its low inter-output *CR*. A practical all-optical 1×2 router employing SMZs, should have a high inter-output *CR* for lower values of output crosstalk (*CXT*). A novel all-optical 1×2 switch based on three SMZs was proposed, offering a high inter-output *CR* (> 32 dB). Most of the reported AND gates exploit the XGM and XPM characteristics of SOAs with only two inputs inherited from 2×2 SMZ switch structures. Realisation of an AND gate with more than two inputs will require a hybrid approach combining parallel and cascaded two-input AND gates. This approach results in a complex optical circuit as well additional noise source due to the SOAs. In addition, employing more than one SOA per AND gate will effect the output amplitude modulation, the on/off ratio and input/output power characteristics. A new three-input AND gates based on FWM using a single SOA was proposed with reduced complexity and offering input data format transparency compared to the existing switch-based AND-gates.

By transmitting packets with conventional binary header address format, routers employing a single PPRT require a SPC module and an array of 1×2 switches to extract individual bits from the incoming binary packet header address and convert to PPM address format. For packets with a long header address, there will be increased switching stages, which will result in deterioration of the extinction ratio of the output PPM address and increased system complexity. By employing PPM packet header format, the PPM address conversion module is no longer required within a node, therefore the complexity of the router is significantly reduced. For optical packets with 4-bit binary address ($N = 4$), the all-optical 1×3 routers employing a single PPRT with an entry slot of 6.25 ps offered the fastest processing time of 112.5 ps (i.e. ~ 100 times faster than router using CRT) capable of operating at 160 Gb/s in the unicast, multicast and broadcast transmission modes. It was shown that predicted and simulated OSNR decreases by ~2 dB after each hop, thus limiting the size of network for packets to reach their destination.

The processing time of routers employing a single PPRT is mainly determined by the duration of a 2^N-slot PPM-frame. In large size networks with a longer PPM address frame length, the processing time will increase at every router, thus leading to decreased data throughputs. A new routing scheme employing multiple PPRTs was proposed where only a subset of the header address is converted into a PPM format, thus resulting in a reduced length of PPRT entries. In multiple PPRTs, the duration of a PPM-frame is reduced from 2^N to 2^{N-2} slots, thus offering four times faster processing time compared to routers with a single PPRT. However, for packets with a conventional binary header address format, the operation speed of the router is limit to

80 Gb/s. This is due to the PPM conversion module with a low extinction ratio at the output PPM address at a high bit-rate operation.

In a conventional binary packet header address format, routers employing multiple PPRTs still require a SPC, an array of 1×2 optical switches, and the FDLs to convert a subset of binary address to a PPM format. To increase the data rate and reduce the complexity of routers with multiple PPRTs, packet header address with a hybrid format was proposed, where PPM address conversion module is no longer required. The simulation results have shown that the router can operate at 160 Gb/s with output intra-channel *CXT* of up to -18 dB and with an output packet power fluctuation of 2 dB, which is largely dependent on the inter packet guard time. In amplified systems, intra-channel *CXT* of -18 dB results in ~ 1 dB power penalty at the receiver [62]. In multi-hop routing, the accumulated packet power fluctuation will deteriorate the system BER performance and leads to switching failures of the router. The effects of packet power fluctuation against the router forwarding capability and BER performance need to be further investigated.

Also proposed was a WDM based router where optical packet processing is carried out at multiple wavelengths simultaneously. The proposed WDM router employing a single PPRT offers faster processing time compared to the routers with CRT, and uses fewer components compared to the existing all-optical router employing wavelength conversions and all-optical flip-flops. Simulation results have shown that WDM based router can operate at 160 Gb/s with 0.3 dB of bit sequence power fluctuations of every packet observed at the output ports and an inter-channel *CXT* of ~ -27 dB at a channel spacing of greater than 0.4 THz and a demultiplexer bandwidth of 500 GHz. In

amplified systems, inter-channel *CXT* of -27 dB only results in ~ 0.1 dB power penalty at the receiver [62].

8.2 Future Work

The proposed further research would start with building a testbed for a single PPM-HP to demonstrate the PPM address correlation. In the practical implementation, the packet clock bit could be transmitted at a different wavelength from the payload bits in order to simplify the clock extraction process by employing an optical bandpass filter. Additionally, the contention problems must be addressed to build an $M \times M$ router for WDM packet-switched core networks. Wavelength conversion modules and additional logic circuits with FDLs could be adopted in the PPM-HPs to solve the contention problems.

Further theoretical analysis to investigate the router's BER and packet error rate performances as well as the relationships between the timing jitter effect and the router output crosstalk would be a logical step forward. Additionally, the effects of packet power fluctuation against the router forwarding capability and BER performance needs to be further investigated. The maximum operation speed of the router is ~ 200 Gb/s, which is limited by the pulse width of the commercial available laser sources (~ 2 ps). Moreover, in order to increase the throughput of the router, the packet guard time could be reduced by employing SOAs with a faster gain recovery time. In multiple-hop routing, the packet forwarding capability of the router is mainly deteriorated by the accumulated noise, the packets overshoot, and the output packets

average power fluctuation. All-optical regenerators and optical power equalisers could be adopted to enhance the forwarding capability of the router.

Nowadays, SDH/SONET dominates the core optical networks. SDH/SONET is used worldwide as it supports a wide range of networking operations such as error monitoring, performance monitoring and network management [86]. The next generation SDH/SONET [86] will be compatible with the variable-length and multi-protocol packets, therefore demonstrating their flexibility and adaption capability to serve as the main transport network for many years. However, in SDH/SONET networks, most functions such as multiplexing, cross-connection, add/drop and routing processing will still be performed in the electrical domain.

Up to now, all-optical signal processing is still an immature technology compared to its electric counterpart. Optical packet-switched (OPS) networks are still not ready for deployment based on today's technologies. A number of challenges still needs addressing, thus hindering the implementation of a truly "transparent" optical network, such as to build a larger scale and more cost-effective all-optical switches, to solve the contention problems, and to deign a more intelligent algorithm and more bandwidth efficient network architecture. Apart from the technical perspective, another hindrance for the deployment of OPS networks is that network operators are reluctant to re-engineer the existing networks due to the considerable expense of replacing existing network equipments.

APPENDIX – A VIRTUAL PHOTONIC SIMULATION SOFTWARE

VPI is a powerful simulation software developed by the VPIsystems, Inc. (http://www.vpiphotonics.com) since 1997. VPIsystems provides the modelling, mathematic evaluation and estimation. In addition, VPI software also offers a flexible Photonic Design Automation (PDA) environment to support requirements in optical component and systems design which makes the users easily control the parameter sets to extensively explore the optical system design.

Figure A.1 illustrates a simple example for observing the switching window profile of the SMZ:

Step 1: Start VPI simulation software by executing "VPItransmissionMaker 7.5.exe", and then click on the TC Modules.

Step 2: Select the required components from the corresponding folders.

Step 3: Drag the desired components to the workspace, and connect the modules.

Step 4: Edit the parameter values.

Step 5: Click the "little green man" to run the simulation. The simulation result is shown in Figure A.2.

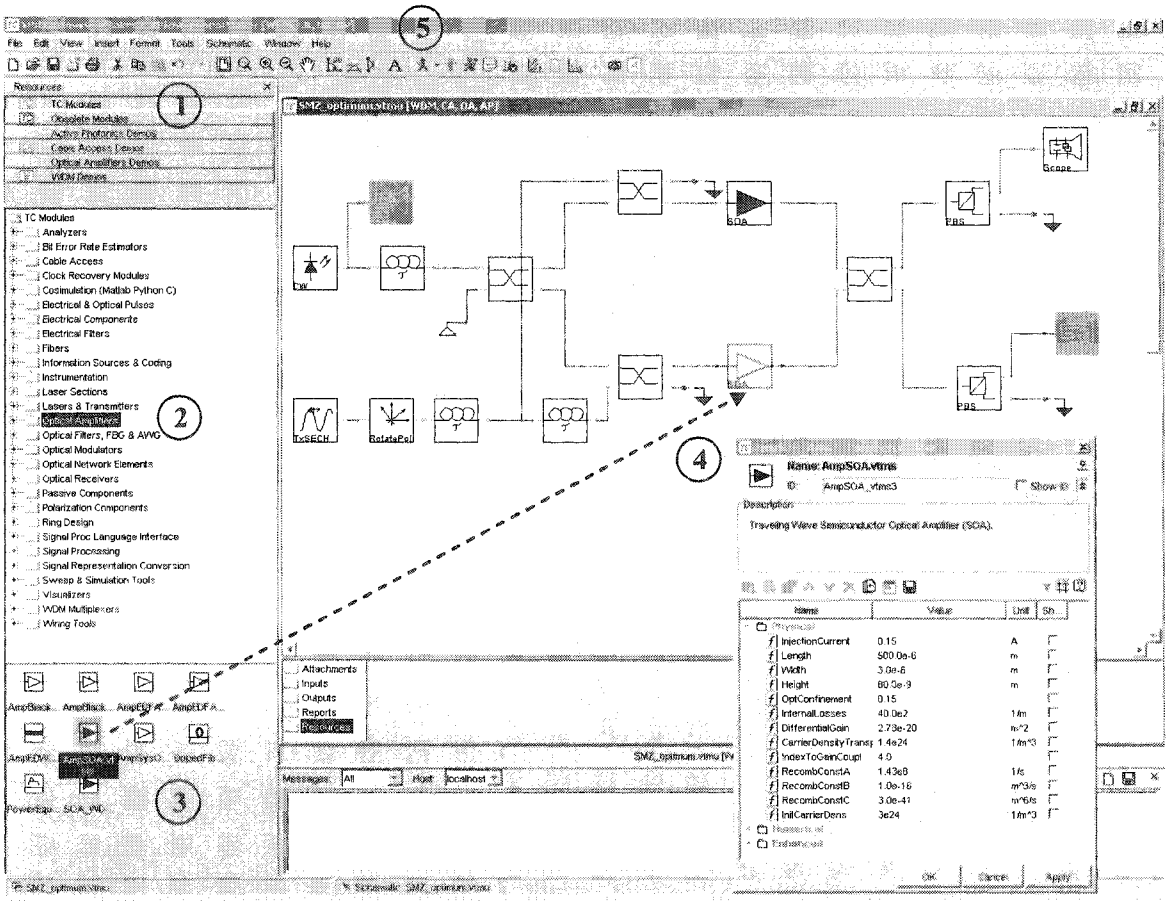


Figure A.1 An example of using VPI simulation software

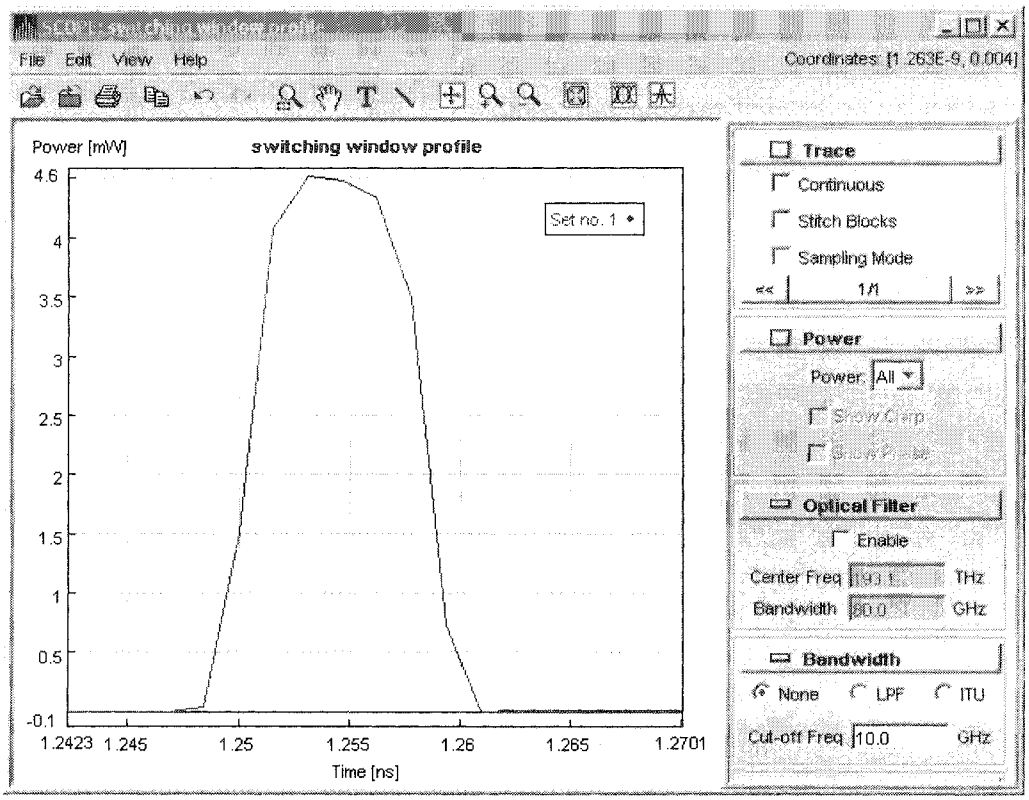


Figure A.2 The switching window profile of the SMZ

APPENDIX – B SYMMETRIC MACH-ZEHNDER

Figure B.1 shows the photo of CIP quad regenerator, which comprises four SMZs. The layout and the pin descriptions of the quad regenerator are shown in Figure B.2 and Table B.1, respectively. In practical systems, phase shifters (PS) are required to adjust the phase different between two SMZ arms, see Figure B.3. By carefully adjusting the applied voltages to the phase shifters, the output extinction ratio will be improved.

Discriminating different polarisation from the control pulse might be an issue in practical system. However, adopting counter-propagating control pulses or employing control pulses at different wavelengths are the alternative solutions.

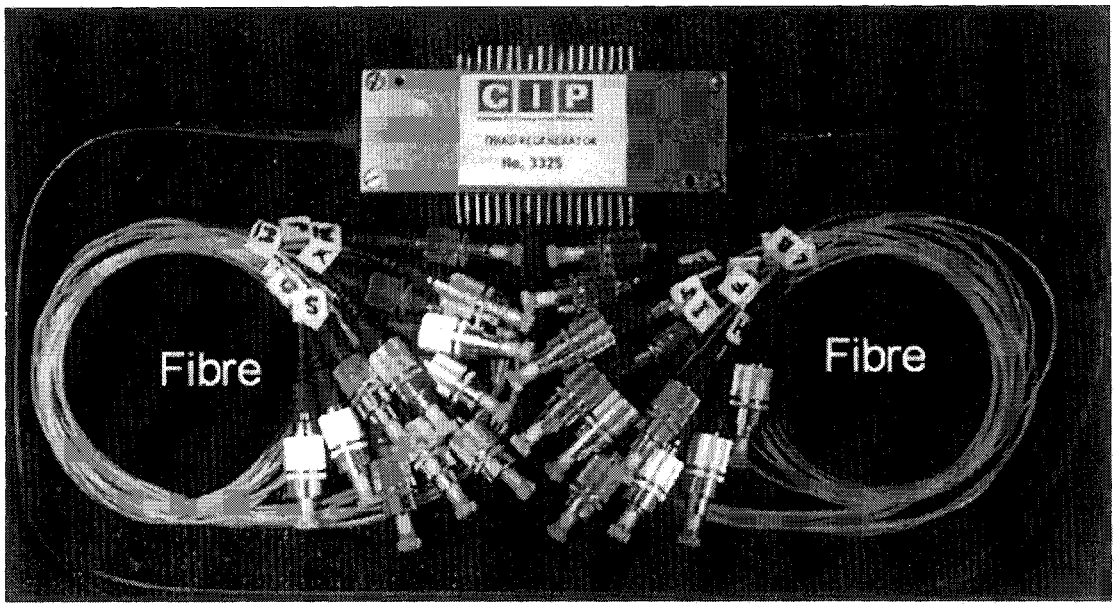
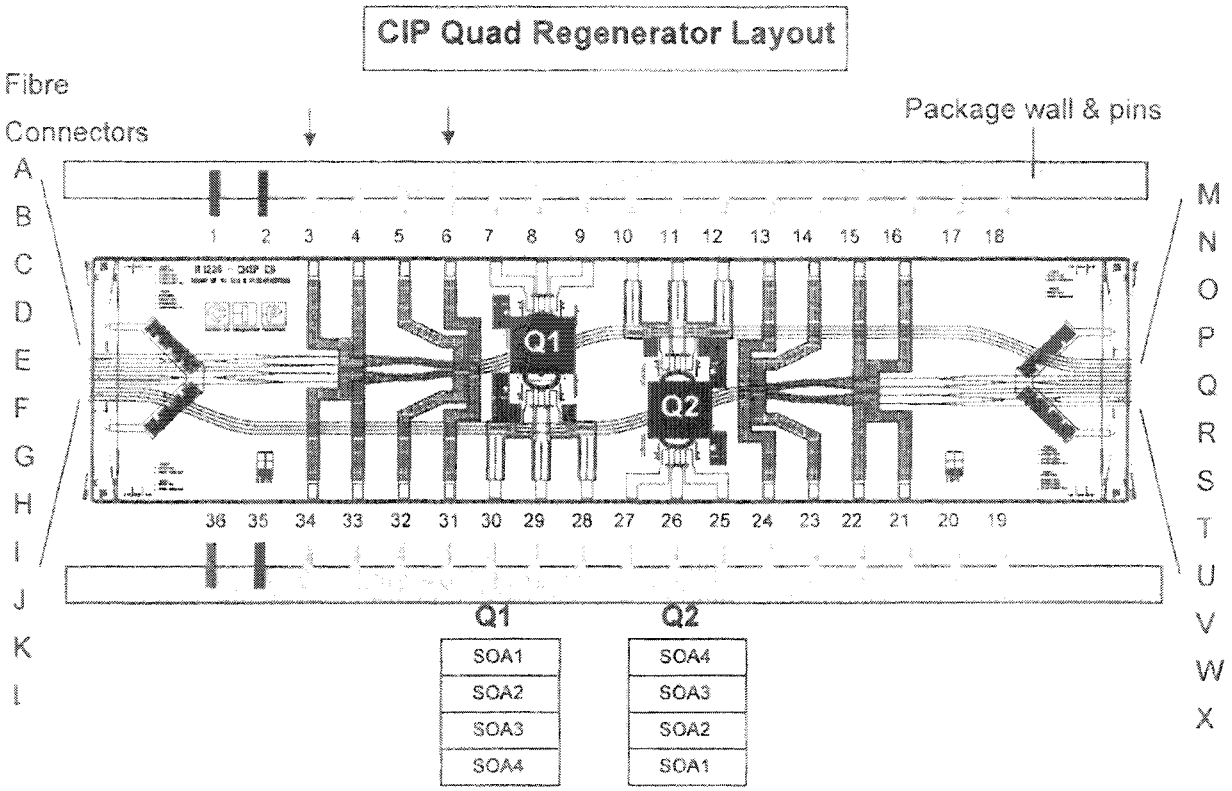


Figure B.1 The photo of CIP quad regenerator which comprises four SMZs



	MZI input waveguides	MZI output waveguides	Switching data input waveguides	SOAs
Regen #1	B,C	M,N	A,D	Q1 SOA 1 & SOA 2
Regen #2	F,G	O,P	E,H	Q1 SOA 3 & SOA 4
Regen #3	R,S	I,J	Q,T	Q2 SOA 3 & SOA 4
Regen #4	V,W	K,L	U,X	Q2 SOA 1 & SOA 2

Figure B.2 The layout of CIP quad regenerator

Table B.1 Pin descriptions of the CIP quad regenerator

1	Thermistor	10	Q2 SOA 4 (+ve)	19	Not connected	28	Q1 SOA 4 (+ve)
2	Thermistor	11	Q2 SOA 3 & 4 (-ve)	20	Not connected	29	Q1 SOA 3 & 4 (-ve)
3	PS 1 Regen #1	12	Q2 SOA 3 (-ve)	21	PS 1 Regen #4	30	Q1 SOA 3 (+ve)
4	PS 2 Regen #1	13	PS 1 Regen #3	22	PS 2 Regen #4	31	PS 1 Regen #2
5	PS 2 Regen #1	14	PS 2 Regen #3	23	PS 2 Regen #4	32	PS 2 Regen #2
6	PS 1 Regen #1	15	PS 2 Regen #3	24	PS 1 Regen #4	33	PS 2 Regen #2
7	Q1 SOA 1 (+ve)	16	PS 1 Regen #3	25	Q2 SOA 1 (+ve)	34	PS 1 Regen #2
8	Q1 SOA 1 & 2 (-ve)	17	Not connected	26	Q2 SOA 1 & 2 (-ve)	35	Peltier (-ve)
9	Q1 SOA 2 (+ve)	18	Not connected	27	Q2 SOA 2 (+ve)	36	Peltier (+ve)

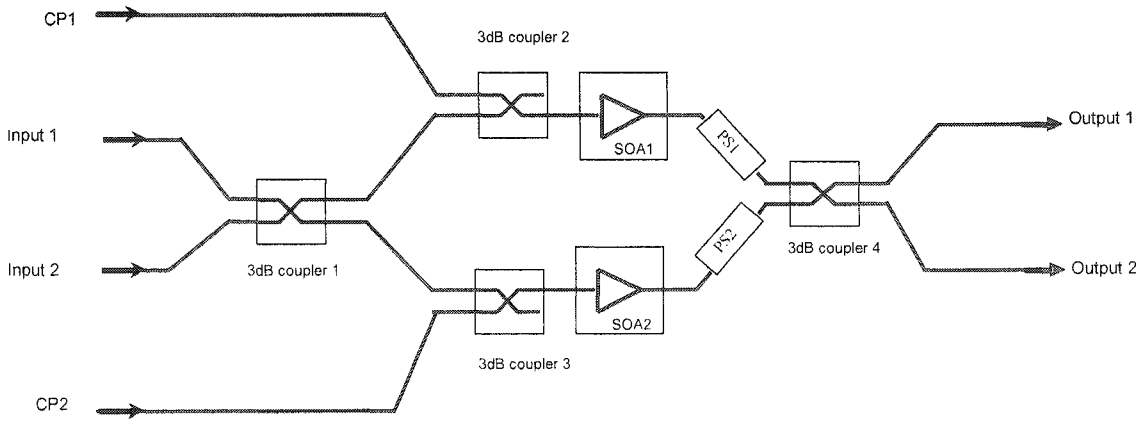


Figure B.3 SMZ with phase shifters (PS)

Note that, all simulations done in this research assume that the SOA has a polarisation-independent gain. However, in practical experiments, SOA has a polarisation-dependent gain thus inducing polarisation ration on the input signals [245-247]. As a result, in practical, CPs are often used at different wavelengths with respect to the input signal. Instead of using PBS, a bandpass filter is used in the output for separating the input signal and CPs.

APPENDIX – C SOA GAIN RECOVERY TIME

In end of 2007, CIP Technologies (http://www.ciphotonics.com/) has successfully developed an advanced SOA offering a gain recovery time of 10 ps [248]. This is a breakthrough for optical systems operating at up to 100 Gb/s.

Moreover, the injection of an optical beam in SOA (i.e. holding beam schemes) [249-251] has also been proposed to improve the SOA gain recovery time below to 20 ps [252].

APPENDIX – D CLOCK EXTRACTION MODULE (CEM)

The clock extraction module is first proposed in [224]. Figure D.1 shows a schematic block diagram of the CEM, which employing two inline SMZs in order to achieve clock signal with low residual crosstalk. The operating principle of the CEM could be explained as follows, which is extracted from [201]:

"(a) The arriving packet is directed to the input of SMZ-1 after being delayed by $T_{SW}/2$. Two amplified (by a gain G_{CP}) versions of the arriving packet, one with no delay and the other delayed by T_{SW}, are fed into the control ports as CP_1 and CP_2, respectively. The control and input signals applied to each SMZ are set in an orthogonal-polarisation state by a PC and are separated by a PBS at the SMZ output. With no CPs (CP_1 and CP_2) at locations (b) and (d) the SMZ-1 is in the balanced state (both SOAs gains and phases are identical) resulting in no signal at its output port (e). In the presence of CPs SMZ-1 is in the imbalanced state (i.e. transmitting mode) and has a SW width of T_{SW}, thus allowing the input signal to emerge from its output port, see point (e). The time delay T_{SW} is selected smaller than a single bit duration T_b, thus only extracting the clock bit using SMZ-1.

The incoming data packet consists of a single clock bit ahead of the address and payload bits, see Figure 2.5. On arrival of the 1st pulse (binary "1" or packet's clock pulse) of CPs, the gains of the SOAs in SMZ-1 will drop. However, as both CPs are amplified packets containing random "0" and "1" bits, the SOA gain starts to recover during bit "0"s since no CPs are present. Successive binary "1"s in the CPs will again create their new residual SW, thus allowing it to emerge at the output of SMZ-1

following the extracted clock bit, see location (e) in Figure D.1. However the intensities of these residual bits "1" are lower than the intensity of the extracted clock bit due to the SOA gain recovery time being typically much greater than the relatively small T_b in high-speed networks (i.e. T_b ~ picoseconds) resulting in low residual SW gain.

In order to suppress the residual signals at the output of SMZ-1 and achieve a higher *CR* in clock extraction, a SMZ is used in cascade (i.e. SMZ-2 with SMZ-1). The extracted signals from SMZ-1 are used in SMZ-2 with the same input/control configurations as in SMZ-1 except for differently chosen input/control powers. The CPs (shown at points (f) and (h)) in SMZ-2 will create a main SW to extract the clock pulse with a high intensity at the output of SMZ-2. Note that due to low-intensity residual signals appearing at the input (at (g)) and control ports of SMZ-2, the gain of the main SW is much larger than the gain of the newly generated residual SWs. As a result, the intensity of the residual signals at the CEM output, see location (i), is further reduced in comparison to the extracted clock pulse."

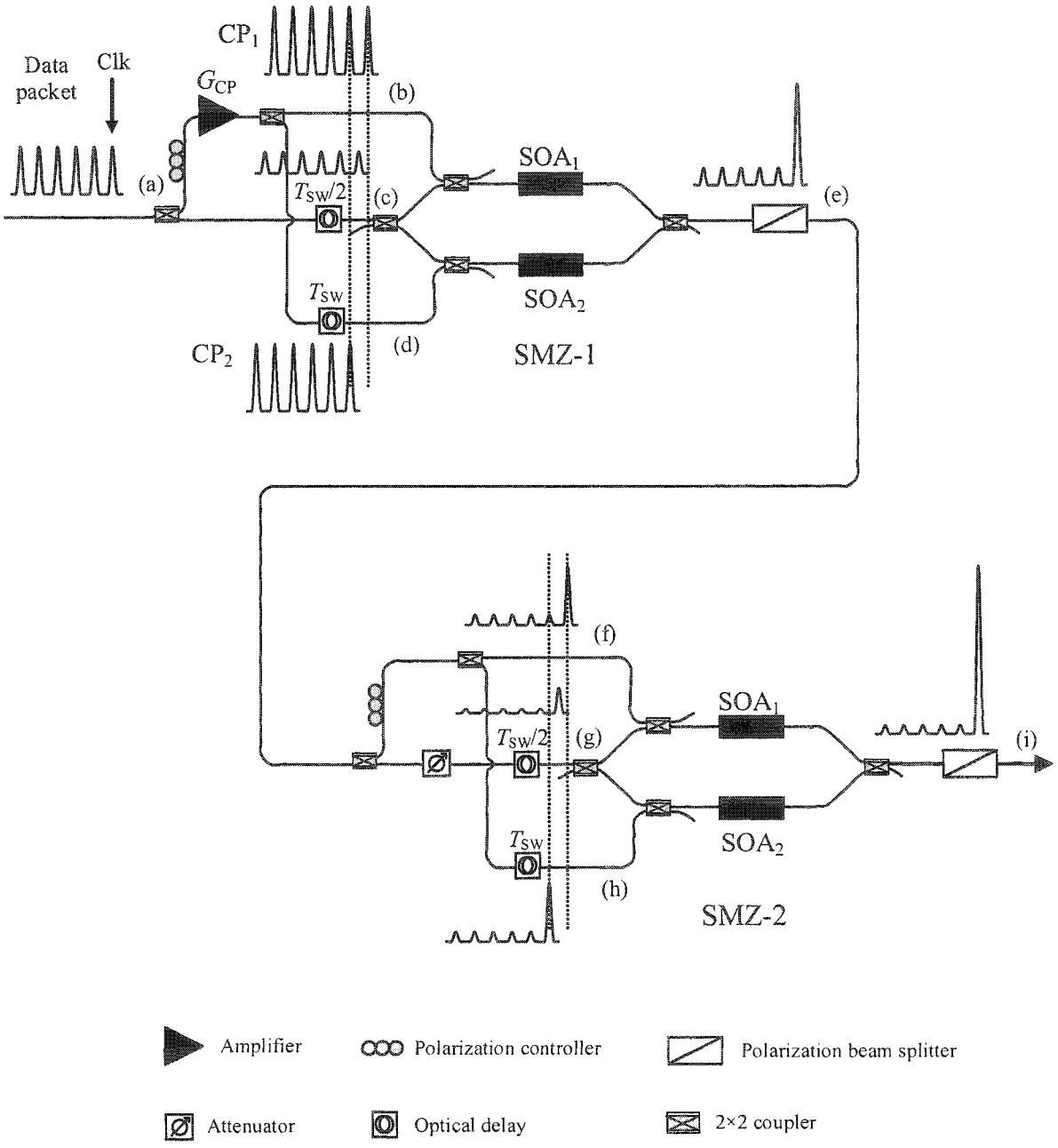


Figure D.1 Clock extraction based on two inline SMZ switches [201]

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