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Citation: Amirkhalili, Arezoo (2017) CdTe Solar Cells in Substrate Configuration: Influence of Mo, Na, Cl and Mg Treatments to Promote Recrystallization in the Absorber Layer. Doctoral thesis, Northumbria University.

CdTe Solar Cells in Substrate Configuration: Influence of Mo, Na, Cl and Mg Treatments to Promote Recrystallization in the Absorber Layer

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PhD 2017

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UNIVERSITY NEWCASTLE

CdTe Solar Cells in Substrate Configuration: Influence of Mo, Na, Cl and Mg Treatments to Promote Recrystallization in the Absorber Layer

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A thesis submitted in partial fulfilment of the
requirements of the University of Northumbria at
Newcastle for the degree of

Doctor of Philosophy

Research undertaken in the
Faculty of Engineering & Environment

April 2017

Dedicated to my loving parents and brother,

Saeid, Sima and Azad.

Abstract

Cadmium telluride (CdTe) is the leading thin-film photovoltaic material with efficiency up to 22.1 % (superstrate configuration). Devices developed in the substrate configuration allow roll-to-roll processing using lightweight and flexible substrates; however, exhibit a lower efficiency (13.6 % on glass substrate). This work focuses on the properties of metal-organic chemical vapour deposition (MOCVD) grown CdTe thin film and devices deposited on molybdenum (Mo) coated glass (substrate configuration). Particular attention is given to the role of sodium (Na) and chlorine (Cl).

A Cl-treatment was performed using either MOCVD-$CdCl_2$ or solution-$MgCl_2$ on MOCVD-grown CdTe Mo-coated glass before formation of the *pn* junction. Devices were completed with the deposition of windows layers (i-ZnO and ITO) and a front metal contact grid (Ni-Al).

Initially, the Mo properties and their effect on Na diffusion from the soda-lime glass (SLG) were investigated. Sputtering conditions were set to achieve Mo layers with a nominal thickness of 1 μm and sheet resistance and resistivity ranging between 0.16 – 0.59 Ω/☐ and 16 – 66 μΩ·cm, respectively. The variations of resistivity are linked to the Na content in the Mo film: for a given deposition power, an increase in resistivity yields a lower Na diffusion in Mo.

Relying on the diffusion of Na from the SLG substrate is not suitable for flexible or metal substrates; therefore, a second approach was investigated using a thin sodium fluorine layer. It was observed that the inclusion of Na between the substrate and the Mo enlarges the CdTe grains following $CdCl_2$ treatment by 50 % but weakens the adhesion to the substrate. The introduction of Na between the Mo and CdTe layer promotes the formation of large faceted grains for the as-grown films with an average grain size 10 times larger than in the case of Na-free deposition while maintaining a good adhesion to the substrate. The devices had a low efficiency (< 5 %) arising from weak *J–V* parameters despite the improved open circuit voltage.

The replacement of the $CdCl_2$-treatment with $MgCl_2$ was tested and this did not affect the morphology or structure of the films and showed limited efficiencies. An investigation in widening the window layer bandgap by addition of cadmium zinc sulfide was successful as improvements in the optical transmission at wavelength range of 400 < ! < 550 nm and the short circuit current were measured.

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Symbol	Name	Unit
A	Diode quality factor	-
c	Speed of light in a vacuum	$?/@$
A_B, A_D	Comparable constants in Auger recombination	-
A_{EFG}	Texture coefficient	-
AH	Correction factor	-
D	Diffusion constant	$?^{I}/@$
$\mathbf{J}_B$, $\mathbf{J}_D$	Electron and hole diffusion coefficients	$K?^{I}/@$
E	Photon energy	eV
L_M	Electron beam energy	keV
L_N, L_O	Acceptor, donor electron energy	eV
L_P	Energy of bottom of conduction band	eV
L_Q	Fermi level energy	eV
L_R	Energy bandgap	eV
L_S	Ionisation energy	eV
L_{QB}, L_{QD}	Electron, hole Fermi level energy	eV
L_T	Energy of top of valence band	eV
U(L)	Fermi distribution function	-
HH	Fill factor	%
G	Net generation rate	$K?^{VW}/@$

h	Planck's constant	Y @
h, Z, [	Miller's indices	-
$\backslash$	Sputtering current	A
$\backslash_{EFG}$	Intensity of peak	-
Y	Current density	$?]/K?^{I}$
$Y_{\wedge}$	Saturation current density	$?]/K?^{I}$
$Y_{\_}$	Light generated current density	$?]/K?^{I}$
$Y_{`D}$	Maximum power current density	$?]/K?^{I}$
Y_{B}, Y_{D}	Electron, hole current density	$?]/K?^{I}$
Y_{ab}	Short circuit current density	$?]/K?^{I}$
Z	Boltzmann's constant	Y/c
L	Crystallite size	d?
e_{B}, e_{D}	Electron and holw diffusion lengths	K?
đ	Refractive index	-
d	Number of reflections	-
d_{S}	Intrinsic carrier density	$K?^{VW}$
d, f	Electron and hole densities	$K?^{VW}$
d_{D}, f_{B}	Minority carrier densities	$K?^{VW}$
d_{Dg}, f_{Bg}	Equilibrium carrier densities	$K?^{VW}$
d_{h}, f_{h}	Electron, hole trap state densities	$K?^{VW}$
i_{j}	Lightly doped material concentration	-
i_{P}, i_{T}	Band density of states	$K?^{VW}$

$\mathbf{i}_N$, $\mathbf{i}_0$	Acceptor, donor density	K?^{VW}
P	Sputtering pressure	mTorr
p	Momentum	Zk ?/@
P_{in}	Input power	W
P_{max}	Maximum output power	W
l	Electronic charge	C
m	Net recombination rate	-
m_{NnRop}	Auger recombination	-
m_{a_q}	Shockley-Read-Hall recombination	-
m	Radiative recombination	-
m_r	Series resistance	$\Theta\ cm^2$
m_{rE}	Shunt resistance	$\Theta\ cm^2$
$m_\square$	Sheet resistance	$\Theta/\square$
s	thickness	d?
t	Temperature	°C
u	Voltage	V
u_{vb}	Open circuit voltage	V
u_{MS}	Built-in voltage	V
$u\text{`}_D$	Maximum power voltage	V
W	Depletion region width	-
w_B, w_D	Electron, hole depletion region penetration	-

x	Lattice parameter	Å
	Strain	-
ε_s	Dielectric permittivity	F/m
z	Electric field in *x*-direction	V/cm
ι	Efficiency	%
ε	X-ray incident angle	°
	Wavelength	nm
{B, {D	Electron and hole mobilities	K?ᴵ/u@
|	Photon frequency	Hz
π	Resistivity	0cm
	Degree of preferred orientation	-
}B, }D	Electron, hole lifetime	s
~j	Barrier height	eV
~`, ~r	Work function of metal, semiconductor	eV
~D	Work function of *p*-type CdTe	eV
χ_n, χ_p	Electron, hole affinity	eV

Acknowledgements

Firstly, I would like to acknowledge the financial support received from the University of Northumbria in the form of a full PhD studentship, laboratory equipment and grants to attend workshops, an international summer school and an international conference.

Secondly, I would like to thank all the individuals that contributed to this outstanding research experience and apologise in case I have missed anyone that supported me during my PhD. Your support helped me to be where I am today, so thank you.

The first person I would like to express my gratitude to is my principle supervisor, Dr Guillaume Zoppi, for guiding me through my PhD by giving me constant constructive feedback and unbelievable support. His enthusiasm, professionalism, technical expertise combined with his exceptional knowledge on the subject provided me with a great path to follow. Working with him was an immeasurable privilege.

I would like to acknowledge Dr Vincent Barrioz and Dr Neil Beattie for their support and guidance. Additionally, I would like to extend my gratitude to Dr Yongtao Qu for his patience and constant assistance during the long hours in the laboratory. I could not have asked for a better team and I am very grateful to have worked with this amazing group.

I would like to thank my parents, Dr Saeid Amirkhalili and Sima Minooie, for everything that they do and provide me with, every single day. I would not be who I am today if it weren’t for their unconditional love, support and guidance. One of my goals in life is to make them both proud and to show them that I appreciate all the sacrifices they have made. I hope I have made you proud and continue to exceed your expectations.

I would like to thank my amazing brother, Azad Amirkhalili, for his support and endless love. I am lucky to have him as my big brother and role model. I appreciate all that he does for me every single day and I can only hope he feels the same way.

I would like to thank my best friend, Krizia Rasile for mentally supporting me through this experience and picking me back up when I was at my worst. Her constant enthusiasm and excitement during my PhD made me want to work harder, so thank you for making me strive harder.

I would like to thank my best friend, Sanaa Rafay for making my life in the UK pleasant and always being there for me. Thank you for being my UK family and making me feel like at home. I appreciate everything you have done for me and your endless support.

Finally, I would also like to thank Rayana Boubezari for her continuous encouragement during this experience. Going through this journey of becoming doctors together was the most amazing experience. I could not have asked for a better person to share this success with. WE DID IT!

Declaration

I declare that the work contained in this thesis has not been submitted for any other award and all the work presented in this was carried out by the candidate except those procedures listed below.

The CdTe and $CdCl_2$ depositions were performed at the Centre for Solar Energy Research (CSER), Swansea University by Dr Vincent Barrioz.

Any ethical clearance for the research presented in this thesis has been approved. Approval has been sought and granted by the University Ethics Committee on the 28th of February 2014.

I declare that the word count of this thesis is 37,471 words.

Candidate:

Date:

________07/04/2017_________

CHAPTER 1

1 Introduction to Photovoltaic Technology

This chapter presents a brief overview on photovoltaic (PV) technology. After stating the motivation and aim behind this study, an outline of the thesis is given.

1.1 Renewable Energy Technologies

Renewable energy technologies have gained increasing interest due to their potential to replace a significant part of the electricity generation by using natural sources. There are several categories of renewable energy technologies including solar, wind, geothermal, hydropower and biomass. Historically, the production cost of energy from renewable sources has been higher than traditional sources of fossil fuels (coal, petroleum and natural gas). However, fossil fuels cannot last forever and supplies will decrease within decades if not years [1]. Therefore, it is important to develop large-scale alternatives to burning fossil fuels. Recent improvements in the renewable technologies has reduced their production costs in some cases being cheaper than fossil fuels. In addition, renewables have proved that they can generate electricity for a wide range of applications, scales, climates, and geographic locations. These technologies have made it possible for rural homeworkers as well as remote transmitter station to access clean electricity without building a road to transport diesel fuel. The statistics from the World Energy Council [2] in figure 1-1 shows how renewable energy consumption has grown over the past 15 years. The growth in the renewables energy market, particularly in terms of investment, new capacity and high growth rates in developing countries has changed the energy market.

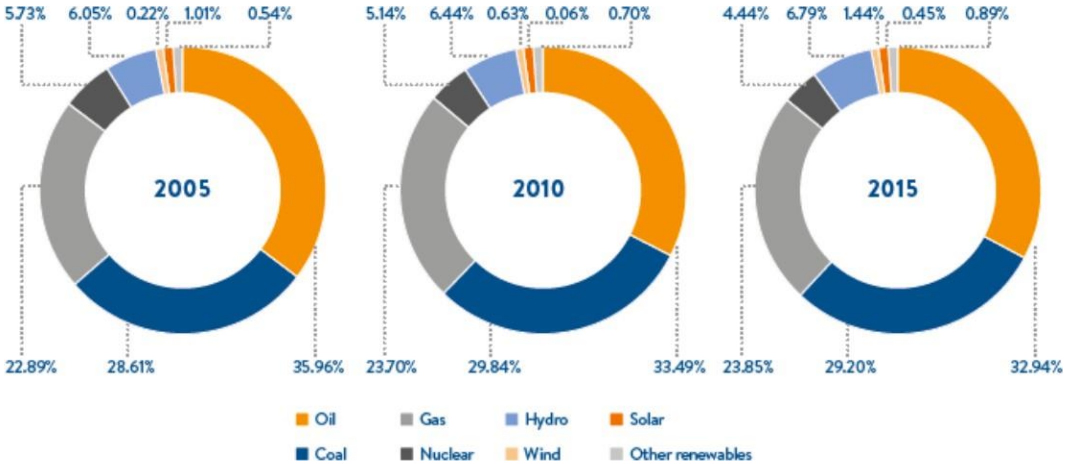

Figure 1-1: A comparative primary energy consumption over the past 15 years [2]**.**

Every day human beings are becoming more aware of the need for sustainable management of the planet Earth. The world's population is growing and so is the appetite for energy demand. PV has the potential to play a key role in energy production mix over the next few decades. The global installed capacity to produce electricity from solar energy has seen an exponential growth. By the end of 2015 electricity net reached around 227 GW, or 1 % of global electricity usage [2]. In 2015, the total capacity for solar heating/cooling in operation was estimated at 406 GW [2]. PV power plants have a shorter planning time than most other technologies and the PV module prices have dropped ~ 80 % since 2007 (from ~ US $ 4 /W in 2007 to ~ US $ 1.8 /W in 2015) [2]. Even though the cost associated with balancing the system rises a challenge, once installed, little maintenance is required, resulting in an extremely low maintenance cost. PV modules also have a long lifetime > 25 years [3].

It is interesting to note that wind is generated as a by-product of the sun interaction with the Earth (through heating the Earth in equatorial and Polar regions). It has been calculated [4] that about 1 % of the solar energy received on Earth (10 times the current world energy demand) is converted into wind; however, only 4 % of this is usable. It has been estimated that with aggressive exploitation, wind (both on-shore and off-shore) generation could provide about 10 % of the world's energy demand [5]. Waves are caused by wind and therefore a small portion of the wind energy is passed on, which means waves also originate from solar energy. Hydropower, electricity created by flowing waters, uses solar energy to produce a small portion of the total energy income by transporting water from the sea to land. Biomass also converts waste into fuel using solar energy however it has low efficiencies and its use for food is more important. In brief, the direct utilisation of the solar energy is the real big energy resource [6].

At sea level the sun provides approximately 1 kW/m^2, with a power of 102,000 TW [7]. This powers the ecosystem, the environment, and helps sustains life on Earth. The amount of energy arriving on Earth from the sun is ~ 10,000 times the current world energy demand [1]; however this distribution is not uniform due to the curvature of the Earth and the atmosphere. PV technologies with efficiencies as low as 10 % can produce enough electricity to provide 1,000 times the current world demand. Limiting the solar collection to the land area, the potential is still 250 times the current need. Therefore, only 0.4 % of the land area is required to provide the current world energy demands [5].

1.2 Overview on PV Technology

Electromagnetic radiation is converted to electricity by the PV effect, where the sun is the source of radiation and this is explained in more detail in chapter 2. For as long as the sun is shining on the solar cell, electrical power measured in watts (W) will be generated. When the illumination terminates, the electricity generation ends. It is important for the solar cell to have a good efficiency and to perform well over a long period of time under real atmospheric conditions.

Solar cells are useful for both terrestrial and space applications. Solar cells supply power for satellites and play an important role in providing an alternative terrestrial energy source due to their conversion efficiency and ability to provide nearly permanent power at a low operating cost [8]. Table 1-1 lists some general advantages and disadvantages of PV technology.

Table 1-1: Advantages and disadvantages of PV technology [1].

Advantages of PVs	Disadvantages of PVs
Source is widely accessible/infinite	Source is diffuse
No emissions	High initial installation cost
Low operating costs	Unpredictable output
No moving parts (no wear)	Lack of storage
Ambient temperature operation	
High reliability of solar modules	
Modular (small or large increments)	
Easy installation	
Easy integration into new/existing building structures	

Most of the solar modules on the market are made of multi-crystalline silicon (multi-Si) with a market share of 68 % in 2016 [9]. In 2015, all thin film solar cell technologies accounted for 8 % of the total annual production [9]. Even though multi-Si accounts for most of solar panels with efficiency as high as 21 % [10]; thin film technology is promising in being able to reduce costs further. Thin film technology is less developed with efficiencies > 18.6 % [10]. This study will be based on further understanding of this technology.

1.3 Thesis Aim and Contribution to Knowledge

Sodium, an essential dopant impurity in chalcopyrite solar cells, is yet to be fully exploited in cadmium telluride (CdTe) thin film solar cells. This study aims to exploit a gap in the research. In particular, this work seeks to clarify the role of sodium in CdTe thin film solar cell developed in the substrate configuration, where the active layers are deposited on a metal coated substrate. The effect of introducing sodium at different stages during the growth of the structure was investigated, including morphological and crystallographic impact on the CdTe layer and solar devices.

This study also investigated the combination of sodium in conjunction with the CdTe activation step as core novelty in the field: currently, cadmium chloride ($CdCl_2$) is being used as the activation agent for CdTe solar cells. However, due to it being toxic to both the environment and operator during manufacture and its expensive nature some studies have shown that it can be replaced with magnesium chloride ($MgCl_2$). $MgCl_2$ is non-toxic; costs is less than a cent per gram; has shown similar efficiencies to those processed with $CdCl_2$, with similar hole densities in the active layer and comparable impurity profiles for chloride and oxygen [11]. The reason why this chloride was selected compared to other low-cost chlorides is because other chlorides such as NaCl, KCl and $MnCl_2$ lead to introduction of electrically active impurities that compromise the device performance [11].

1.4 Outline and Objectives of the Thesis

Initially the thesis discusses the principles and fundamentals of solar cell technology and materials used (chapter 2). Following this, chapter 3 will focus on the CdTe/CdS multi-crystalline thin film solar cell by reviewing the technologies and properties of the layers. Then the range of experimental techniques used throughout the course of this work is described in detail in chapter 4. The experimental results are then described and analysed in the following three chapters to fulfil the following objectives:

- Study the properties of molybdenum (Mo) films by varying the deposition parameters (chapter 5);
- Investigate the influence of sodium diffusion from soda-lime glass in Mo/CdTe as a function of Mo deposition parameters (chapter 5);
- Examine the role of intentionally added sodium layer (thermally evaporated sodium fluorine) on CdTe absorber layer with and without $CdCl_2$ and $MgCl_2$ treatment (chapter 6);
- Fabricate and characterise devices in substrate configuration by combining sodium and chlorine in MOCVD grown CdTe thin films (chapter 7).

CHAPTER 2

2 Overview of PV Cells

This chapter presents a review of the basic features of the PV effect, ideal *pn* junction cells, their band structure and the description of solar cell parameters. Finally, losses and limitations affecting the solar cell parameters are introduced followed by a brief review of the different types of PV devices.

2.1 Introduction

Semiconductors are commonly characterised by their conductivity types at room temperature, with values ranging between 10^{VI} to $10^{Ä}$ Ωcm [12], and are strongly temperature dependent. Devices based on semiconductors include: PV solar cells, diodes, transistors, switches, detectors, and thermistors.

Solar cells are semiconductor devices that use the PV process to convert solar radiation (photons) into direct current electricity (electrons). The basic structure of a solar cell is a *pn* junction that contains two layers; a *p*-type and an *n*-type material. When illuminated and in the dark, a potential difference is created between the layers by the PV effect. Therefore, a successful solar cell must have three main parts: a semiconductor with strong absorption of incident light, a *pn* junction that separates the electron hole pairs and electrical contacts on either side of the *pn* junction to extract the generated current. Not only is the efficiency of the solar cell important, but also its ability to perform well over a long period under real atmospheric conditions.

The intensity of solar radiation outside the Earth’s atmosphere, at the average distance of its orbit around the sun, is expressed by the solar constant, 1367 W/m^2 [13]. Terrestrially, the sunlight is attenuated by clouds as well as atmospheric scattering and absorption. Since the radiation from the sun is not homogenous, the degree of which the atmosphere attenuates the solar radiation reaching the Earth's surface depends on the length of the light’s path through the atmosphere, or the mass of air through which it passes. A simulated air mass (AM) spectrum is usually used to illuminate the solar cells. Figure 2-1 shows the curves associated with solar spectral irradiance (power per unit area per unit wavelength). The upper curve, which represents the solar spectrum outside the Earth’s atmosphere, is the air mass zero spectrum (AM0). The AM0 spectrum is related to satellite and space vehicle applications and terrestrial solar cell performance is specified with air mass 1.5 spectrum (AM1.5). The AM1.5 spectrum represents the sunlight at the Earth’s surface when the sun is at an angle of 48 ^{o} from the vertical. At an angle of 48 ^{o}, the incident power is about 963 W/m^2 [8].

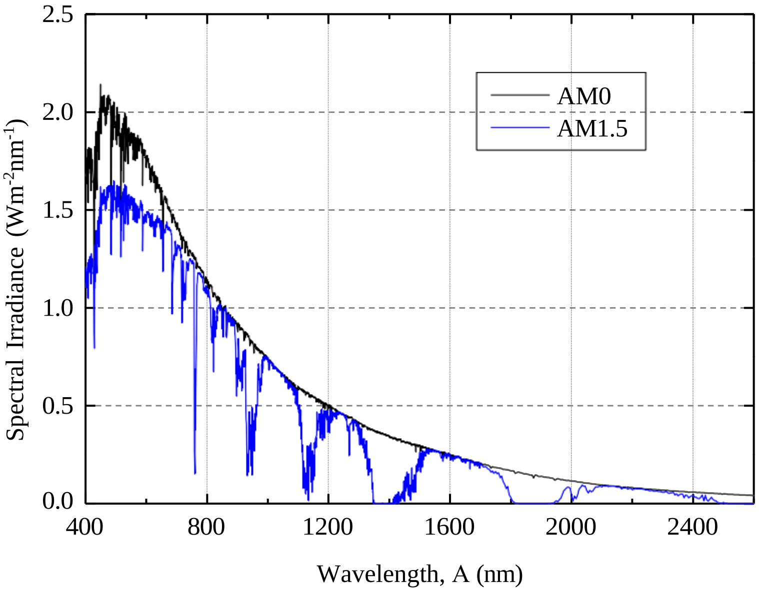

Figure 2-1: AM0 and AM1.5 spectra (reproduced from ASTM G173-03 reference spectra).

Solar cells are fabricated from a range of semiconductor materials based on how their absorption characteristics match the solar spectrum and the fabrication costs; most commonly silicon (Si) – crystalline, multi-crystalline, and amorphous. Solar cells are fabricated from other semiconductor materials such as gallium arsenide (GaAs), indium phosphide (InP), copper indium gallium diselenide ($Cu(InGa)Se_2$, CIGS), and cadmium telluride (CdTe).

To form a *pn* junction for a solar cell, two semiconductors can be of two different compounds (heterojunction) or from the same material but differently doped (homojunction). An example of homojunction is Si as both the *p* and *n* type material is Si doped with impurities; and CdTe/CdS is an example of heterojunction, where CdTe is the *p*-type and CdS is the *n*-type [8]. Understanding the main principal of PVs and the physics behind the PV effect is important to further develop solar cells.

2.2 Fundamental Properties of Semiconductors

The PV effect is the basic process where a solar cell converts sunlight to electricity. Carriers are generated from the interaction of incident photons with the semiconductor need depuration of carriers. Then these carriers are collected to create an electrical current. For the PV process to happen, a photon of energy $E = hv$ (where h is Planck’s constant and v is the photon frequency) must reach the material and enter through the surface. If $hv < L_R$ (where L_R is the energy of the bandgap) then electron-hole pair does not form as the energy provided by the photon is too small to excite an electron from the valence band (VB) to the conduction band (CB) of the semiconductor. However, if the photon provides enough energy ($hv > L_R$), an electron from the VB will be promoted to the CB. When an electron is promoted to a higher energy level, a corresponding hole is created. This results in a flow of electrons from the VB to the CB.

2.2.1 Energy Bands

A semiconductor has a property that the CB is vacant at absolute zero and it is separated by an energy gap from the filled VB (figure 2-2). Therefore, the energy bandgap (L_R) is the difference in energy between CB minimum (known as conduction band edge with energy L_P or CBM) and the VB maximum (known as valence band edge with energy L_T or VBM). The energy bandgap between L_T and L_P is the width of the forbidden energy gap, which is not accessible for free electrons.

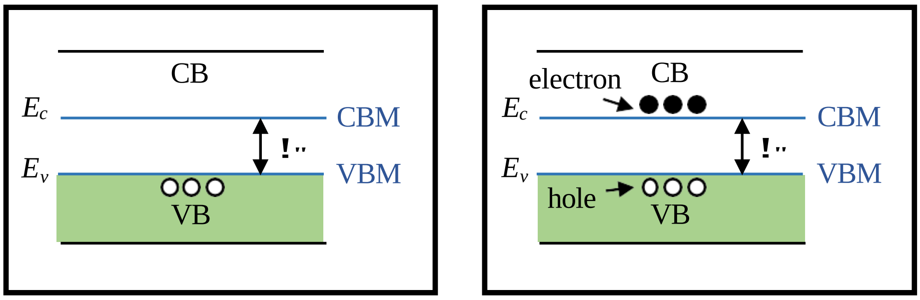

Figure 2-2: Schematic energy band representations of a semiconductor at absolute zero (left), post excitation (right).

Semiconductors are poor conductors at low temperatures. The thermal energy *kT* at room temperature, where Z is Boltzmann's constant and *T* is the temperature in Kelvin, is a fraction of L_R, and a small number of electrons are thermally excited across the L_R to leave positively charged vacancies or holes in the VB. Since there are many empty states in the CB, a small applied potential can easily move these electrons, resulting in a moderate current.

Depending on the position of the CBM and the VBM in the energy momentum diagram, the semiconductors can be divided into two groups: direct or indirect bandgap materials. Figure 2-3 shows the direct and indirect bandgap semiconductors basic photon absorption process.

For the energy-momentum relationship in figure 2-3 a the excitation of an electron from the VB to the CB with the smallest possible energy ($L_R = L_P - L_T$) occurs without change in crystal momentum. Therefore, the CBM and the VBM occur at the same momentum ($p = 0$), this is the characteristic of a direct bandgap semiconductor (*e.g.* GaAs, InP, CIGS and CdTe). On the other hand, for indirect bandgap semiconductors (*e.g.* Si and Ge) excitation from the VBM to the CBM is only possible with a change of crystal momentum (figure 2-3 b). Therefore, the

CBM and the VBM occur at different values of the crystal momentum of the electrons ($p \neq 0$). Notice that in indirect bandgap semiconductors, the light absorption is enabled by either phonon absorption or phonon emission. Phonons are the particle form of lattice vibrations in the semiconductor. Semiconductors are suitable for this process due to their low-energy particles with relatively high momentum (figure 2-3 b).

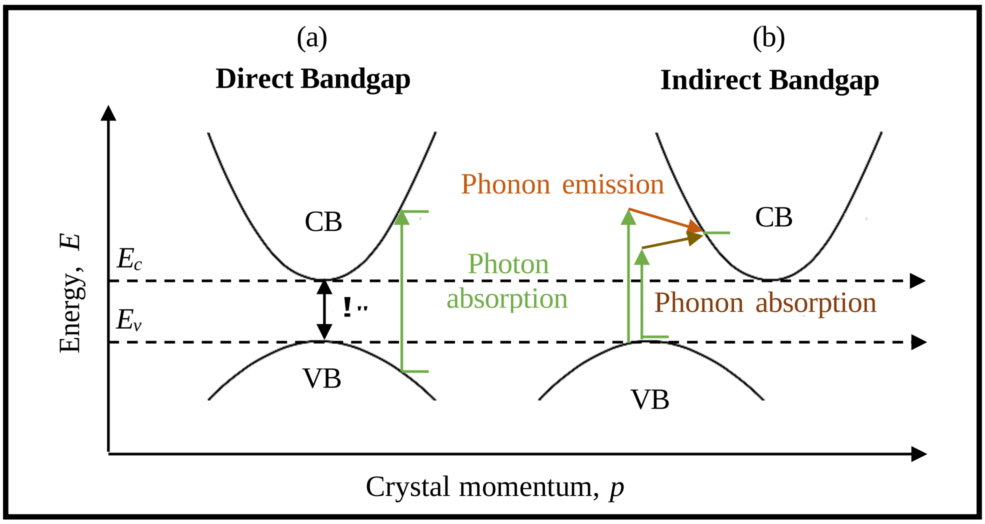

Figure 2-3: A schematic energy-momentum (energy band) diagram showing the photon absorption for a direct and indirect bandgap semiconductor.

2.2.2 Intrinsic Carrier Concentrations

When the semiconductor is in thermal equilibrium condition (at a uniform temperature without any external excitations such as light, pressure, or electric field) the probability that an electron occupies an electronic state with energy E is given by the Fermi–Dirac distribution function, also known as Fermi distribution function [1]:

$$\mathrm{U}\big(\mathrm{L}\big) = \frac{1}{1 + \acute{\mathrm{E}}^{(\tilde{\mathrm{N}}\mathrm{V}\ \tilde{\mathrm{N}}\ddot{\mathrm{o}})}/_{\mathrm{Fq}}} \qquad \textbf{(2-1)}$$

where $\mathrm{L_Q}$ is the energy of the Fermi level, where the probability of occupation by an electron is exactly one-half. The Fermi distribution function is a strong function of temperature as illustrated in figure 2-4, *f* (*E*) is symmetrical around E_F ($E - E_F = 0$). At absolute zero, it is a step function and all the states below E_F are filled with electrons and above E_F are empty. With thermal excitation, some states below E_F will be left empty while corresponding number of states above E_F will be filled with the excited electrons.

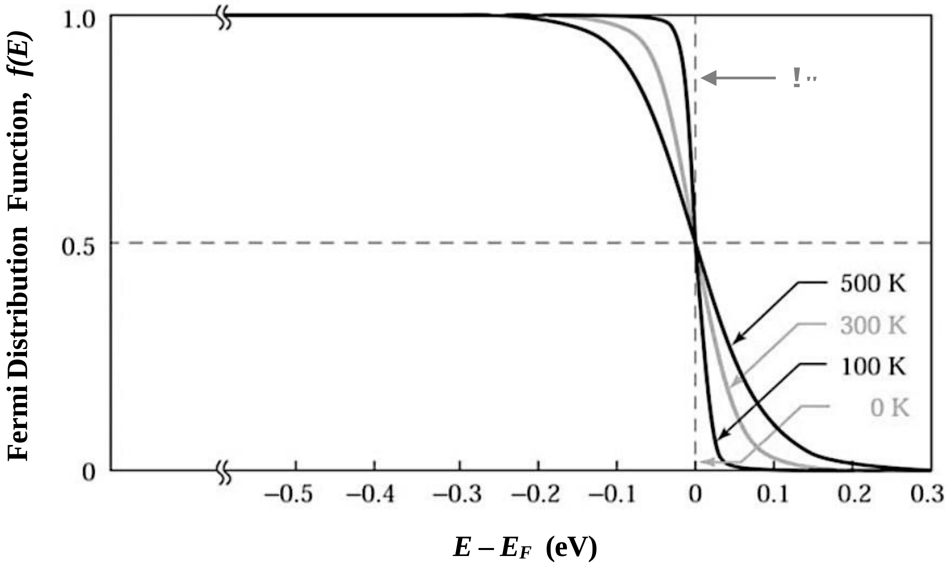

Figure 2-4: Fermi distribution function *f* (*E*) versus (*E* – *E*$_F$) for various temperatures [8]**.**

For energies that are $3kT$ above E_F, the exponential term in equation 2-1 becomes larger than 20 [1]. Therefore, the Fermi distribution function can be approximated by the simpler expression:

$$\text{U}(\text{L}) \cong \text{É}^{(\text{ÑVÑ}_\text{ö})}/_{\text{Fq}} \qquad \text{for} \qquad (E - E_F) > 3kT \qquad \textbf{(2-2)}$$

In an intrinsic semiconductor material, the electron and hole densities, *n* and *p* are equal to the intrinsic carrier density, $\text{d}_\text{S} = \text{d} = \text{f}$, with high dependency on the temperature as shown in the following equations:

$$\text{d} = \mathbf{i}_\text{P} \times \text{U}(\text{L}_\text{P}) = \mathbf{i}_\text{P}\ \text{É}^{\text{V}(\text{Ñ}_\text{á}\text{V}\ \text{Ñ}_\text{à})}/_{\text{Fq}} = \text{d}_\text{S} \qquad \text{for} \quad (\text{L}_\text{P} - \text{L}_\text{S}) > 3kT \qquad \textbf{(2-3)}$$

$$\mathbf{f} = \mathbf{i}_\text{T} \times [1 - \text{U}(\text{L}_\text{T})] = \mathbf{i}_\text{T}\ \text{É}^{\text{V}(\text{Ñ}_\text{à}\text{V}\ \text{Ñ}_\text{â})}/_{\text{Fq}} = \text{d}_\text{S} \quad \text{for} \quad (\text{L}_\text{S} - \text{L}_\text{T}) > 3kT \qquad \textbf{(2-4)}$$

where $\mathbf{i}_\text{P}$ and $\mathbf{i}_\text{T}$ are constants representing the density of states in the CB and VB respectively and L_S is the Fermi level for an intrinsic semiconductor. In an intrinsic semiconductor, L_S can obtained by equating equations 2-3 and 2-4:

$$\text{L}_\text{S} = \frac{\text{L}_\text{P} + \text{L}_\text{T}}{2} + \frac{\text{Zt}}{2} \ln\left(\frac{\mathbf{i}_\text{T}}{\mathbf{i}_\text{P}}\right) \qquad \textbf{(2-5)}$$

At room temperature, the second term is much smaller than L_R ($\text{L}_\text{R} = \text{L}_\text{P} - \text{L}_\text{T}$). Therefore, L_S generally lies very close to the middle of the L_R. Since $\text{fd} = \text{d}^\text{I}{,}_\text{S}$ then:

$$\mathbf{d}_\text{S}^\text{I} = \mathbf{i}_\text{P} \mathbf{i}_\text{T} \text{É}^{\text{Ñ}_\text{ä}}/_{\text{Fq}} \qquad \textbf{(2-6)}$$

2.2.3 Donors and Acceptors

The conductivity of the semiconductor and the number of electrons and holes in their respective bands can be controlled through the introduction of specific impurities, or dopants, called donors and acceptors. For example, when semiconductor Si is doped with phosphorous (P), one electron is donated to the CB for each atom of P presented. P is in column V of the periodic table and therefore it has five valence electrons. Four of these electrons are used to satisfy the four covalent bonds of the Si lattice and the fifth is available to fill an empty state in the CB. If Si is doped with B (valency of three, in column III of periodic table), each B atom accepts an electron from the VB, leaving behind a hole. The impurities introduce additional localized electronic states into the energy band structure between E_c and E_v as shown in figure 2-5. The controlled introduction of donor and acceptor impurities into a semiconductor allows the creation of the *n*-type (donor – figure 2-5 b) and *p*-type (acceptor – figure 2-5 a) semiconductors, respectively. The energy state close to the CBM, E_D, is introduced by a donor atom and is a positively charged ion. Similarly, an acceptor atom introduces a negatively charged ion at energy state close to the VBM, E_A.

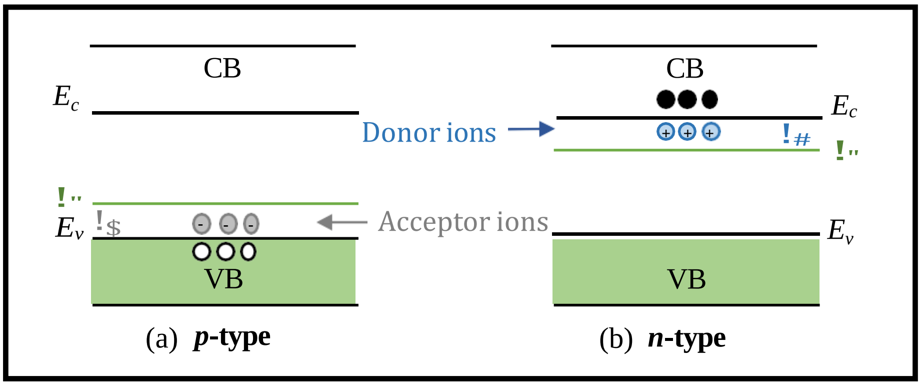

Figure 2-5: Schematic energy band representation of extrinsic doped semiconductor with (a) acceptor ions and (b) donor ions.

If the material is doped with an *n*-type semiconductor with a density N_D of donor atoms such that $N_D \gg n_i$ then at room temperature $n = N_D$. However, since for a semiconductor in equilibrium $pn = n_i^2$, the hole concentration should be $p = n_i^2/N_D$. Thus, in *n*-type semiconductor material $n \gg p$ and electrons are majority carriers while holes are minority carriers. Similarly, for a material doped with *p*-type having a density of N_A of acceptor ions, $p = N_A$ and $n = n_i^2 / N_A$.

Doping shifts the Fermi level away from the centre of the bandgap. Based on equations 2-3 and 2-4 and the relation between *n* and *p* and their densities the following relations can be deducted:

$$n = N_C e^{-(E_C - E_F)/kT} = n_i e^{(E_F - E_i)/kT} \qquad \textbf{(2-7)}$$

$$p = N_V e^{-(E_F - E_V)/kT} = n_i e^{(E_i - E_F)/kT} \qquad \textbf{(2-8)}$$

In both intrinsic and extrinsic semiconductors under thermal equilibrium conductions $n_i^2 = pn$ and this relationship is known as mass action law.

2.2.4 Semiconductor Transport and Recombination

2.2.4.1 Current Density Equations

Electrons and holes will flow under the influence of an electric field (drift current) and a concentration gradient (diffusion current). For a system where *n* and *p* vary only in the *x*-dimension, the total current density at any point is the sum of the drift and diffusion components. Therefore, the electron and hole current densities equations are [8]:

$$J_n = qD_n \frac{dn}{dx} + qn\mu_n E \qquad \textbf{(2-9)}$$

$$J_p = -qD_p \frac{dp}{dx} + qp\mu_p E \qquad \textbf{(2-10)}$$

where *q* is the electric charge, D_n, D_p are diffusion constants for electron and hole, μ_n, μ_p are the respective mobility and E is the electric field in the *x*-direction. A negative sign is used in equation 2-10 as for a positive hole gradient the holes will diffuse in the negative *x*-direction. Sum of equation 2-9 and 2-10 gives the total conduction current density.

A more concise definition of electron and hole currents is through the gradient of the Fermi level, E_{Fn} (for electron) and E_{Fp} (for holes):

$$Y_B = ld\{_B \frac{åL_{QB}}{åw} \tag{2-11}$$

$$Y_D = \mathbf{l}f\{_D \frac{åL_{QD}}{åw} \tag{2-12}$$

which is from the definitions of n, p and the electron and hole current densities above where z is related to the intrinsic Fermi level, E_i:

$$lz = \frac{åL_S}{åw} \tag{2-13}$$

It is important to understand that diffusion and mobility constants are related to each other via Einstein's relation ($\{_{B,D} = \mathbf{lJ}_{B,D} / Zt$) for either carrier.

2.2.4.2 Recombination

Electron-hole pairs are continually created and destroyed in a semiconductor material. At thermal equilibrium ($fd = d_S^I$), the net generation rate, G, and net recombination rate, R, are exactly equal (R = G). When a semiconductor is no longer at thermal equilibrium ($fd \neq d_S^I$), for example by illumination and/or injection of current, the concentrations of electrons and holes tend to relax back toward their equilibrium values by recombination in which an electron falls from the CB to the VB, thus eliminating a VB hole (R $\neq$ G). Several important recombination mechanisms (figure 2-6) for solar cell operation include: non-radiative recombination, radiative recombination, and Auger recombination.

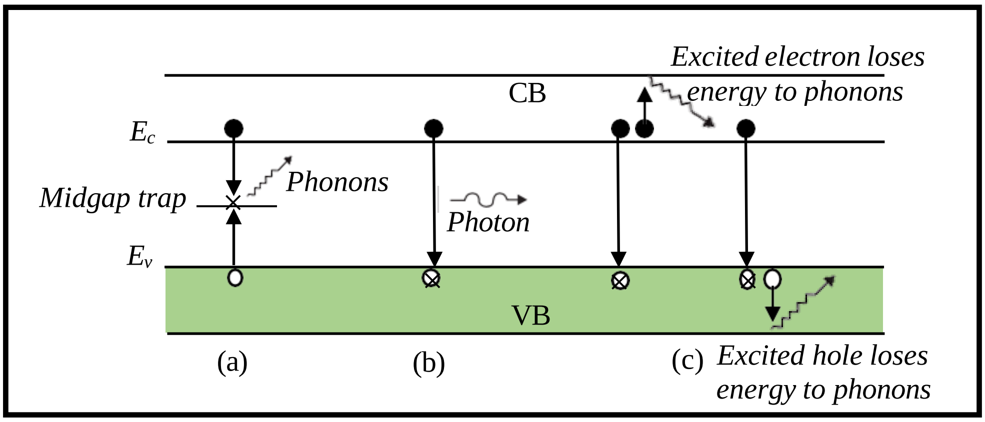

Figure 2-6: Recombination processes in semiconductors (a) non-radiative, (b) radiative and (c) Auger [1]**.**

Non-radiative recombination, the most common form of recombination, occurs through traps (material defects) in the bandgap (forbidden gap). For a single level trap (*SLT*) state in the bandgap, the rate of electron-hole recombination (m_{a_q}) is given by the Shockley-Read-Hall recombination formula [1]:

$$m_{a\_q} = \frac{fd - d_S^I}{\}_B(f + f_h) + \}_D(d + d_h)} \qquad \textbf{(2-14)}$$

where $\}_B$, $\}_D$ are the lifetime for the excess minority carriers of electrons and holes respectively, and d_h, f_h are the densities of the available trap states at equilibrium. In the case where one carrier concentration greatly exceeds the other, the net recombination rate becomes proportional to the excess minority carrier concentration:

$$m_{a\_q} \approx \frac{\Delta B}{\hat{e}_{\ddot{e}}} \qquad \text{for minority of electrons, where } \Delta d = d - d_g \qquad \textbf{(2-15)}$$

$$m_{a\_q} \approx \frac{\Delta D}{\hat{e}_{\acute{\imath}}} \qquad \text{for minority of holes, where } \Delta f = f - f_g \qquad \textbf{(2-16)}$$

Radiative (band-to-band) recombination, $m_{\grave{\imath}}$, is simply the opposite of the optical generation process and is much more efficient in direct bandgap semiconductors. During radiative recombination, the energy of the electron is given to an emitted photon. The net recombination rate due to radiative processes is:

$$m_{\grave{\imath}} = \hat{\imath}(fd - d_{\S}^{I}) \qquad (\hat{\imath} \text{ is a constant}) \qquad \textbf{(2-17)}$$

Auger recombination, m_{NnRop}, is similar to radiative recombination, except that the energy of transition is given to another carrier (in either the CB or the VB). The electron or hole then relaxes thermally by emitting its excess energy and momentum to a phonon. This recombination is the opposite of impact ionization, where an energetic electron collides with a crystal atom created an electron-hole pair by breaking the bond. The net recombination rate due to Auger processes is:

$$m_{NnRop} = (A_B d + A_D f)(fd - d_{\S}^{I}) \quad (A_B \text{and } A_D \text{are comparable constants}) \qquad \textbf{(2-18)}$$

2.3 The *pn* Junction of Solar Cells

Figure 2-7 illustrates the *p* and *n* type regions of a semiconductor materials that are uniformly doped and physically separated before the junction formation. Notice that the Fermi level, E_F, is near the VB edge and near the CB edge in the *p* and *n*-type material, respectively. Where an *n*-type semiconductor encounters a *p*-type semiconductor, a *pn* junction is formed as illustrated in figure 2-8.

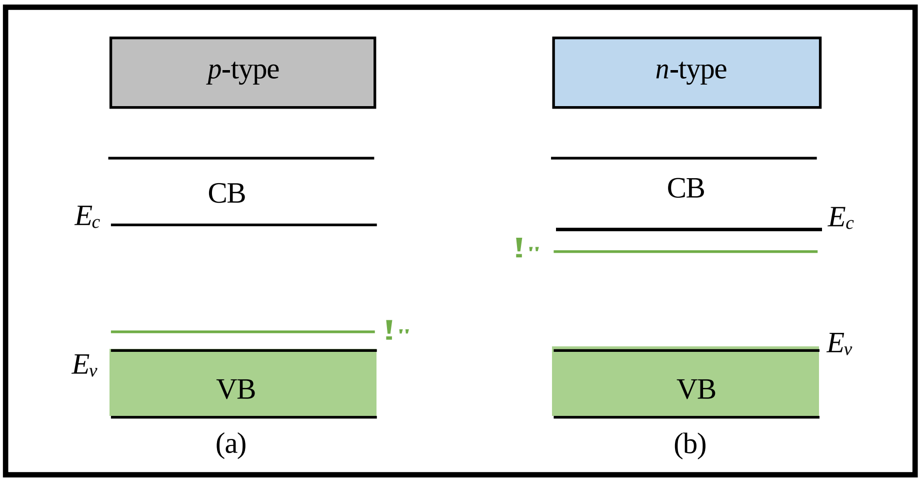

Figure 2-7: Uniformly doped (a) *p*-type and (b) *n*-type semiconductor materials before the junction formation.

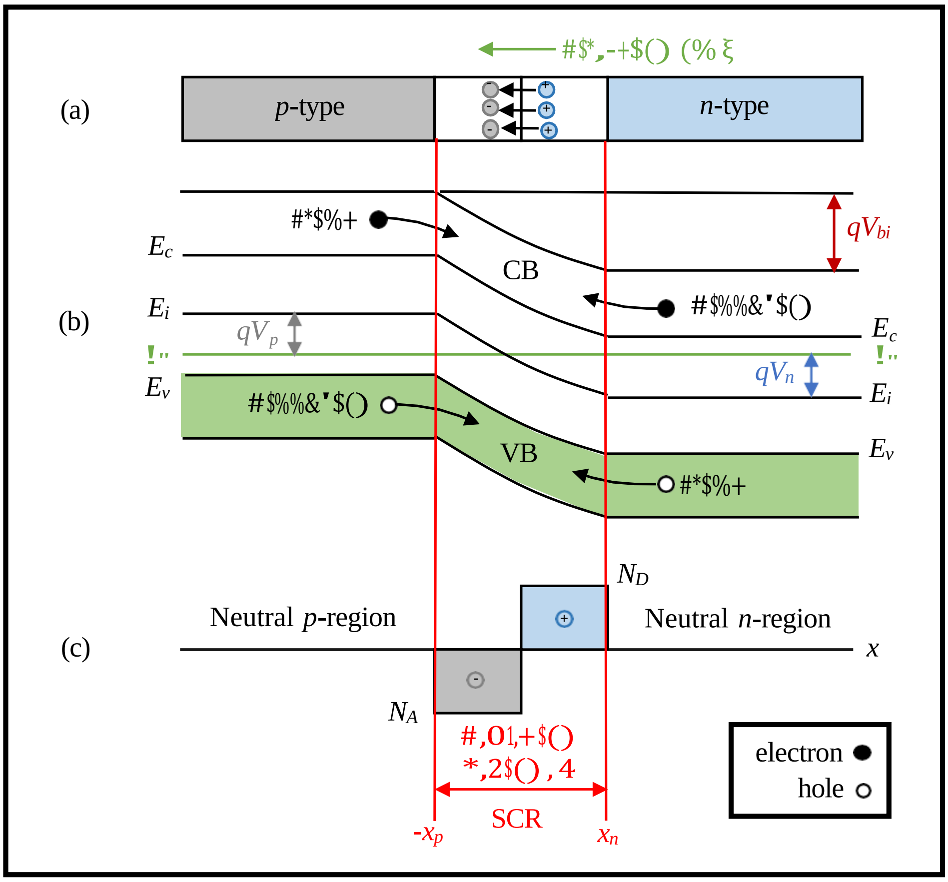

Figure 2-8: (a) Schematic of a *pn* junction at thermal equilibrium, (b) energy band diagram of abrupt *pn* junction at thermal equilibrium and (c) rectangular approximation of the space charge distribution of a *pn* junction at thermal equilibrium.

2.3.1 Formation of *pn* Junction at Thermal Equilibrium Conditions

When the *p*-type and *n*-type semiconductors are joined together, the large carrier concentration gradients at the junction causes carrier diffusion. Under thermal equilibrium conditions, the net current flow is zero and E_F should be independent of position. An electric field is directed from the positive (*n*-side) to the negative (*p*-side) charge, as indicated in figure 2-8 a. Due to holes and electrons concentration difference, the holes diffuse from the *p*-type region into the *n*-type region and, similarly, electrons diffuse from the *n*-type material into the *p*-type region (figure 2-8 b). As the carriers diffuse, the charged impurities (N_A^- in the *p*-type and N_D^+ in the *n*-type) are exposed and they are no longer screened by the majority carrier. Under thermal equilibrium conditions, the steady state condition at a given temperature with no external excitations, the diffusion and drift currents flowing across the junctions are balanced, therefore the net current flow is zero. The transition region between the *n* and *p* type semiconductor materials are known as the space-charge region (SCR) or depletion region (*W*), since it is effectively depleted of both holes and electrons (figure 2-8 c).

The energy difference between E_F and E_i away from the junction in the *p* and *n* side as shown in figure 2-8 b is [1]:

$$\mathrm{lu}_{\mathrm{B}} = \mathrm{L}_{\mathrm{Q}} - \mathrm{L}_{\mathrm{S}} \qquad \textbf{(2-19)}$$

$$\mathbf{l}\,\mathrm{u}_{\mathrm{D}} = \mathrm{L}_{\mathrm{S}} - \mathrm{L}_{\mathrm{Q}} \qquad \textbf{(2-20)}$$

Substituting equations 2-7 and 2-8 in to 2-19 and 2-20 respectively while assuming complete ionisation ($\mathrm{d} = \mathbf{i}_{\mathrm{O}}, \mathbf{f} = \mathbf{i}_{\mathrm{N}}$) then:

$$\mathbf{l}\mathrm{u}_{B} = \mathrm{Zt}\ln\left(\frac{\mathbf{i}_{O}}{\mathrm{d}_{S}}\right) \tag{2-21}$$

$$\mathbf{l}\mathrm{u}_{D} = \mathrm{Zt}\ln\left(\frac{\mathbf{i}_{N}}{\mathrm{d}_{S}}\right) \tag{2-22}$$

The electrostatic potential difference resulting from the junction formation is called the built-in voltage, u_{MS}. It originates from the electric field (z) created by the contact of the positive and negative charges in the depletion region. Therefore, addition of equation 2-21 and 2-22 gives [1]:

$$\mathbf{l}\mathrm{u}_{MS} = \mathrm{Zt}\ln\left(\frac{\mathbf{i}_{N}\,\mathbf{i}_{O}}{\mathrm{d}_{S}{}^{\mathbf{I}}}\right) \tag{2-23}$$

The overall space charge neutrality of the semiconductor requires that the total negative charge per unit area in the *p*-side is equal to the total positive charge per unit area in the *n*-side, therefore:

$$\mathrm{w}_{D}\,\mathbf{i}_{N} = \mathrm{w}_{B}\,\mathbf{i}_{O} \tag{2-24}$$

where $\mathrm{w}_{D}$and w_{B} are the extent of depletion region penetrating in the *p* and *n* type, respectively (figure 2-8 c). The total depletion region width, *W*, as a function of u_{MS} is given by [1]:

$$\grave{\mathbf{o}} = \mathrm{w}_{D} + \mathrm{w}_{B} = \sqrt{\frac{2\hat{\mathrm{o}}_{a}}{\mathbf{l}}\left(\frac{\mathbf{i}_{N}+\mathbf{i}_{O}}{\mathbf{i}_{N}\,\mathbf{i}_{O}}\right)\mathrm{u}_{MS}} \tag{2-25}$$

where $\hat{\mathrm{o}}_{a}$ is the semiconductor permittivity. It is clear from equation 2-25 that *W* strongly depends on the doping concentrations of both *p* and *n* side. Therefore, when the impurity concentration on a side of an abrupt junction is much larger than the other side, a one-sided abrupt junction is produced. For example, when the depletion layer width of the *p*-side is much smaller than that of *n*-side ($\mathbf{i}_N \gg \mathbf{i}_O$), then equation 2-25 can be simplified to:

$$\grave{o} \cong w_B = \sqrt{\frac{2\hat{o}_a u_{MS}}{\mathbf{l}\,\mathbf{i}_O}} \qquad \textbf{(2-26)}$$

As shown in figure 2-8 c the potential energy difference from the *p* to *n* side is $\mathbf{l}u_{MS}$. If a positive voltage u_Q is applied to the *p*-side with respect to the *n*-side, the *pn* junction becomes forward-biased and the total electrostatic potential across the junction decreases by u_Q. Therefore, the forward-bias reduces the depletion region width and u_{MS} is replaced with $u_{MS} - u_Q$. In contrast, if a positive voltage $u_ö$ is applied to the *n*-side with respect to the *p*-side the *pn* junction becomes reverse-biased and the total electrostatic potential across the junction increases by $u_ö$. Therefore, the reverse-bias increases the depletion region width and u_{MS} is replaced with $u_{MS} + u_ö$. Thus, for one-sided abrupt junction, *W* as a function of u_{MS} is given by [1]:

$$\grave{o} = \sqrt{\frac{2\hat{o}_a(u_{MS} - u)}{\mathbf{l}\,\mathbf{i}_j}} \qquad \textbf{(2-27)}$$

where $\mathbf{i}_j$ is the doping concentration of the lightly doped material, u is positive for forward-bias and negative for reverse-bias.

2.3.2 Heterojunction

A heterojunction is defined as a junction formed between two dissimilar semiconductors, in contrast to a homojunction. In a heterojunction, the following parameters for the two semiconductors are expected to be different: energy bandgaps, E_g, dielectric permittivity's, ε_s, work functions $\sim$, and electron affinities χ.

Figure 2-9 a illustrates the energy band diagram of two isolated semiconductor materials before heterojunction formation. Work function (~) is the energy required to remove an electron from the E_F to the vacuum level. The electron affinity (χ) is the energy required to remove an electron from the bottom of the CB (E_c) to the vacuum level. The difference in energy of the CB edges in the two semiconductors is ΔE_c, similarly, the difference in energy of the VB edges is ΔE_v.

Figure 2-9 b illustrates the energy band diagram of an *pn* heterojunction under thermal equilibrium conditions. In this case, it is assumed that the two materials have similar lattice constants as lattice mismatch causes traps at the interface of the two semiconductors. Therefore, when these two dissimilar semiconductors with different E_g and χ are in contact the charge is transferred until LQD = LQB = LQ as shown in figure 2-9.

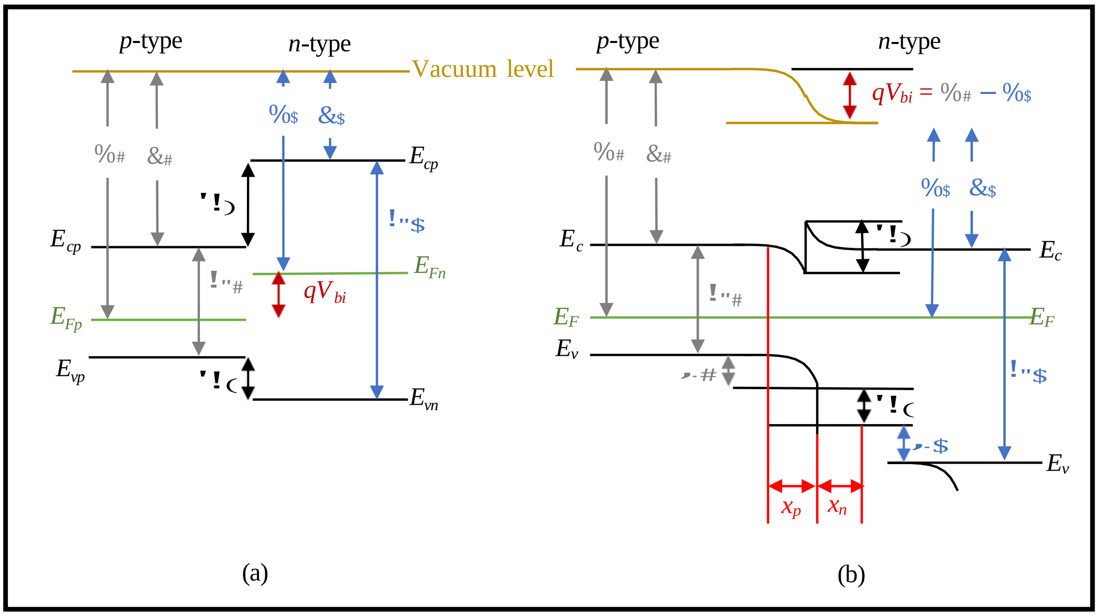

Figure 2-9: Electron energy band diagram of (a) two isolated semiconductors and (b) an *pn* heterojunction under thermal equilibrium condition.

The total built-in potential, u_{MS}, of a heterojunction is the sum of the electrostatic potentials of both *p* and *n* side ($u_{MS} = u_{MD} + u_{MB}$). Thus, when a bias is applied to the heterojunction, the total depletion region width is [1]:

$$ò = w_D + w_B = \sqrt{\frac{2ô_Bô_D(i_N + i_O)(u_{MS} - u)}{l\, i_N i_O(ô_B i_O + ô_D i_N)}} \qquad \textbf{(2-28)}$$

2.3.3 Schottky Junction

In addition to the *pn* junction formed between the two semiconductors, metal contacts are necessary to collect photo-generated carriers at the front and rear surface of a solar cell. The potential barrier, which forms when a metal is in contact with a semiconductor, arises from the separation of charges at the metal semiconductor interface. Figure 2-10 illustrates the energy bandgap diagrams for the barrier formation process. Figure 2-10 a shows the electron energy band diagram of a metal and an *n*-type semiconductor having a work function of ~ and $\sim_{r}$, respectively, and $õ_{r}$ is the electron affinity of the *n*-type semiconductor.

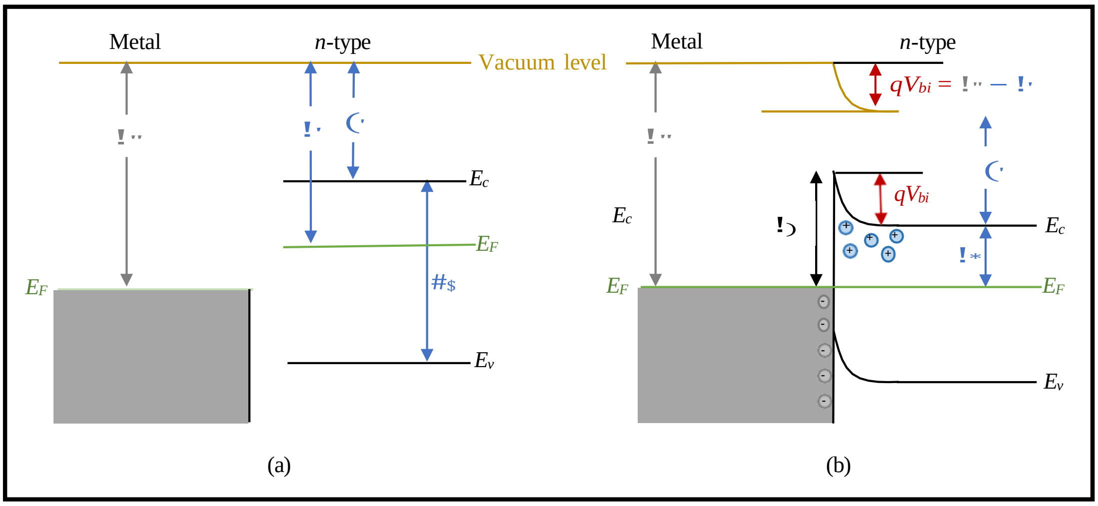

Figure 2-10: Electron energy band diagram of a metal contact to an *n*-type semiconductor with $ú_{ù} > ú_{û}$. (a) Neutral materials isolated from each other and (b) Schottky junction at thermal equilibrium.

Figure 2-10 b shows the energy band diagram of the metal and the *n*-type semiconductor after the contact is made and thermal equilibrium has been reached. When the two materials come into direct contact, electrons from the CB of the *n*-type semiconductor with higher energy than that of the metal, flow into the metal until the L_{Q} on both sides is brought into coincidence. As the electrons move out of the *n*-type semiconductor into the metal, the free electron concentration in the *n*-type region near the boundary reduces. Since the separation between the L_{P} edge and the L_{Q} of the *n*-type semiconductor increases with decreasing electron concentration, the L_{P} edge bends up as illustrated in figure 2-10 b. The CB electrons that cross over into the metal leave positive charges (ionised donors), so the *n*-type region near the metal becomes depleted of mobile electrons. Therefore, a positive charge is established on the *n*-side of the interface and the electrons that cross over into the metal form a thin layer of negative charges (figure 2-10 b). Accordingly, an electric field is established from the *n*-type semiconductor to the metal. The amount of band bending is equal to the difference between the two vacuum levels:

$$1u_{MS} = \sim\grave{} - \sim_{r} \qquad \textbf{(2-29)}$$

where u_{MS} is the built-in potential of the junction and $1u_{MS}$ is the potential barrier where an electron, moving from the *n*-type semiconductor into the metal, must overcome. However, the barrier looking from the metal towards the semiconductor is different and is given by:

$$\sim_{j} = \sim\grave{} - \tilde{o}_{r} = 1u_{MS} + \sim_{B} \qquad \textbf{(2-30)}$$

where $\sim_{B} = L_{P} - L_{Q}$ represents the depth of L_{Q} in the bandgap of the *n*-type semiconductor.

2.4 Electrical Characteristics of Solar Cells

A voltage applied to a *pn* junction will disturb the balance between the diffusion and drift currents of electrons and holes. Due to the depletion region and built-in voltage, a *pn* junction only allows current to flow in one direction when a bias is applied. As described earlier, in forward bias, the applied voltage reduces the electrostatic potential across the depletion region and in reverse bias, the applied voltage increases the electrostatic potential across the depletion region.

2.4.1 Ideal Characteristics

When in dark, a solar cell has the same current–voltage (*I*–*V*) characteristic as a diode. To derive the ideal *I*–*V* characteristics, it is assumed that the doped regions are doped uniformly and have abrupt boundaries, and low-injection so that the injected minority carrier concentration is small compared to the majority carrier concentration. Under thermal equilibrium conditions, the majority carrier density in the neutral regions is equal to the doping concentration. The thermal equilibrium condition is specified by the *o* subscript. Hence, n_{po} and n_{no} are the equilibrium electron densities in the *p* and *n* sides, respectively. Therefore, the expression for $\mathbf{1}u_{MS}$ in equation 2-23 can be rewritten as (using the mass action law, $d_{Dg}f_{Dg} = d_S{}^{I}$) [1]:

$$\mathbf{1}u_{MS} = \mathrm{Zt}\ln\left(\frac{f_{Dg}d_{Bg}}{d_S{}^{I}}\right) = \mathrm{Zt}\ln\left(\frac{f_{Dg}d_{Bg}}{d_{Dg}f_{Dg}}\right) = \mathrm{Zt}\ln\left(\frac{d_{Bg}}{d_{Dg}}\right) \qquad \textbf{(2-31)}$$

Rearranging equation 2-31 yields:

$$d_{Bg} = d_{Dg}\text{É}^{\text{ü†°à}}/_{\text{Fq}} \qquad \textbf{(2-32)}$$

$$f_{Dg} = f_{Bg}\,\text{É}^{\text{ü†°à}}/_{\text{Fq}} \qquad \textbf{(2-33)}$$

From equations 2-32 and 2-33, it can be deduced that the electron densities at the two depletion region boundaries are related by u_{MS}. When a bias is applied then equation 2-32 becomes:

$$d_B = d_D\text{É}^{\text{ü(†°àV†)}}/_{\text{Fq}} \qquad \textbf{2-34)}$$

where n_n and n_p are the nonequilibrium densities of the electrons at the boundaries of the depletion region in the *n* and *p* side, respectively, with *V* positive for forward bias and negative for reverse bias. In low-injection condition, the injected minority carrier density is much smaller than the majority carrier density; thus, $d_B \cong d_{Bg}$. The electron density at the *p*-side boundary $(w = -w_D)$ and hole density at the *n*-side boundary $(w = w_B)$ of the depletion region can be obtained using this relation and equation 2-32 and 2-33 respectively, so that:

$$d_D(w = -w_D) = d_{Dg}\,\text{É}^{\text{üt}/\text{Fq}} \tag{2-35}$$

$$\mathbf{f}_B(w = w_B) = f_{Bg}\,\text{É}^{\text{üt}/\text{Fq}} \tag{2-36}$$

Due to the earlier assumptions, no current is created in the depletion region and all the currents come from the neutral region. Therefore, in the neutral *n*-region, the steady-state continuity equation becomes:

$$\frac{\text{å}^{\text{I}} f_B}{\text{å}w^{\text{I}}} - \frac{f_B - f_{Bg}}{\mathbf{J}_D\}_D} = 0 \tag{2-37}$$

Using the general solution from equation 2-37, boundary conditions in equation 2-36 and $\mathbf{f}_B(w = \infty) = f_{Bg}$ the expression below is generated:

$$f_B(w) - f_{Bg} = f_{Bg}\left(\text{É}^{\frac{\text{üt}}{\text{Fq}}} - 1\right)\left(\text{É}^{\frac{V(\text{£}V\text{£}_{\text{ë}})}{-\text{í}}}\right) \tag{2-38}$$

where the hole diffusion length, e_D, is equal to $\sqrt{\mathbf{J}_D\}_D}$. The hole diffusion current density, $Y_D(w = w_B)$ is then:

$$Y_D(w = w_B) = -\mathbf{l}\mathbf{J}_D\frac{\text{å}f_B}{\text{å}w} = \frac{\mathbf{l}\mathbf{J}_D\mathbf{f}_{Bg}}{e_D}\left(\text{É}^{\frac{\text{üt}}{\text{Fq}}} - 1\right) \tag{2-39}$$

Similarly, the following is obtained from the neutral *p*-region:

$$\text{d}_{\text{D}}(\text{w}) - \text{d}_{\text{Dg}} = \text{d}_{\text{Dg}}\left(\text{É}^{\frac{\text{ü†}}{\text{Fq}}} - 1\right)\left(\text{É}^{\frac{\text{£§£ë}}{\text{–ë}}}\right) \qquad \textbf{(2-40)}$$

$$\text{Y}_{\text{B}}(\text{w} = -\text{w}_{\text{D}}) = -\mathbf{lJ}_{\text{B}}\frac{\text{åd}_{\text{D}}}{\text{åw}} = \frac{\mathbf{lJ}_{\text{B}}\text{d}_{\text{Dg}}}{\text{e}_{\text{B}}}\left(\text{É}^{\frac{\text{ü†}}{\text{Fq}}} - 1\right) \qquad \textbf{(2-41)}$$

where the electron diffusion length, e_{B}, is equal to $\sqrt{\mathbf{J}_{\text{B}}\}_{\text{B}}}$.

The total current density is constant throughout the diode and it is the sum of the current densities in equation 2-39 and 2-41. The sum shown in equation 2-42 is the ideal diode equation (or Shockley equation):

$$\text{Y} = \text{Y}_{\text{D}}(\text{w} = \text{w}_{\text{B}}) + \text{Y}_{\text{B}}(\text{w} = -\text{w}_{\text{D}}) = \text{Y}_{\text{g}}\left(\text{É}^{\frac{\text{ü†}}{\text{Fq}}} - 1\right) \qquad \textbf{(2-42)}$$

where Y_{g} is the reverse saturation current density equal to $\frac{\text{ü0}_{\text{í}}\text{D}_{\text{ë}}\bullet}{\text{–í}} + \frac{\text{üO}_{\text{ë}}\text{B}_{\text{í}}\bullet}{\text{–ë}}$. Y_{D} will increase exponentially when a forward-bias is applied on the *p*-side, and saturates at Y_{g} in the reverse direction. Y_{g} is a measure of the recombination rate in a diode, where a larger Y_{g} relates to a higher recombination rate.

2.4.2 Current Density–Voltage Characteristics

When illuminated, the solar cell generates electron-hole pairs. In the dark, the expression for an ideal diode was given in equation 2-42; however, under illumination the current density–voltage curve (Y–*V*) of the solar cell shifts downward as the light generated current opposes the diode dark current, therefore Y becomes:

$$Y = Y_g\left[É^{\left(\frac{üt}{NFq}\right)} - 1\right] - Y\_ \qquad \textbf{(2-43)}$$

where Y_ is the light generated current density and *A* is the diode ideality (quality) factor and it normally has a value 1 < *A* < 2, with *A* ≈ 1 for diode dominated by recombination in the quasi-neutral regions and *A* ≈ 2 when recombination in the depletion region dominates. The ideal characteristics of a solar cell operating under illumination and in the dark, are shown in figure 2-11.

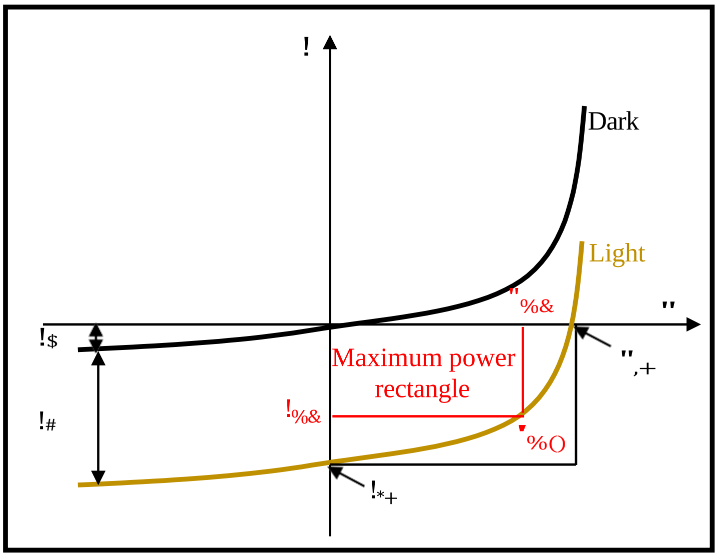

Figure 2-11: Current density–voltage characteristic of a solar cell under illumination and in the dark.

The key performance characteristics of a solar cell are short circuit current density (Yab), open circuit voltage (uvb), fill factor (HH) and device efficiency (*ρι).* The cell reaches its maximum operating point at the maximum power (*mp*), which occurs at u`D and Y`D (figure 2-11).

The short circuit current density, Yab , is the current density measured when no bias is applied to the device and in an ideal case is equal to Y_ .

The open circuit voltage, u_{vb} , is the applied voltage at which no current is flowing through the junction. In an ideal case the u_{vb} is measured when the total current is zero and is calculated using:

$$u_{vb} = \frac{]Zt}{l} \ln\left(\frac{Y\_}{Y_g} + 1\right) \tag{2-44}$$

The fill factor, HH, is the ratio of power available at maximum point against u_{vb} and Y_{ab} , therefore:

$$HH = \frac{\text{¶`ß£}}{u_{vb} \times Y_{ab}} = \frac{\text{u`}_{D} \times \text{Y`}_{D}}{u_{vb} \times Y_{ab}} \tag{2-45}$$

where u`}_{D}$ and $\text{Y`_{D} are the voltage and current density at the maximum output power, ¶`ß£, of the solar cell. HH is a measure of the "squareness" of the *J–V* curve (figure 2-11).

Finally, the performance of the device is obtained using these parameters. The efficiency of the device, ®, is the number of photons converted into electrical power and is calculated using:

$$\text{®}(\%) = \frac{\text{¶`ß£}}{\text{¶}_{SB}} = \frac{Y_{ab} \times u_{vb} \times HH}{\text{]™Éx ´U } sh\text{É KÉ[[} \times \text{¨dK¨åÉds [¨k}hs\text{ f′}\neq\text{É™ åÉd@¨sÆ}} \tag{2-46}$$

2.5 Limitations to Solar Cell Efficiency

2.5.1 Material Limitations

Requirements for maximum solar cell efficiency include: optimum bandgap, complete absorption of photons above the bandgap, perfect separation at the junction, high built-in voltage, lossless transport to the contacts and no electrical losses. These requirements can be achieved by: selecting the material, minimising reflection, increasing film thickness, increasing diffusion length, reducing density of traps and impurities, improving surface quality, increasing contact area, and increasing doping level in the front contact. However, for real materials different parameters cannot always be separately optimised. For instance, a strong optical absorption would likely mean a high recombination [14].

In 1960, Shockley and Queisser published an article [15] presenting the generation due to light absorption has a detailed balance equivalent, which is the radiative recombination (section 2.2.4.2). This Shockley and Queisser efficiency limit occurs in ideal solar cells which are prototypes of current solar cells. Such cells (figure 2-8 b) are made up of a semiconductor with a VB and a CB, which has more energy and is separated from the VB by the bandgap, LR.

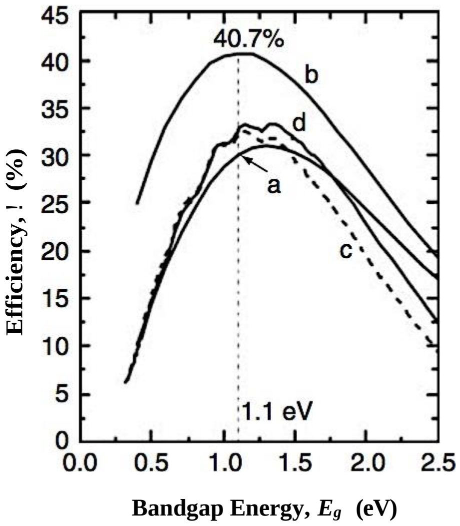

Figure 2-12: Shockley and Queisser efficiency limit for an ideal solar cell versus Ø∞ for (a) unconcentrated black body radiation (1596 W/m^2), (b) full concentrated black body radiation (7349 × 104 W/m^2), (c) unconcentrated AM1.5-Direct (767 W/m^2) and (d) AM1.5-global (963 W/m^2) [1].

2.5.2 Parasitic Resistances

In the case of an ideal solar cell discussed in section 2.4, parasitic resistances (m_r and m_{rE} shown in figure 2-13) are always present in real solar cells and cause power loss, therefore they cannot be disregarded.

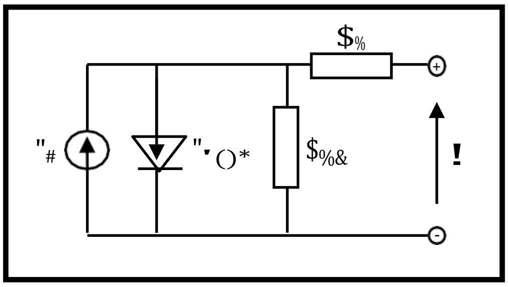

Figure 2-13: Equivalent circuit of an ideal solar cell with inclusion of main parasitic losses represented by series resistance R_s and R_{sh}.

Series resistance, m_r, develops due to both the resistance of the semiconductor bulk and contact resistance to the semiconductor to complete the circuit. Shunt resistance, m_{rE}, develops from either the surface and bulk defects of the solar cell or leakage currents paths for the light generated current. The HH is strongly affected by these parasitic resistances due to their influence on Y_{ab} and u_{vb} ; when m_r and m_{rE} are introduced, equation 2-43 will be modified to describe a real solar cell:

$$Y = Y_g\left[\acute{E}^{\left(\frac{\underline{\text{ü(†V≤ö≥)}}}{NFq}\right)} - 1\right] + \frac{u - Ym_r}{m_{rE}} - Y_{\_} \qquad \textbf{(2-47)}$$

Therefore, m_r should be as low and m_{rE} as high as possible to avoid reducing the overall performance of the device. The detailed m_r and m_{rE} experimental determination from the *J–V* curve is explained in chapter 5.

2.5.3 Optical Losses

Another method of measuring the performance of a solar cell is by measuring its quantum efficiency. This means viewing the spectral response (*SR*) of the solar cell by measuring the efficiency over a range of wavelengths. External quantum efficiency (L¥L) is the probability that a photon at a given wavelength will cause electron generation for the photocurrent of the solar cell. Therefore, this shows the effectiveness of a real solar cell to produce an electronic charge from electromagnetic radiation with varying wavelengths. At a certain wavelength, the L¥L is given by:

$$\text{L¥L}\,(!) = \frac{h\mathrm{K} \times \mu\mathrm{m}(\mathbf{!})}{\mathbf{1!}} \qquad \textbf{(2-48)}$$

where λ is the electromagnetic wavelength, h is the Plank's constant, c is the speed of light, q is the unit charge and μm (!) is spectral response of the solar cell.

Under ideal conditions, a photon at a given wavelength will cause electron excitation for the photocurrent of the solar cell, however due to optical losses in the case of a real solar cell this is not very effective. L¥L is commonly used to describe the different types of losses responsible for a reduction in the measured Y_{ab} . Some types of optical losses include [16, 17]: shading from the collection grid (substrate configuration); reflections from the front contact and interfaces between different constituent layers; absorption losses in the front contact layer and window layer; incomplete collection of photo-generated carriers and incomplete absorption in the absorber layer near the absorber bandgap.

2.6 Types of Photovoltaic Devices

In 1839, the PV effect was first discovered by Becquerel [18] by converting light into electrical potential differences. However, it was not until 1883 that the first functional, intentionally made PV device was produced [19]. The modern era of PV did not start until 1954 when researchers at Bell laboratories accidentally learnt that *pn* junction diodes generated a voltage when illuminated. They then produced a Si *pn* junction solar cell with efficiency of 6 % [20]. By the 1960s, numerous key papers by Prince [21], Loferski [22], Rappaport and Wysocki [23], Shockley and Queisser [15], established the fundamentals of *pn* junction solar cell operation, as well as the theoretical relation between bandgap, incident spectrum, temperature, thermodynamics, and efficiency. Until the early 1970s, cost was of little concern due to huge space program budgets. However, in the 1980s, the industry began to mature, as emphasis on manufacturing and costs grew.

In the last two decades the PV market, has had a huge growth. At present, solar cells can be single junction devices or multi-junction structures and new technologies are employed for making solar cells. Even though organic cells with efficiencies of 11.2 % are reported [10] the best efficient devices are produced using inorganic materials and they are briefly described in this section.

2.6.1 Single Crystal and Multi-Crystalline Silicon

Si is still the most popular solar cell material for commercial application because it is so readily abundant [24]. In 2015, Si-wafer PV technology accounted for ~ 93 % of the total production [9]. The source material for extraction of Si is silicon dioxide (SiO_2), the major constituent of sand.

The material usage for Si cells have reduced considerably during the last decade from ~16 g/Wp to less than 6 g/Wp because of thinner wafers and improved efficiencies [9]. Single crystal silicon devices have efficiency up to 26 % [10]. The major disadvantages of single crystal Si solar cells are the requirements of high grade material and the problems associated with producing single crystals over large areas. Recently creative attempts to make single crystal ribbon Si accounts for 10 % of the world PV total and it is lower in cost than high quality single crystals [25].

In contrast to single crystal Si, the production of multi-crystalline Si cell is more cost effective, where Si is poured into blocks that are subsequently sawn into plates. However, it has the disadvantage that large grain sizes are required to reduce the negative influence caused by grain boundaries. Since, multi-crystalline Si is much cheaper than single crystal Si, researchers are working on new creative ways of minimizing the effects of grain boundaries.

2.6.2 Group III–V Technologies

PV technologies based on group III and V elements of the periodic table have very high efficiencies under either normal or concentrated sunlight. Even though they are costly, their cost can be compensated by using concentrator systems to increase the energy conversion efficiency under high illumination [27, 28]. The most important solar cells in this category are those based on GaAs and InP.

GaAs is a compound semiconductor for which the use in solar cells has been developed synergistically with its use in light emitting diodes, lasers, and other optical devices. Since GaAs is very resistant to radiation and has a high efficiency of 28.8 % [10] (most efficient single junction solar cell up to date) it is very suitable for space applications. The greatest disadvantage of GaAs solar cells is the high cost of single crystalline GaAs substrates. Therefore, the cells are mostly used in concentrator systems. Other disadvantages of GaAs include: availability of Ga and the toxic nature of As.

Due to unavailability of high quality single crystals of *p*-type InP, research on this type of solar cell did not start until early 1970s. The most efficient InP crystalline cell has an efficiency of 22.1 % [10]. A multi-junction InGaP/GaAs/InGaAs device with efficiency of 37.9 % has also been achieved [10]. However, this technology has major limitations, being expensive, having limited resources for In and requiring purification of P.

2.6.3 Thin Film Solar Cell

Even though high purity single crystalline Si and GaAs semiconductors produce high efficiency solar cells; the materials are expensive. An alternative is to use lower purity materials in the form of thin films a few microns thick. Due to this reason, thin film materials have been the subject of intensive research. In 2015, the market share of all thin film PV technologies amounted to ~ 8 % of the total annual production [9]. Three main types of materials have emerged as the most promising candidates for the next generation of solar cells. These are hydrogenated amorphous silicon (a-Si:H), copper indium diselenide ($CuInSe_2$, CIS) and CdTe.

Amorphous Si films presents different characteristics compared to crystalline Si and currently have a maximum efficiency of 10.2 % [10]. The main difference is that there is no long-range order in the amorphous film. There are many dangling bonds in amorphous films that create trap states throughout the bandgap region, to remove these dangling bonds they are hydrogenated during the deposition. Solar cells fabricated from a-Si:H are based on a *p-i-n* structure rather than a *pn* junction. This is because the doping necessary to generate the field across the junction results in a very high defect density, greatly reducing carrier lifetime. The main disadvantage of a-Si:H cells is the photo-induced increase in defect density which causes poor performance [28]. Therefore, the current research goal is to eliminate this effect.

CIS is one of the most promising thin film solar cell devices. Its bandgap can be modified over a wide range (*e.g.* 1.0 – 1.65 eV) by substituting Ga for In or Se for S. Ga can also enhance the u_{vb} due to increase in L_R and improve adhesion between the CIS and the molybdenum electrical back-contact [29]. Currently CIGS cells have efficiency of > 22 % [10].

CdTe is one of the best materials for solar cell applications as it is a nearly ideal material for absorbing the maximum amount of the solar spectrum with minimal losses. The most recent record efficiency for both small area and large module are 22.1 % [30] and 18.6 % [10], on-par with multi-crystalline Si. One of the critical issues for CdTe based devices is the formation of an ohmic back-contact, which requires in most cases a chemical treatment of the surface. Also, they require a post deposition heat treatment in a $CdCl_2$ environment to perform well.

The state of the art properties and fabrication techniques of the CdTe based thin film solar cells are detailed in the next chapter, including cell design and structure, back-contact formation and heat treatment.

CHAPTER 3

3 Cadmium Telluride Thin Film Solar Cells

This chapter focuses on a review of CdTe thin film and devices used in PV applications. Since CdTe based solar cells have a multilayer structure, chemical, physical and morphological characteristics of each layer play important roles in the efficiency of the device. Therefore, this chapter reviews the functions and properties of each layer that constitutes the CdTe thin film solar cell as well as state of the art performance.

3.1 Introduction

Thin film properties are often different from those of the bulk material, as influence of the surface on the structure becomes more noticeable as the film is thinner. Thin films can be deposited using various techniques, involving physical or chemical deposition, vacuum or atmospheric pressure systems. Depending on the deposition methods, the resulting material characteristics such as optical and electrical properties, crystal orientation, morphology, internal stress of the thin film can vary.

Thin film technology has diverse applications which include electronics, optics, aesthetics, and corrosion protection. An opto-electronic application is PV. Thin film

PVs is an alternative to traditional Si technology with the advantage of reducing the amount of semiconductor material used for solar cell devices to a few microns thickness.

The cost aspects require PV devices to be fabricated from abundant material with low energy consumption, and with negligible environmental impact while showing a high efficiency of solar to electrical energy conversion. Therefore, thin film materials have been the subject to intensive research. Figure 3-1 shows the remarkable improvement of cell efficiency of thin film (green) and all other technologies.

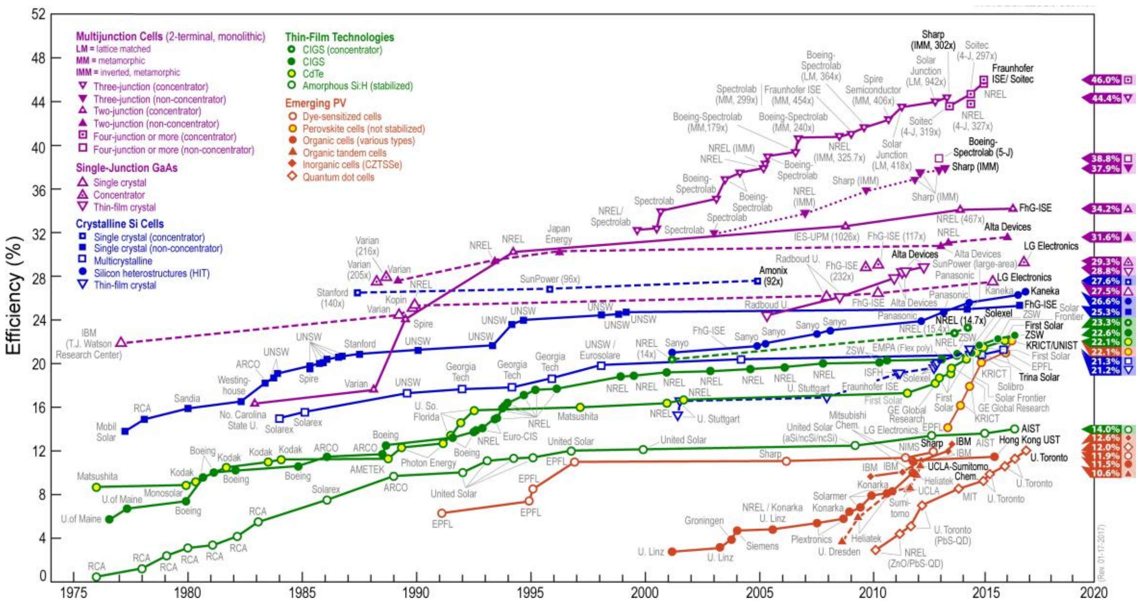

Figure 3-1: Development milestone for best research-cell efficiencies [30]**.**

3.1.1 Potential of CdTe Thin Film for PV Application

Solar technology based on CdTe thin film is the cheapest and offers the fastest energy payback time of all current commercial PV technologies with a theoretical efficiency limit of ~ 30 % [22]. CdTe is a nearly ideal material for absorbing the maximum amount of the solar spectrum with minimal losses and can be deposited using a wide variety of techniques. It is a semiconducting material with a direct energy bandgap of 1.44 eV and high optical absorption coefficient in the visible wavelength range ($6 \times 10\Sigma\mathrm{cm}^{V\Pi}$[31]); therefore, complete absorption of visible light occurs within 2 µm of the material [32]. The maximum recorded laboratory efficiency produced is now over 22.1 % for a small area device [33]. Table 3-1 shows the maximum theoretical output properties of a CdTe solar cell.

Table 3-1: Overview of theoretical PV properties of CdTe thin film [34]**.**

CdTe	
Bandgap (eV)	1.44
Maximum theoretical Y_{ab} (mA/cm^2)	30.5
Maximum theoretical u_{vb} (V)	1
Maximum CdS/CdTe potential (V)	1.1
Maximum theoretical efficiency (%)	~ 30

CdTe thin film solar cells are multilayer structures consisting of semiconductor and metal layers. Frerichs first measured the photoconductivity of CdTe in 1947 [35], but it was only in 1956 that CdTe found application as a PV material [22], using a *pn* homojunction. Later on heterojunction using an *n*-type single crystal CdTe was combined with another *p*-type material, such as Cu_2Te [36]. *P*-type CdTe was later employed as a single crystal to form a heterojunction with different *n*-type materials, such as indium tin oxide (ITO) [37], ZnO [38] or CdS [39]. The CdTe absorber layer is typically used in conjunction with CdS window layer in hetero structured solar cells.

3.2 CdTe Thin Film Solar Cell Structure

Thin film CdTe solar cells can be manufactured in the superstrate or substrate configuration. Figure 3-2 shows the cross-section diagram of the conventional CdTe solar cell in superstrate configuration (left) as follows: glass substrate/front contact/*n*-type CdS/*p*-type CdTe/metal back-contact, which was first described by Adirovich *et al.* in 1969, with evaporated CdTe on CdS/SnO_2/glass substrate giving an efficiency of > 2 % [40]. In superstrate configuration, the light enters through the substrate; therefore, it limits the substrates to transparent materials only such as rigid glass substrates. In 1972, to ultimately step away from the limitation of substrate transparency, Bonnet and Rabenhorst reached efficiency of 5 – 6 % in CdS/CdTe/Mo device in a substrate configuration [41]. This study defined the fundamental issues that affect the progress of high efficient CdS/CdTe thin film solar cells such as: the controlling role of doping efficiency in CdTe; the role of Cu in *p*-type doping of CdTe; the effects of abrupt versus graded CdS/CdTe junctions; the effects of active against passive grain boundaries; and the formation of low resistance contacts to *p*-type CdTe. The substrate configuration is constructed on metal or plastic although most of the time it is glass substrates in a reverse order compared to the superstrate configuration (figure 3-2 right) as follows: metal back-contact/*p*-type CdTe/*n*-type CdS/front contact. With the substrate configuration, thin flexible sheets can be utilized as a mechanical support and electrode. Following early work on polycrystalline superstrate and substrate [31] cells, the superstrate polycrystalline CdS/CdTe was further developed during the 1980s and 1990s [31]. The superstrate configuration progressed by modifications in device design, post deposition treatments and formation of low resistance contacts rather than by modifications in deposition methods. The PV behaviour of CdTe/CdS solar cells achieving a high conversion efficiency is independent of the CdTe deposition technique since CdTe has a relatively high chemical stability compared with the elemental a compound precursors used to prepare it.

The turning point for CdTe thin film solar cell performance was the introduction of post deposition air-heat treatment of CdTe/CdS structures with $CdCl_2$, by groups at Ametek and at the Institute of Energy Conversion [42, 43]. In 1993, a group at the University of South Florida combined the $CdCl_2$-treatment with advancements in low resistance contact formation to achieve efficiencies of > 15 % with CdTe deposited by close-space sublimation [44]. Additional advancements were followed by refinements in window layer processing [45] and employing vapour $CdCl_2$ treatments [46]. Since 2000, research has moved mainly towards superstrate polycrystalline CdTe/CdS solar cells due simplicity of the structure for manufacturing and high achieved efficiencies.

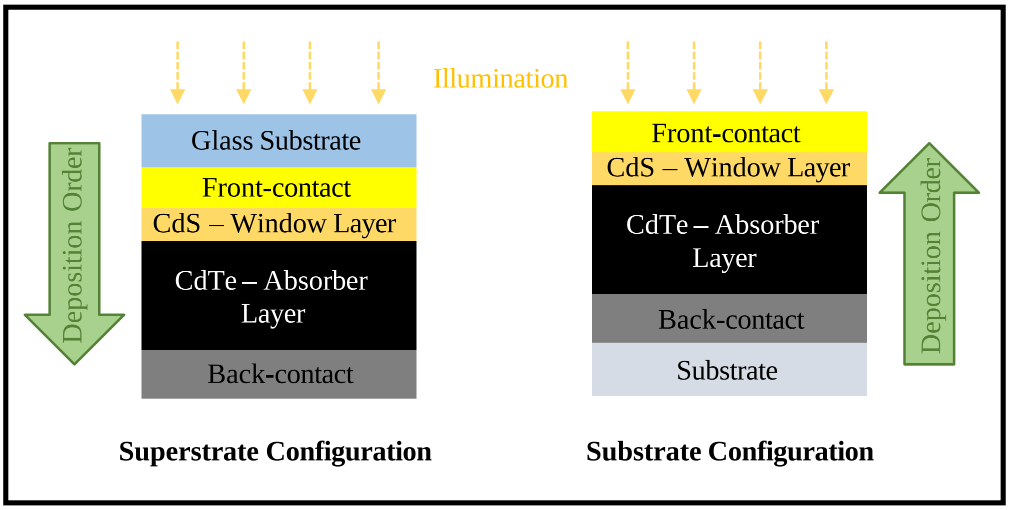

Figure 3-2: A schematic diagram of superstrate and substrate configuration for CdTe solar cell.

The challenges for CdTe thin film solar cells in superstrate and substrate configuration are listed in table 3-2.

Table 3-2: Key Challenges for CdTe thin film solar cells in superstrate and substrate configuration [1, 18, 47].

Superstrate Configuration:
- Substrate must be transparent and withstand high temperature processes.
- High weight and fragile nature of the modules due to the glass substrate.
- Difficulty to separately control the CdTe recrystallization and intermixing because the CdS layer is already present during the recrystallization of CdTe.
- Need for antireflection coating on the glass rear surface to reduce the reflection at the air-glass interface.
Substrate Configuration:
- Low efficiencies due to low open-circuit voltage and fill factor.
- Poor quasi-ohmic electrical back-contact and difficulty in maintaining low-resistance, as CdS/CdTe layers need to be grown at high temperatures and interdiffusion degrades the CdTe back-contact interface and cells are shunted.
- Poor CdS/CdTe heterojunction junction quality (recombination losses) due to high electron affinity and relatively large bandgap of CdTe that cause a severe Schottky barrier formation at the metal-CdTe interface with most of the metals.
- Poor film adhesion to substrates and the need for special contacting techniques between CdTe and the foil.

Despite the disadvantages previously listed, the substrate configuration has several advantages such as (i) possible reduction in optical losses at the front surface thereby higher current generation [31], (ii) use of lightweight and flexible substrates and (iii) roll-to-roll processing that can potentially increase production rate and decrease module cost [1]. Also, treating the CdTe layer at high temperatures before the CdS deposition permits a better control over the heterojunction formation and interface properties. This is another advantage of using substrate configuration as the temperature of the $CdCl_2$-treatment in superstrate configuration is limited at the point where the inter mixing gets excessive and the CdS layer gets consumed in the CdTe [1]. Even though, the maximum efficiency reported in the substrate configuration is low, this configuration has a large potential to further improve.

3.3 Layer Properties and Processing

In this section, the properties and growth processes of the different layers in CdTe based solar cells are described using both superstrate and substrate configuration.

3.3.1 The Substrate

Different substrates have diverse influences on the film microstructure, growth of the layers, and the device characteristics. Therefore, selection of a suitable substrate is important. The substrate should withstand high temperatures during fabrication processes. In addition, elemental impurities from the substrate must not diffuse into the layers of the solar cell device structure during high temperature processing. The substrate is an electrically passive component in the device and is required to be mechanically stable, matching the thermal expansion coefficient with deposited layers during the device fabrication.

The general choice of substrate in both superstrate and substrate configuration is glass as it is cheap and withstands relatively high temperatures. The glass substrate usually has a thickness of 2 – 4 mm. A common type of glass used is soda-lime glass (SLG) as it is robust to processing and inexpensive compared to other transparency glasses such as borosilicate, quartz or Vycor [31] and also with respect to other types of foil and flexible substrates. Even though SLG is generally preferred for low-cost production it has impurities such as Na, Mg and K that can diffuse into the other deposited layers. Sodium, a major constituent of SLG, is known to diffuse during thermal processes > 300 °C [48–50].

First Solar [51] achieved the lowest production cost per Watt on glass substrate that showed promising potential of the CdTe solar cells. Even though CdTe solar cell technology on glass substrates has progressed to a high level of manufacturing, it still has disadvantages (table 3-2). For example, in glass-molybdenum (Mo) samples, even though the glass substrate is mechanically durable at low temperatures, over 500 °C the substrate can deform plastically [52], which means that thermally induced extrinsic stresses in the glass-Mo sandwich may cause bending or mechanical distortion of the initially flat and smooth substrate. On the other hand, flexible metallic substrates have the advantage of being light-weight that makes them suitable for space and terrestrial application [53].

For terrestrial purposes, devices on flexible foil (*e.g.* flexible Mo substrate [54]) have a special advantage since they can be prepared on any appropriately oriented structure at lower costs. Also, polyimide (PI) film with a stable temperature up to about 450 °C [55], and high efficiencies of CdTe solar cells were achieved [56]. Flexible CdTe solar cells in substrate [54] and superstrate [55, 57–59] configurations on PI films have been developed. The use of flexible substrates is restricted in superstrate configuration to flexible PI film which is the only material with suitable properties [55]. Nevertheless, use of flexible substrate is possible in solar cells grown in substrate configuration. The main advantage of substrate configuration is that it allows the use of opaque substrates like metal foils to produce flexible cells. However, the reversed deposition order does not allow simple transfer of the process from one configuration to the other. The diffusion of impurities and chemical reactions between the layers can change when the deposition order reverses. Even though the development of flexible CdTe solar cell technology has just started, it has potential. The advantages of high speed deposition of CdTe/CdS and adapting those low temperature processes for roll-to-roll manufacturing could lead to reduction in production costs.

3.3.2 The Back-Contact

The important challenge with the fabrication of CdTe devices in a substrate configuration is the formation of a quasi-ohmic electrical back-contact that withstands all the deposition and annealing steps for activation as well as the formation of the *pn* heterojunction with minimized recombination losses. For polycrystalline CdTe solar cells, the back-contact is applied to the *p*-type semiconductor. The criteria of matching thermal expansion coefficients and work function, limit the choice of available substrate materials. Another issue is that during the $CdCl_2$-treatment, diffusion of impurities changes the ohmic contact properties [34]. To form an ohmic contact on *p*-CdTe, a metal with a work function

$(\sim^{\sim})$ greater than that of *p*-type CdTe 5.7 eV $(\sim^{\sim} > \sim_{D})$ [34] are required as illustrated in figure 3-3. The high electron affinity $(\tilde{o}_{D} = 4.28 \text{ eV}$ [60]) and relatively large bandgap of CdTe causes a severe Schottky barrier formation at the metal-CdTe interface with most metals as illustrated in figure 3-4 [61]. Additionally, CdTe shows strong Fermi level pinning due to its covalent nature. However, in an ideal case the metal Fermi level aligns with the upper VB edge. Mo is considered as a suitable substrate material from the point of view of matching thermal expansion coefficient of $4.8 \times 10^{V\Omega}$ $K^{V\Pi}$at 25 °C with CdTe ($4.9 \times 10^{V\Omega}$ $K^{V\Pi}$at 25 °C) [47]. But the difference in work functions of *p*-CdTe and Mo (~ 4.36 – 4.95 eV) demands the need of an interlayer between CdTe and Mo substrate which can give a non-rectifying tunneling contact. In 1980, the first Schottky barrier CdTe device Au/*n*-CdTe/ITO-glass was reported, and later the efficiency of this Schottky structure was enhanced to 6 % by including a CdS ohmic contact layer between the *n*-CdTe and the ITO [62]. The Amtek group further improved the electrodeposited CdTe Schottky devices by introducing a Cd-contact and in the early 1980s the first electrodeposited heterojunction CdTe/CdS solar cell was developed [63].

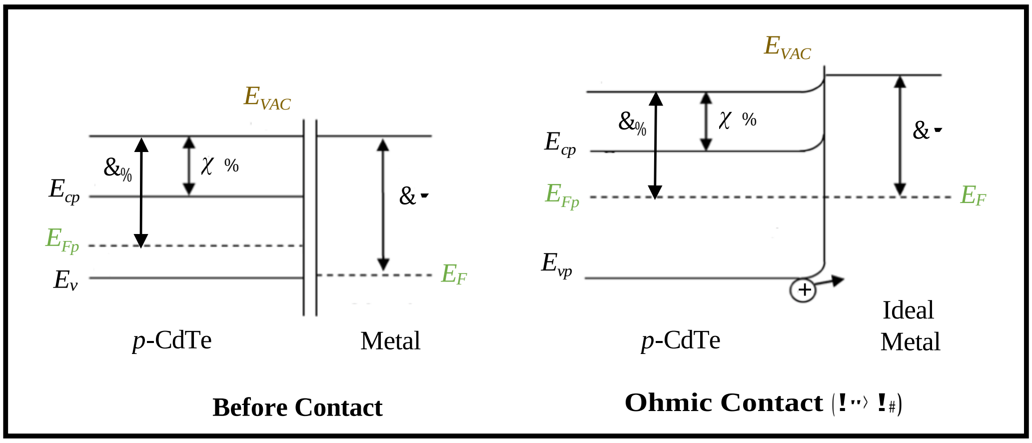

Figure 3-3: Illustration to show the band energies at the CdTe/metal interface before (left) and after (right) ohmic contact (ú$_{\text{ù}}$>ú$_{\text{ø}}$).

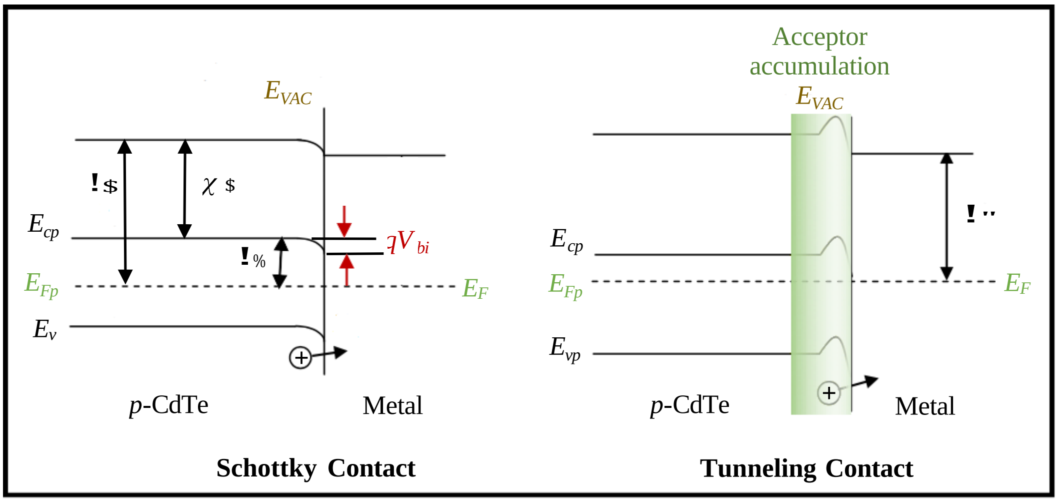

Figure 3-4: Illustration of a Schottky contact (left) and a tunnelling contact (Quasi-ohmic) (right) band diagram.

The common approach to overcome Schottky contact is the introduction of a highly-doped semiconductor buffer layer between the absorber and the metal back-contact. This buffer layer can either lower the Schottky barrier height when a high work function material is used or the barrier can be narrowed by the inclusion of a *p*-type layer with high acceptor density, allowing the holes to tunnel through the barrier [64]. Different materials have been tested as back-contact buffer layers. In the case of superstrate configuration, materials such as graphite paste, Te/Au, Sb/Au, Ni, PbTe, SnTe, HgTe, ZnTe, Au/Pd, As, Sb_2Te_3, As_2Te_3 and Te-rich surface [54, 62, 65–74] can be used. In the case of substrate configuration, various materials can be used, including ZnTe:Cu, Sb_2Te_3, MoO_x, Cu_xTe and antimony [47, 75–77].

A different method for contacting CdTe/CdS solar cell is to make contact to a n^+-CdS layer instead of *p*-CdTe layer by changing the cell structure to the following: n^+-CdS/p^+-CdTe/*p*-CdTe/*n*-CdS/ITO/glass substrate. Forming a low resistive tunnel junction between the absorber layer (p^+-CdTe) and the window layer would achieve the n^+-CdS contact. The CdTe layer doped with arsenic (As) creates the p^+region of the tunnel junction. Studies [78–80] have shown that to simplify the back-contact, the last part of the CdTe absorber layer can be heavily doped. The approach uses the same dopant as in the absorber layer itself, directly after the deposition of the CdTe:As absorber layer.

The back-contact is an area with intensive research and back-contacts with good contact properties and long-term stability are under investigation [81, 82].

3.3.3 The Absorber Layer

CdTe is an ideal II–VI compound semiconductor with high optical absorption and when ~ 2 µm thick it can absorb about 99 % of the incident photons [83] reaching a theoretical maximum efficiency of ~ 30 % [22]. Amongst the II–VI compounds, CdTe shows the highest average atomic number, least negative enthalpy formation [84], lowest melt temperature (1092 °C [31]), lowest vapour pressure [84], largest lattice parameter, highest iconicity (72 % [85]), and *p* and *n* type conductivity [86]. The crystalline CdTe should be *p*-type to form the *pn* junction with the *n*-type

CdS [39]. Since CdTe has a lower carrier concentration than CdS, the depletion region is mostly located within the CdTe where most of the carrier generation and collection occurs. Even though the as-deposited CdTe is either *n*-type or highly resistive *p*-type, a suitable heat treatment in the presence of $CdCl_2$ or oxygen [87–89] can convert it to *p*-type and potentially increase its conductivity. This will be further described in section 3.3.5.

One of the advantages of the CdTe technology is the simple phase diagram which is characterised by a congruently melting intermediate phase, α-CdTe, that forms at 50 atomic % Te (figure 3-5). The high liquidus temperature of 1098 °C at 50 atomic % Te, results from a strong ionic binding between Cd and Te atoms; therefore CdTe can form both crystallographic structures of zincblende and wurtzite depending on the pressure [90]. It has been shown that due to the low energy difference between the two phases, both structures can form within the same grain. When CdTe is deposited onto substrates above 449 °C, it condenses stoichiometrically as the stable phase in this regime [91]. CdTe can be Cd-rich or Te-rich depending on the deposition conditions [84]. When deposited from a binary source CdTe is generally stoichiometric, although Cd has a higher vapour pressure and the formation of Cd vacancies can occur [31]. In the cases of high temperature depositions, the films are deposited with Cd deficiencies, resulting in material property of *p*-type conductivity.

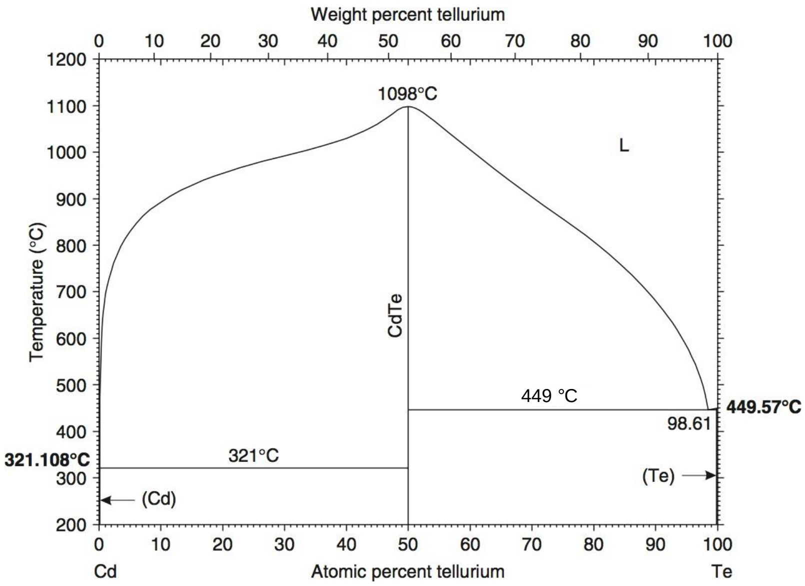

Figure 3-5 CdTe phase diagram [92]**.**

CdTe can be deposited using a wide range of deposition methods. The standard methods used to deposit CdTe thin film can be divided according to the substrate temperature. High temperature deposition methods (substrate temperature up to 550 °C): close space sublimation (CSS) [32], physical vapour deposition (PVD) or vapour transport deposition [93]; and low temperature deposition methods (substrate temperature up to 450 °C): RF sputtering [94], electrodeposition [62], high vacuum evaporation [56, 95], metal organic chemical vapour deposition (MOCVD) [79], chemical spray or screen-print deposition. The highest efficiencies for CdTe laboratory devices were achieved with either CSS or vapour transport processes [32, 44, 96, 97]. Figure 3-6 presents schematic illustrations the fabrication methods and deposition conditions. The deposition method and temperature affects the film structure.

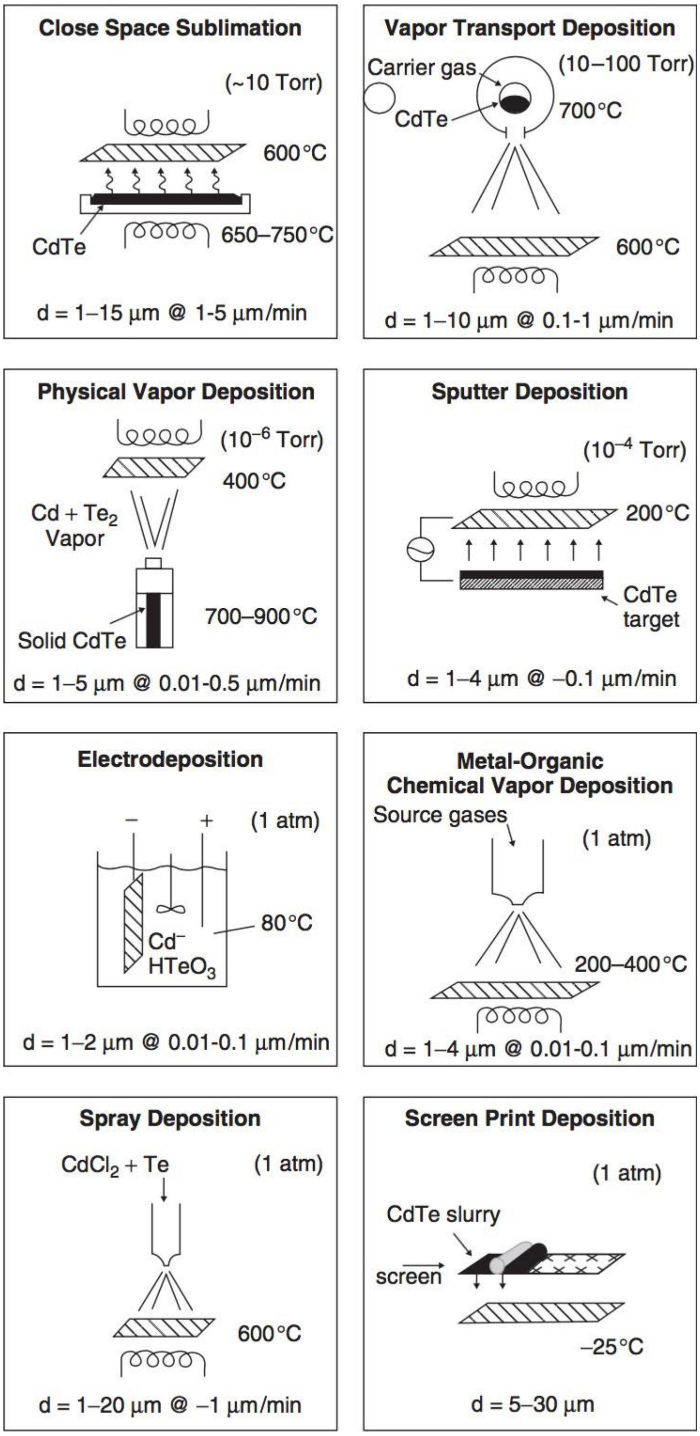

Figure 3-6: Schematic illustrations of CdTe film deposition methods including their nominal temperature and pressure conditions. The film thickness (d) and growth rate are shown at the bottom of each method (the substrate is the cross-hatched rectangle) [1]**.**

In order to evaporate CdTe films onto substrates at temperatures > 400 °C, re-evaporation of Cd and Te from the growing CdTe surface causes limitation to the deposition rate and utilization [1]. This can be reduced by depositing at higher total pressure (− 1 Torr) but mass transfer from the source to the substrate becomes diffusion-limited, therefore, the source and substrate must be close to each other. In CSS process, the CdTe source material holder has the same area as the substrate; the source holder and substrate cover serve as susceptors for radiative heating and conduct heat to the CdTe source and the substrate, respectively. In this process, the ambient for deposition typically contains a nonreactive gas such as N_2, Ar, or He. A small partial pressure of O_2 appears to be beneficial for good film density and solar cell junction quality.

Amongst the deposition methods, MOCVD is an effective method for CdTe film deposition [98]. MOCVD is a non-vacuum technique for depositing CdTe films from organic Cd and Te precursors in H_2 carrier gas (detailed process description in chapter 4). It was Chu *et al.* [99] who showed CdTe, grown by MOCVD, could be used for the PV applications. Promising PV efficiencies have been achieved using MOCVD for CdS while using CSS for CdTe [100]. However, the possibility to deposit the full CdTe/CdS junction by MOCVD using alkyl precursors was initially reported in 1998 [101]. Since then, improved *p*-type activation of the CdTe absorber layer has been obtained using As doping without $CdCl_2$ treatment [71]. The advantages of MOCVD include: (i) doping consistently in all areas of the device, (ii) controlling the growth of the CdTe/CdS structures and (iii) annealing in a controlled atmosphere during and after growth cycles. Also, the ability to fabricate the entire device structure using one method at atmospheric pressure and the potential to have an inline roll-to-roll process provides further benefits of using this method [102].

Rohatgi [103], Berrigan *et al.* [101] and Hartley *et al.* [104] reported a full polycrystalline MOCVD structures. Berrigan and Hartley took full advantage of the MOCVD method to control doping during growth. In situ Cl doped-CdS and As doped-CdTe formed PV solar cells have limited efficiencies. However, the performance was improved when undoped-CdS was used. In this condition, the CdTe deposition was optimised for a VI/II ratio of 1:1 at which devices demonstrated a 2 % efficiency, without the use of the post deposition treatment. Post $CdCl_2$-treatment, a study done by Rohatgi [103], the full MOCVD process produced a device with an efficiency of 11 %.

The polycrystalline nature of the CdTe film has an impact on device performance. There is a 10 % lattice mismatch between CdTe and CdS that results in dislocations at the interface and can impact the grain size. CdTe films with small grains (~ 1 µm) usually undergoes recrystallization and grain growth during processing for samples grown by low temperature methods. Where there is a preferred orientation it can be randomised during the recrystallization. However, films with large grains (> 1 µm), such as material grown at high temperatures normally have a grain structure that is stable to processing (the exception is in the near-interface region where small grains can exist [105]). Grain boundaries can induce trap states, and therefore should be appropriately passivated [106]. Grain boundaries are considered defects; high or low angle boundaries will affect the material properties (*e.g.* conductivity). High angle boundaries will give larger diffusion paths, promoting segregation or increase diffusion. When passivated, the grain boundaries outperform their single crystalline counterpart. According to Visoly-Fisher *et al.* [107] this can be described by the active participation of grain boundaries in charge separation and transport, which is caused by local downward band bending close to the grain boundaries. Dislocations occur in CdTe due to their low formation energy. These can be extrinsic, intrinsic or twin boundaries.

3.3.4 The Window Layer

CdS, an *n*-type semiconductor from the II–VI series in the period table has a large energy bandgap of ~ 2.4 eV at 300 K [86, 108] and low absorption and therefore it is largely transparent down to a wavelength of ~ 510 nm [109]. The main function of a window layer in a heterojunction is to form a junction with the absorber layer while permitting the maximum amount of light to the junction region and absorber layer. For high optical quality and relatively high electrical conductivity, the bandgap of the window layer should be as high as possible and the thickness as thin as possible to maintain low series resistance. Since CdTe has high absorption and cannot easily be doped to form a homojunction, the best option is to have a window layer and form a heterojunction. CdS is used as a window layer with CdTe to form the *pn* junction [39]. When a CdS layer is introduced into the device structure, it generally helps to reduce reflection losses and suitable energy band alignment with CdTe layer [110]. The optical transmission, thickness, thin film uniformity and film resistivity can affect the solar cell device efficiency.

A key reason for an efficient CdTe/CdS junction is that CdTe and CdS are miscible, and a reaction between them during the device fabrication leads to the formation of an interfacial layer of $CdS_{1-x}Te_x$ [111]. The formation of $CdS_{1-x}Te_x$ is responsible for lowering the interfacial defect density resulting in high efficiency devices [112]. This layer is formed during the post deposition $CdCl_2$-treatment of the of the CdTe/CdS structure.

Similar to CdTe, CdS can be deposited under most deposition conditions in a stable stoichiometric phase, α-CdS, usually in the hexagonal wurtzite structure [86, 108]. The CdS phase diagram is shown in figure 3-7. In high pressure growth conditions or in thin films, CdS may be found in a zincblende structure [86, 108]. CdS remains the best heterojunction partner for CdTe as high efficiency devices can be fabricated with reduced lattice mismatch, which is generally around 10 % with high defect density at the interface. To further reduce optical losses, alternative *n*-type materials are under investigation, for example $Cd_{1-x}Zn_xS$ [98] or $ZnO_{1-x}S_x$ [113].

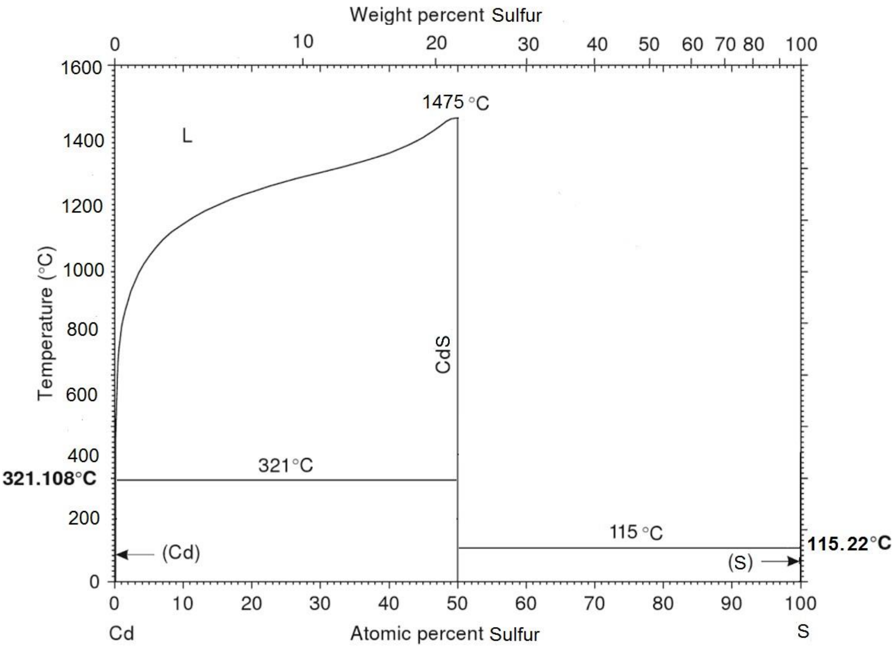

Figure 3-7:CdS phase diagram [92]**.**

Depending on the thickness of the CdS layer, some of the light below the 510 nm wavelength can still pass through to the CdTe layer giving additional photo current in the device. Since the CdS layer can limit current generation by absorption; this problem can be avoided by using thinner films but on the other hand the uniform coverage of the transparent conducting oxide (TCO) and the utilisation of CdS into the CdTe layer during annealing treatment requires that the thickness is not reduced below a certain limit, otherwise the cell is shunted or gives low voltage [114]. Also, the use of a thin CdS layer can lead to incomplete coverage of the CdS layer due to grain growth during the $CdCl_2$-treatment, leading to pinhole formation and locally occurring weak diodes. Pinhole formation causes shunts in the device specially when the thickness is reduced [115]. The simplest solution is the deposition of a thicker layer. However, the thicker the layer, the less light transmitted into CdTe layer. The optimal value of CdS layer thickness exists where reduction of u_{vb} and *FF* values due to pinholes and leakage along grain boundaries is minimized and transmission is maximized. Plotnikov *et al.* [115] showed a correlation between thickness and uniformity of the film and final efficiency with sputtered layers. The study showed an optimum thickness of the layer is 100 nm. Reducing the thickness below 80 nm results in severe losses in u_{vb} and *FF* due to non-uniformity of the CdS layer. Another solution is deposition of a thin layer of CdS with a second layer of small grains to fill pinholes (~ 80 nm), in a bi-layer structure which can improve the short circuit current of the cell [116]. In a bi-layer structure, pinhole formation is reduced, maintaining a relatively thin CdS layer.

The morphology, electrical performance, grain size, orientation and a crystallographic phase of the CdS layer is influenced by the deposition method and post deposition treatments. The most common deposition method is chemical bath deposition (CBD) which results in small grains and uniform coverage of the TCO surface [95, 117, 118]. However other methods include: high vacuum evaporation [39, 56, 119], CSS [44, 120], radio frequency sputtering [121, 122], metal organic chemical vapour deposition [123, 124], close space vapour transport [125] and spray pyrolysis [37]. Deposition of CdS at low temperature deposition methods (*e.g.* CBD) generally requires a post deposition heat treatment to increase grain size and reduce defect density [126]. This treatment has been found to be less influential for layers deposited by methods such as CSS, spray pyrolysis and screen printing where temperatures higher than 500 °C are used during the deposition. In the conventional glass based superstrate devices, the formation of the CdS layer is significantly easier as it is deposited before the CdTe layer. On the other hand, in the substrate configuration, the CdS layer is deposited on the rough CdTe surface which influences the formation of the CdS layer.

3.3.5 The Post Deposition Heat Treatment

As-deposited CdTe/CdS junctions exhibit poor PV properties. Therefore, a heat treatment is implemented to enhance the conversion efficiencies primarily by: (i) the formation of the interfacial layer, (ii) recrystallization and grain growth in the CdTe layer and (iii) defect passivation/carrier lifetime improvement in the absorber [127]. A heat treatment in a chlorine (Cl) and oxygen (O) containing ambient at around 400 – 450 °C is beneficial to the cell performance and is widely accepted in the CdTe solar cell device field [94, 128–130]. Mostly, $CdCl_2$ is used as the supply of Cl; however other chemicals such as freon [131] and magnesium chloride [11] were successfully used. This post deposition heat treatment in a Cl and O environment is known as $CdCl_2$-treatment or junction activation [132–135]. Oxygen has been reported to enhance *p*-type doping in CdTe solar cell devices [136, 137] and increase the minority carrier lifetime in the CdTe layer [138] and have an impact on CdTe/CdS interdiffusion [139]. Also, $CdCl_2$-treatment has been reported to improve *p*-type conductivity [88, 89]. This is not obvious as Cl is a *n*-type in CdTe, however this improvement can be explained by the formation of Cl A-centers (*p*-

type) [140]. During the $CdCl_2$-treatment, sulfur is introduced into the CdTe layer, which diffuses from the CdS layer into the CdTe layer and forms a CdS_xTe_{1-x} alloy at the interface [134, 141], which favours the growth of the CdTe grains as it enhances the mobility of Cd and Te atoms and leads to a more random arrangement after recrystallization [135]. The main consequence of the interdiffusion is that the light transmission through the buffer layer is reduced; however, this effect can be lessened by heat treatment of the as-deposited CdS to enlarge the grain size and improve film density. CdS diffusion in CdTe is a rapid process therefore it is difficult to control [31] and can be both beneficial and detrimental. The CdTe bandgap is reduced, which results in higher long wavelength quantum efficiency; but built-in voltage can reduce and shunt issues can result due to consumed CdS, leading to weak diodes [142].

The exact effects that $CdCl_2$-treatment has on the thin films and reasons why it is required to produce devices with good efficiencies (> 10 %) is still the subject of much research [143]. Major beneficial morphological changes occur when treated with $CdCl_2$, creating a better film for PV applications. Several investigations on the structural impact of the treatment were carried out. Although, these effects are difficult to list due to the dependence on the as-deposited sample morphology, the main changes observed are: grain orientation of CdTe layer; the interface between CdTe and CdS; reduction in the volume of grain boundaries and defects, resulting in reducing recombination; enlargement of grain size and shape. The bigger grains and less boundaries in thin film leads to higher minority carrier lifetime and lower resistivity. Several detected electrical effects include: increased conductivity and *p*-type doping; increased carrier life-time; Y_{ab} improvement due to increased acceptor density; u_{vb} improvement due to better structural quality; unpinning of the Fermi level at the CdTe/CdS interface [18, 144].

Various efforts to find the most efficient, safe and least expensive $CdCl_2$-treatment have been made and research is focused on understanding the actual mechanism of this treatment. The treatment can be performed either in situ or as a post deposition treatment. Several methods used to perform this post deposition process include: vapour transport [145], close spaced sublimation [146], thermal evaporation [57] and a wet chemical treatment [147]. The effects of the treatment are significant not only on morphological properties but also on the electrical performances. In superstrate configuration, the $CdCl_2$-treatment is done after the CdTe/CdS layer [141, 148]. In substrate configuration the treatment is done in various ways such as: post-CdTe layer [47, 75, 149, 150], post CdTe/CdS layer [151], or treatment after each CdTe and CdS layers [47, 69, 75, 150]. Also, a post processing annealing either after cell fabrication or after the CdS layer at relatively low temperatures ~ 200 – 250 °C was reported to be beneficial for device performance [75].

The main differences in the as-deposited device morphology are caused by the deposition temperature. The post deposition heat treatment is typically carried out for both high and low temperature deposited layers. Even though the treatment has a different effect on each deposition temperature, they both improve the structural quality of the layers by a reduction in stacking faults and misfit dislocations [152], which in turn improves the electronic characteristics of the CdTe recrystallization. In a low temperature CdTe deposition, the $CdCl_2$-treatment leads to recrystallization, grain growth and reduction of stacking faults in the CdTe layer

[141, 153, 154]. The treatment furthermore leads to reduction of optical losses with optimized interdiffusion of the CdS and CdTe layers. While these structural effects are enhanced by the presence of Cl, a $CdCl_2$-treatment is also required in high temperature grown solar cells, where it does not lead to significant structural changes, except for the region close to the CdTe/CdS interface, where the small CdS grain size has caused the formation of small CdTe grains during the early stage of the deposition [49].

3.3.6 The Front Contact

A highly transparent and conducting oxide layer with an electron affinity below 4.5 eV is required to form an ohmic contact and a good band alignment with the CdS ($õ_B = 4.5$ eV [60]). If the electron affinity of the TCO is higher than that of CdS, a blocking Schottky contact is formed (similar to that shown in figure 3-4 for a *p*-type contact). In general, TCOs are *n*-type semiconductors used as front contact that have good electrical conductivity and high transparency in the visible spectrum. For high efficiency cells, it is required that the sheet resistance of the front contact is ≤ 10 Ω/□. The conductivity of the TCO depends on the carrier concentration and mobility. In superstrate devices TCO deposition is the initial step, but in substrate configuration, it is the final step.

Transmission, reflectance and conductance are the key properties. Transmission and conductance show opposite behaviour as a function of thickness (*i.e.* the thinner the film, the higher the transmission and lower the conductance). Different front contacts result in slightly different growth of the semiconductor layers when used in thin film solar cells such as CdTe. The most common TCOs used for CdTe solar cells include: indium doped tin oxide (SnO_2:In or ITO) [155] and fluorine doped tin oxide (SnO_2:F or FTO) [82]. Their transmissions spectra are shown in figure 3-8. Other TCOs include: aluminium doped zinc oxide (ZnO:Al or AZO) [56] and cadmium stannate (Cd_2SnO_4 or CTO) [32].

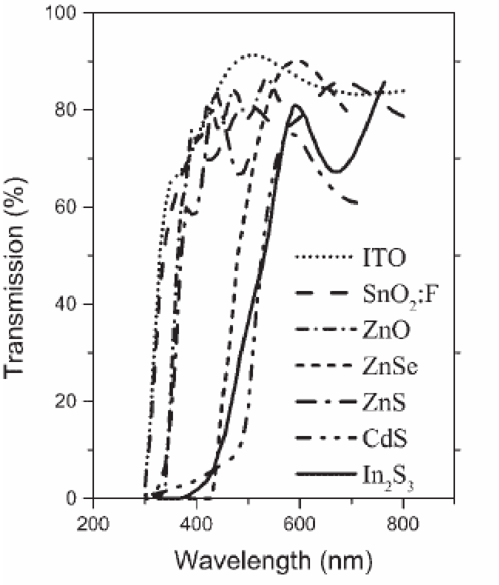

Figure 3-8: Optical transmission of different front contacts [34].

The TCO growth is influenced by the initial structure of the substrate, temperature and deposition method [156]. The layer can be deposited by different methods such as sputtering [32, 56], chemical vapour deposition [44], or spray deposition [157]. The most common material is SnO_2 deposited by sputtering or atmospheric pressure chemical vapour deposition. Since SnO_2 has a low conductivity, it is often doped with indium or fluorine. Depending on deposition temperature of CdS and CdTe films [158] either ITO or FTO is used. For low temperature deposition methods, ITO is selected, due to its high optical transmission for a given sheet resistance. Since ITO is sensitive to high temperatures and an increase of the electron affinity from around 4 to 5 eV is caused by oxidation or a post deposition heat treatment which results in a blocking contact [159]. It is often used in combination with a thin intrinsic SnO_2 layer between the TCO and the CdS window layer maintaining a high voltage by preventing possible shunts through pinholes in the CdS [160]. Use of a bi-layer TCO, one that consists of a low/high resistivity stack of transparent films has been found to effectively minimize efficiency losses resulting from the use of thin CdS films [96].

Even though ITO has proved to be one of the best TCOs on the market for different applications, there are issues regarding indium availability. AZO is one substitute for ITO. AZO is an *n*-type degenerated semiconductor where Al is used to dope ZnO to obtain higher conductivity, by improving the carrier concentration and mobility [161]. Its resistivity and chemical stability are less favourable than ITO; however, it is cheaper and exhibits higher transparency in the visible range. Another material is CTO which has shown improvements in power conversion [96] due to the higher conductivity compared to ITO and high transmittance.

3.4 Achieved Efficiencies

PV modules based on CdTe thin film technologies have manufacturing costs as low as US $ 0.6 /Wp in the superstrate configuration [162]. The most recent record efficiency for both small area and large module in this configuration are 22.1 % [30] and 18.6 % [33], respectively, on-par with multi-crystalline silicon. The rapid growth of CdTe superstrate configuration in the past few years is mainly achieved by minimizing optical losses in the window layers to improve the Y_{ab}. Other deposition methods have been used to develop solar cells on flexible and light weight substrates instead of rigid glass substrates. Devices with efficiencies up to 13.8 % [163] were achieved on flexible polyimide film in superstrate configuration.

Currently CdTe devices grown in the substrate configuration exhibit lower efficiencies of 13.6 % [164] and 11.5 % [164] on glass and flexible metal foil, respectively than those produced in the superstrate configuration. However, there is a lack of research on substrate configuration devices compared to the developed superstrate configuration despite some obvious advantages including roll-to-roll processing using lightweight and flexible polyimide or metal foils substrates. Since CdTe can be deposited quickly, roll-to-roll processes can increase the production and decrease module cost compared to other conventional processes. In addition higher current generation can be achieved compared to superstrate configuration by limitation of parasitic light absorption in the substrate material up to ~ 10 % [18, 47]. Furthermore, the growth in substrate configuration offers more control of the *pn* junction properties as recrystallization of CdTe and *pn* junction formation with CdS can be decoupled.

CHAPTER 4

4 Experimental Setup and Characterisation Techniques

This chapter describes the sample processing and characterisation methods used throughout this study. The procedures to fabricate the individual layers and devices used in this thesis are defined in detail in sections 4.1 and 4.2. Section 4.3 follows by outlining the characterisation methods used to study the properties of the materials and PV devices.

4.1 Thin Film Fabrication

Techniques such as magnetron sputtering, chemical bath deposition, metal-organic chemical vapour deposition, electron beam and thermal evaporation were used to fabricate the layers and structures in this study as shown in figure 4-1. These deposition techniques can be categorised into either physical or chemical depositions.

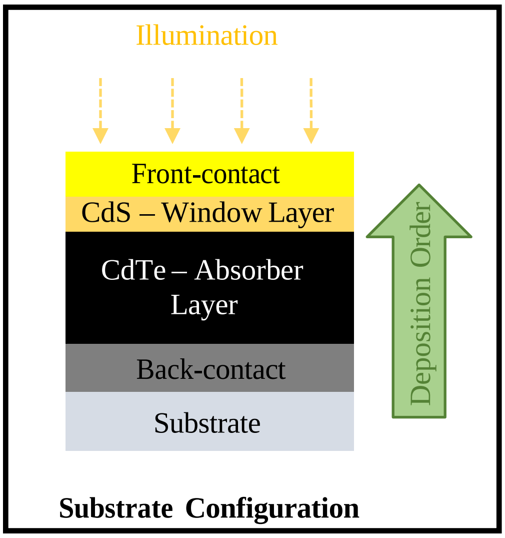

Figure 4-1: A schematic diagram of substrate configuration for CdTe solar cell fabrication in this study.

4.1.1 Substrate Preparation

Prior to any deposition the glass substrates were cleaned by standard means before being loaded into the appropriate chamber for the first layer deposition. SLG with the following composition: 10 % lime (CaO), 16 % soda (Na_2O), and 74 % silica (SiO_2) and quartz substrate composed of SiO_2 with purity of 99.999 % were used as substrates during this study. The standard cleaning procedure was as follows: the substrates were brushed twice with Decon90 solution diluted in deionised (DI) water (ratio 1:5) and rinsed thoroughly followed by 15 min ultrasonic bath filled with high purity DI water before drying under a nitrogen (N_2) stream.

4.1.2 Physical Depositions

Physical depositions use mechanical, electromechanical or thermodynamic concepts to grow a thin solid film on a substrate surface. Since most physical deposition techniques require vacuumed vapour environment, they are labelled as physical vapour depositions. High vacuum is essential to prevent reaction between the vapour and atmosphere.

4.1.2.1 Magnetron Sputtering

Magnetron sputtering is a powerful vacuum coating technique used to easily deposit high purity layers of metals, alloys and compounds onto a wide range of materials with thicknesses up to approximately 5 μm. Magnetron sputtering has several advantages over other vacuum coating techniques such as high adhesion of films on the substrate, excellent coverage of steps and small features, ability to coat heat-sensitive substrates, low temperature depositions, ease of automation and excellent uniformity on large-area substrates [165]. A schematic diagram of the sputtering chamber used in this work, Teer Coatings UDP 350, is shown in figure 4-2.

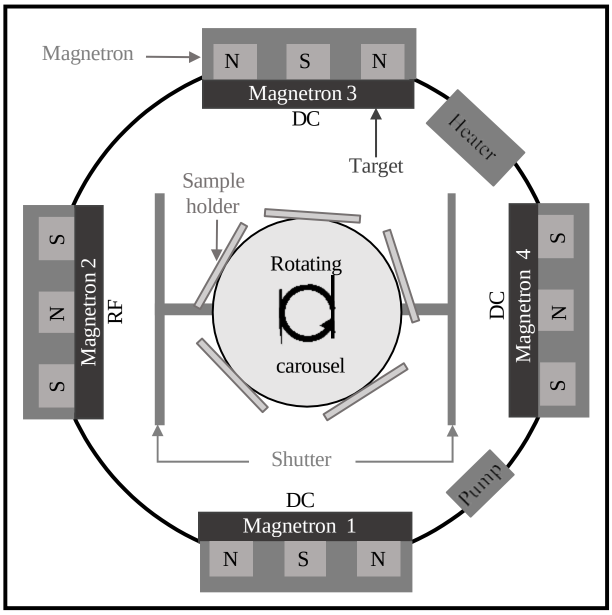

Figure 4-2: Schematic representation of the magnetron sputtering equipment: three targets operate in DC-magnetron mode and one target operates in RF-magnetron mode.

Magnetron sputtering is the process where atoms are removed from a target (or cathode) and emission of secondary electrons from the target surface by bombardment of high energy particles in this case by positive ions delivered from an electrical discharge in a gas (Ar^+) (figure 4-3). The magnets are arranged such that a magnetic field configured parallel to the target surface can constrain secondary electron (e^-) motion to the vicinity of the target, increasing the probability of gas ionisation. These secondary electrons are essential for creating the plasma. The increased ionisation efficiency achieved in the magnetron mode allows the plasma to be maintained at lower operating pressures and voltages than in unbalance sputtering mode [165, 166].

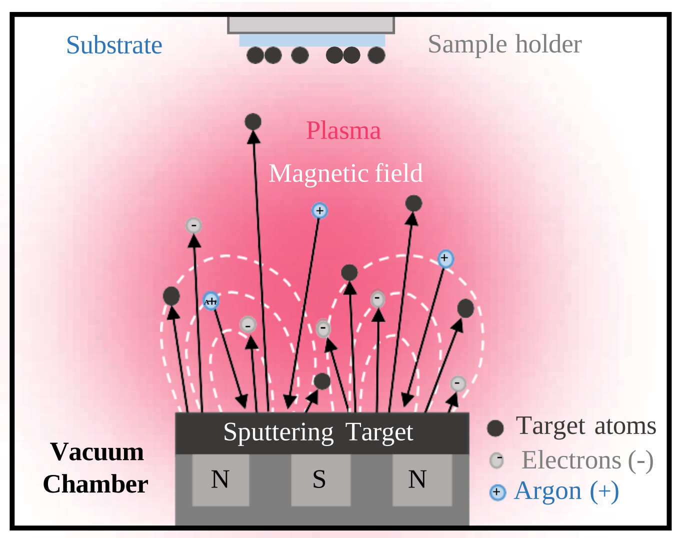

Figure 4-3: Schematic illustration of magnetron sputtering system.

Magnetron sputtering runs in two modes, direct current (DC) and radio frequency (RF) sputtering. In DC mode, the target is directly conducting electricity and is subject to I^2R losses. RF mode requires an impedance matching network to guarantee maximum power absorption into the plasma. RF sputtering was established to enable the sputtering of dielectric materials and has the dual advantage that it will sputter metals as well as insulators. Considering that and the complexity of RF generators, DC power supplies are simpler and cheaper to purchase. DC magnetrons will not work for insulating targets as no current can flow through them; therefore to overcome this, use of pulse DC or RF is considered (*e.g.* ZnO) [165].

In order to provide an electrical back-contact, a thin film of Mo with thickness of ~ 1 µm was deposited on either SLG or quartz substrates (76 × 26 × 1 mm^3) using DC magnetron sputtering. A rectangular target with dimensions 248 × 133 × 10 mm^3 of 99.95 % purity, supplied by PI-KEM Ltd, was used. The substrates were placed into the sputtering chamber parallel to the target surface at a substrate-target distance of 70 mm before evacuating down to $< 7 \times 10^{V\Omega}$ mbar. A standard 20 min pre-sputtering treatment was done to clean the target surface and eliminate all adhered impurities. The sputtering time 30 – 100 min, current 1.5 – 4 A and Ar-mass flow rate 25 – 70 sccm (Ar pressure 3 – 10 mTorr) were varied to adjust the morphological and structural properties of the Mo samples prepared at room temperature. The substrate carousel was equipped with five sample holders holding three full slides each, and was set to rotate at a constant rotation of 2.5 and 5 rpm to enhance the homogeneity of Mo films.

Pulse DC magnetron sputtering was also used to deposit the intrinsic transparent zinc oxide (ZnO) layer at room temperature. A circular target with diameter 100 mm and thickness of 3 mm of 99.99 % purity, bonded to 3 mm copper back plate was used. A standard 20 min pre-sputtering treatment was followed by a 35 min deposition in Ar/O_2 working gas at Ar pressure of 7.5 mTorr, voltage of 600 V and current of 0.2 A, respectively. The carousel was rotating at a speed of 5 rpm to achieve a homogenous layer of ZnO with a nominal thickness of 60 nm.

The indium tin oxide (ITO) layer was deposited using RF magnetron sputtering following the ZnO deposition at substrate temperature of ~ 150 °C. After the standard pre-sputtering stage, 200 nm thick layer of ITO were deposited on the samples rotating at 5 rpm with an RF forward power of 200 W for 90 min at a pressure of 3 mTorr. A circular target with purity of 99.99 % In_2O_3/SnO_2 (90/10 wt %) with diameter of 100 mm and thickness of 3 mm bonded to a 3 mm thick copper plate was used for this deposition.

4.1.2.2 Electron Beam Evaporation

In electron beam evaporation, the source material is evaporated via a high-energy electron beam to form a thin film in high vacuum. A typical setup is shown in figure 4-4. Once ideal base pressure of $< 10^{V\neg}$ mbar has been achieved the evaporation process begins by passing current through the filament unit resulting in electron emission from the gun. The beam is focused and bent by a series of magnets onto the evaporation material which causes vaporisation. The vapour condenses onto the substrate surface [167, 168]. This technique also offers many advantages such as high deposition rates, dense coatings, controlled composition and microstructure, low contamination and high thermal efficiency [168].

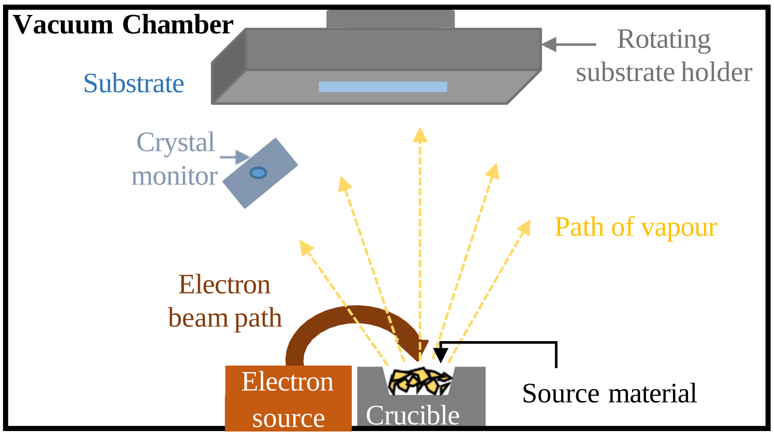

Figure 4-4: Schematic diagram of electron beam evaporating system.

The front contact nickel (Ni) and aluminium (Al) bilayer of the device were deposited in the same chamber using this technique, Tecvac ECU 700. The substrates were covered with a shadow mask pattern and placed parallel to the evaporation source at a distance of 40 cm on suitable substrate holders. The chamber was evacuated down to 10^{-5} mbar. The Ni and Al pieces, placed in copper and graphite crucibles respectively, were then subjected to heat produced by the electron gun to create evaporating conditions. The current was varied in the range of 0.01 – 0.40 A with voltage of 7 kV to achieve desired thickness of ~ 50 nm and ~ 1 µm for Ni and Al, respectively. The deposition rates of 0.2 nm/s and 2.0 nm/s were used for Ni and Al, respectively. The thickness and deposition rate were monitored using a quartz crystal oscillator. The substrates were rotating at a constant speed of 10 rpm to enhance homogeneity of the films.

4.1.2.3 Thermal Evaporation

Thermal evaporation is the simplest and cheapest PVD technique and is similar to electron beam evaporation where evaporating material is turned into vapour once heated and then condenses on a cooler substrate surface in a vacuum chamber [169]. Low pressure allows for free path of atom vapour, the average distance an atom travels in a vacuum chamber before collision with another atom, so that the particles can travel in straight lines from the boat towards the substrate once the shutters have opened (figure 4-5).

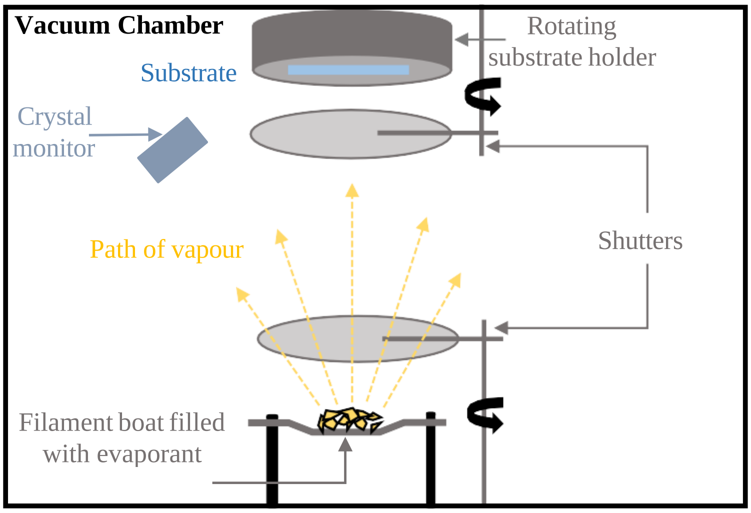

Figure 4-5: Schematic diagram of thermal evaporating system.

Thermal evaporation was used to deposit a thin (~ 10 nm) layer of sodium fluoride (NaF) at room temperature before or after the Mo layer using an Oerlikon Univex 250 system. The chamber was pumped down to $< 10^{V\Omega}$ mbar and a constant rotation speed of 10 rpm was set for the substrate holder to enhance homogeneity. The voltage was varied between 0.8 – 1.4 V to melt the 3 – 6 mm NaF pieces (sintered), 99.9 % purity using a Mo boat. The current was measured to range from 50 to 65 A during the evaporation. The thickness of the layer was controlled using a crystal quartz monitor.

4.1.3 Chemical Depositions

Chemical deposition is the growth of thin solid films on a substrate by a chemical reaction of a fluid or gas phase precursor.

4.1.3.1 Metal-Organic Chemical Vapour Deposition

Metal-organic chemical vapor deposition (MOCVD) is a complex chemical vapour deposition (CVD) process for growing crystalline layers using metal-organic (or organometallic) precursors in a chemical reaction which was first reported in 1968 [170]. During this process the chemicals are vapourised and transported into a horizontal reaction chamber where they reach a heated substrate. The heat enhances chemical reaction and turns the chemical into desired crystals. This process allows for high quality semiconductor layers with desired properties to be grown by varying the gas composition [171]. A schematic block diagram of an MOCVD system showing its functional subsystems is shown in figure 4-6.

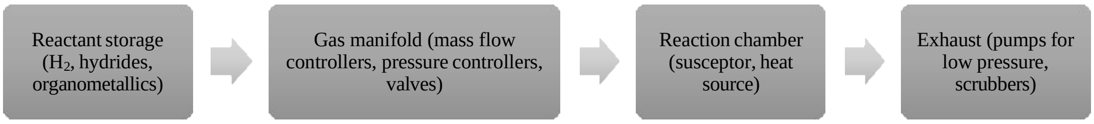

Figure 4-6: Schematic block diagram showing the function of an MOCVD system.

Amongst the variety of deposition techniques, MOCVD is capable of depositing high quality semiconductor and has been shown to be an effective technique for the deposition of polycrystalline CdTe PV cells [98].

The CdTe, $CdCl_2$ and CdZnS layers used in this work were grown by MOCVD at the Centre for Solar Energy Research (CSER), Swansea University. A schematic of the actual growth system is shown in figure 4-7. The organic precursors used were dimethylcadmium (DMCd), diisopropyltelluride (DIPTe), trisdimethylaminoarsine (tDMAAs), diethylzinc (DEZn) and ditertiarybutylsulphide for Cd, Te, As, Zn and S respectively. CdTe thin films were grown on Mo coated SLG and quartz substrates in a horizontal configuration using purified H_2 as the carrier gas and with a growth temperature of 390 °C [79]. An in situ triple wavelength (532, 670 and 980 nm) laser reflectometer was used to monitor the growing layer thickness and deposition rate of $CdTe:As^+$ (250 nm) and CdTe:As (2500 nm), where the As dopant concentrations are ~ 10^{19} atoms/cm^3 and ~ 10^{18} atoms/cm^3, respectively [98]. The $CdCl_2$ activation treatment [80] was carried out in situ at 200 °C after the growth of the CdTe layer, by depositing a 1 μm thick $CdCl_2$ layer and then annealed under H_2 at 420 °C for 10 min and cooled down. Also, a selected number of CdTe samples were deposited by cadmium zinc sulphide ($Cd_{1-x}Zn_xS$) ($0 \leq x \leq 0.9$) at 360 °C.

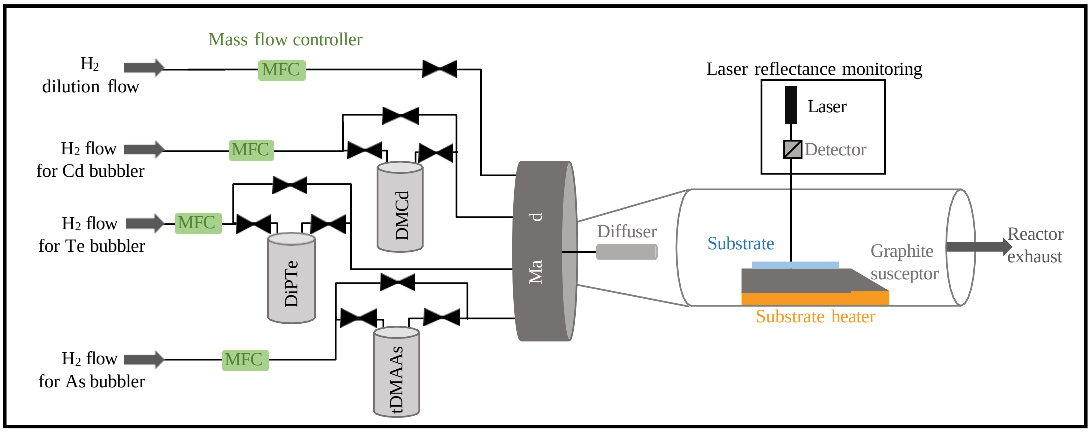

Figure 4-7: Horizontal reactor with gas supply for MOCVD growth. The actual system contains six bubblers for Te, Cd, S, As, Cl and Zn organometallics.

4.1.3.2 Alternative Chlorine Doping Methods

An alternative harmless and inexpensive chloride treatment is investigated in this thesis to replace $CdCl_2$ with $MgCl_2$. Vapour and solution processes are simple deposition techniques that were investigated to deposit $MgCl_2$ onto CdTe samples. The $MgCl_2$ solution used for this work was provided by Sigma-Aldrich.

During the vapour process a glass substrate was sprayed with $MgCl_2$ solution and placed inside the quartz tube furnace next to the CdTe sample, where the vapour deposition occurred during annealing stage in Ar gas. The deposition conditions such as annealing time 15 – 40 min and annealing temperature 300 – 450 °C were investigated during this process. This process did not allow for uniform samples to be fabricated therefore it was eliminated.

Solution process is similar to that of vapour process, however, the $MgCl_2$ solution was directly sprayed onto the CdTe surface at a set distance of 150 mm before being annealed inside a quartz tube furnace, allowing much finer control and uniformity. The deposition conditions such as annealing time 15 – 40 min and annealing temperature 300 – 450 °C were investigated for this process. The optimal processing conditions for this process was found to be 20 min annealing at 420 °C in Ar gas. Therefore, solution process was selected as the preferred process for $MgCl_2$ deposition for this study.

4.1.3.3 Chemical Bath Deposition

Chemical bath deposition is a simple and inexpensive deposition technique with an advantage of growing reproducible, homogeneous and adherent films [172]. CBD is suitable for thin film deposition on large areas at low temperatures ($< 100\ ℃$) without the need of sophisticated instruments. CBD was selected as a suitable method to deposit the CdS layer.

During the CBD process, the heat necessary to stimulate the chemical reaction is transferred from the bath to the sample surface. The deposition process is defined by two mechanisms of homogeneous and heterogeneous growth: a heterogeneous growth of cadmium sulfide (CdS) on the surface and homogeneous CdS formation in the bath volume [173]. Deposition of thin CdS films from aqueous solutions is a reaction between cadmium salt ($CdSO_4$) and sulphide agent (thiourea). Thiourea has a high affinity to metal cations and decomposes at low temperatures. Deposition process can be defined by two mechanisms [174, 175]. The homogeneous mechanism involves formation of layer with the CdS colloidal particles, that are formed in solution and consists of three stages [173]:

i. Ammonium dissociation

$$\mathbf{i}»^{§}_{\Sigma} + …»^{V} \rightleftarrows \mathbf{i}»_{W} + »\mathrm{I}… \tag{4-1}$$

ii. Thiourea hydrolysis $(NH_2)_2CS$ with the formation of sulphide ions

$$»µ^{V} + …»^{V} \rightleftarrows µ^{VI} + »\mathrm{I}… \tag{4-2}$$

iii. Final production formation

$$Aå^{§I} + µ^{VI} \rightleftarrows Aåµ \downarrow \tag{4-3}$$

Deposition of thin CdS films from the aqueous solutions through the stage of cadmium tetramin $[Cd(NH_3)_4]^{+2}$ complex ion formation, that reduces the overall speed of reaction and prevents $Cd(OH)_2$ formation by the heterogeneous mechanism, the general form is as follows [173]:

$$[Aå(\mathbf{i}»_{W})_{\Sigma}]^{§I} + (\mathbf{i}»_{I})Aµ + …»^{V} \rightarrow Aåµ \downarrow + 4\mathbf{i}»_{W} + »^{§} + (\mathbf{i}»_{I})_{I}A… \tag{4-4}$$

After removing residual $CdCl_2$ and $MgCl_2$ from the surface of the CdTe films with DI water, the CdS buffer layer was deposited by CBD. Initially, DI water was poured into a double-walled beaker and brought to a stable temperature of 70 °C. $CdSO_4$ (2 mM) and ammonia (1.5 M) were added to the solution successively while continuously stirring the solution to guarantee uniform thermal and chemical homogeneity for the deposition of the film. The samples with the following configuration: substrate/Mo/CdTe were then soaked in the solution as shown in the setup of figure 4-8 for 2 min before thiourea (12 mM) was added to the solution and left for 20 min. The samples were then removed from the solution, rinsed in DI water, dried using nitrogen gas and annealed at 200 °C for 10 min in air [176]. The annealing step is thought to promote some CdTe/CdS intermixing and provides opportunity to improve their electrical properties such as reducing their resistivity [47, 70].

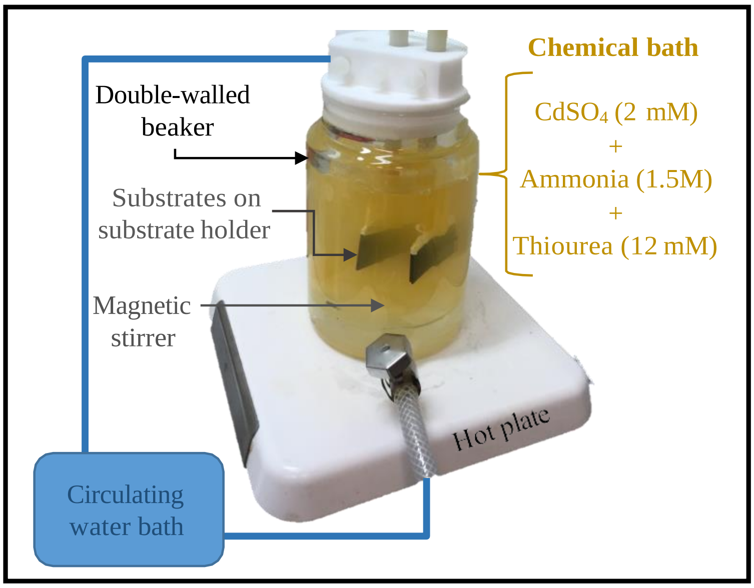

Figure 4-8: Chemical bath setup for depositing the CdS layer.

4.2 Characterisation Methods

Properties of the layers and solar cells were analysed using the techniques described in this section. The material characterisation includes: scanning electron microscopy (SEM), X-ray diffraction (XRD), secondary ion mass spectroscopy (SIMS), four-point probe and profilometer. The device characterisation includes: current density–voltage (Y–*V*) curves and external quantum efficiency (L¥L).

4.2.1 Scanning Electron Microscopy

Microstructural analysis is essential to fully understand the material properties such as grain size, surface morphology, composition and interdiffusion between the layers. The scanning electron microscope scans the surface of a sample with a high-energy electron beam to collect the resulting signal. Once the electron beam hits the sample surface, they interact with the sample atoms within a bulb shaped interaction volume and generate a variety of radiations that contain details about the surface topography, composition and other properties. The main emitted radiations are shown in figure 4-9. Secondary electron mode is the most common source used for surface topography imaging.

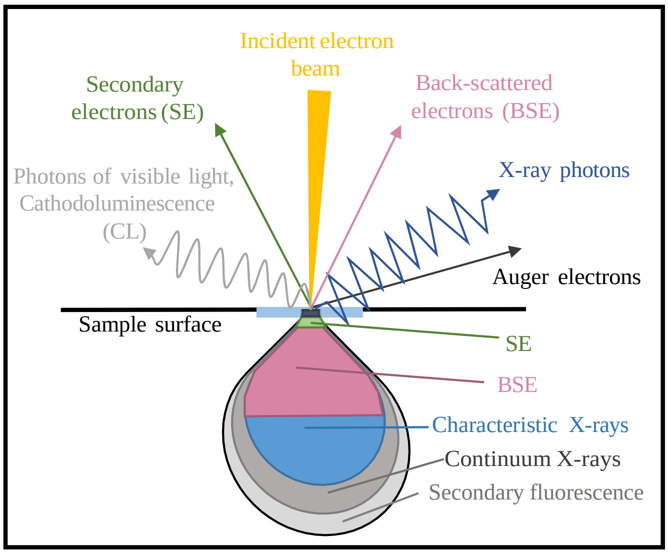

Figure 4-9: Schematic representation of electron beam interactions with the material surface (depth is dependent upon incident electron energy and material density).

In this study, a FEI Quanta 200 SEM and Tescan Mira 3 with operating voltage of 5 – 20 kV and working distance of 5 – 10 mm were used to investigate the CdTe solar cells stacks, as well as the individual layers that make up the cell.

4.2.2 X-ray Diffraction

X-ray diffraction is a powerful non-destructive technique based on the crystal lattice interactions with an X-ray beam, where interactions between the beam and material surface occur at specific incident angles. Crystallographic structures, phases, crystallinity, crystal orientation and stress can be extracted from this technique. Each crystalline material has its unique characteristic X-ray powder diffraction pattern (PDF) that is used for material identification within a standard diffraction database.

The diffraction condition is described by Bragg's law:

d ! = 2 åEFG @¨dÕ **(4-5)**

where is the incident X-rays wavelength, d_{hkl} is the spacing between atomic planes *hkl* in the crystalline lattice, *8* is the X-ray incident angle with respect to the diffracted atomic plane, *n* is the order of diffraction and equals to 1 in an XRD measurement. This is illustrated in figure 4-10 and is referred to as Bragg-Brentano 8 - 8 configuration.

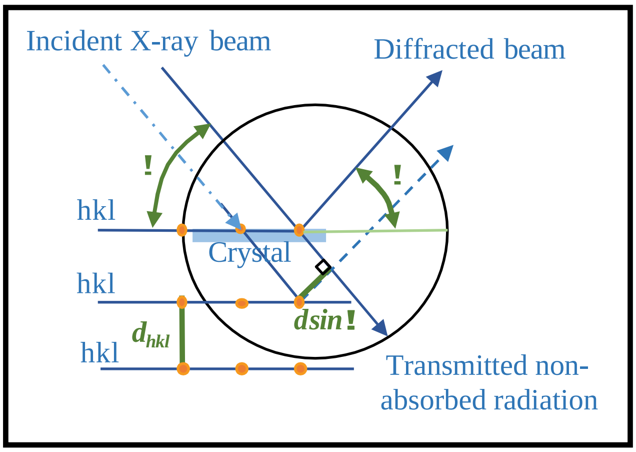

Figure 4-10: X-ray diffraction from atomic planes.

The XRD measurements for this study were carried out with Siemens D-5000 diffractometer using a Cu K_α radiation source (λ = 0.15406 nm). Typical scans were carried out from 20 ° to 90 ° with a step size of 0.02 °. During scanning mode, the instrument was operated at 40 kV and 40 mA.

4.2.3 Secondary Ion Mass Spectroscopy

Secondary ion mass spectroscopy is a highly sensitive analysis technique used to study the compositional details from the surface to the bulk of solid materials [177]. This technique uses an internally generated focused beam of positive or negative ions (primary beam) bombarded onto the substrate surface (under vacuum) to generate secondary ions that are transferred into a mass spectrometer (figure 4-11). There are different variants of the technique such as dynamic and static SIMS. In static SIMS, sufficient signal is obtained to provide a compositional analysis of the surface with minimum damage. Whereas dynamic SIMS obtains compositional information as a function of depth below the initial surface.

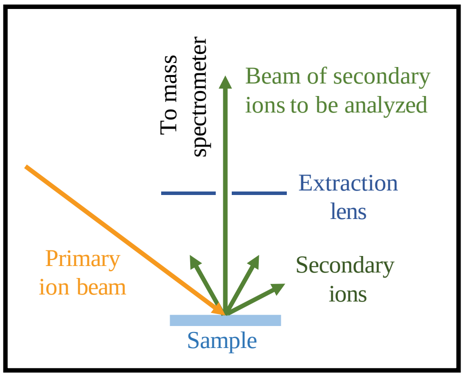

Figure 4-11: Schematic depiction of SIMS source region.

Elemental depth profiling was investigated by SIMS using a Hiden Analytical gas ion gun and quadrupole detector. A primary Ar^+ beam with an impact energy of 4 keV and beam current of 600 nA was used to sputter over a 600 × 600 µm rastered area with 10 % gating. The depth profiles were then normalized and an average count was calculated for the measured sets, this is described in more depth later in the thesis.

4.2.4 Resistivity and Sheet Resistance Measurements

Four-point probe is a device used for measuring material resistivity by sourcing a current through two outer probes and measuring its voltage through the two inner probes. The sheet resistance ($m_{\square}$) is calculated using:

$$m_{\square} = AH\,\frac{u}{\backslash} \tag{4-6}$$

where the correction factor (AH) is 4.53 using Van der Pauw technique for sample geometry in this work [178]. The material resistivity (π) was then calculated using:

$$Œ = m_{\square} \times s \tag{4-7}$$

where s is the film thickness. The $m_{\square}$ was measured at room temperature using a Keithley 2602 source meter and Jandel four-point probe for the Mo back-contact, intrinsic transparent oxide and indium tin oxide layers.

4.2.5 Thickness Measurements

A Bruker Dektak XT stylus profilometer was used to measure the thickness and roughness of each layer. The instrument measures step heights with a force of 3 mg precisely monitoring the displacement of a stylus placed in contact with the sample underneath it.

4.2.6 Current Density –Voltage characteristic

The performance of a solar cell was studied using a solar simulator by recreating the solar spectrum. Current is measured as a function of input voltage and a curve is generated.

The performance of the processed solar cells was evaluated using Y–*V* setup shown in figure 4-12. These measurements were performed in a four-wire configuration using a Keithley 2400 series source-meter in the dark and under illumination at room temperature. The current was then recorded as the voltage was typically swept from - 0.2 to 0.7 V. Illumination was provided by an Abet Technologies Sun 2000 solar simulator with an air mass 1.5 filter adjusted to 1000 mW/cm^2 using a GaAs reference solar cell.

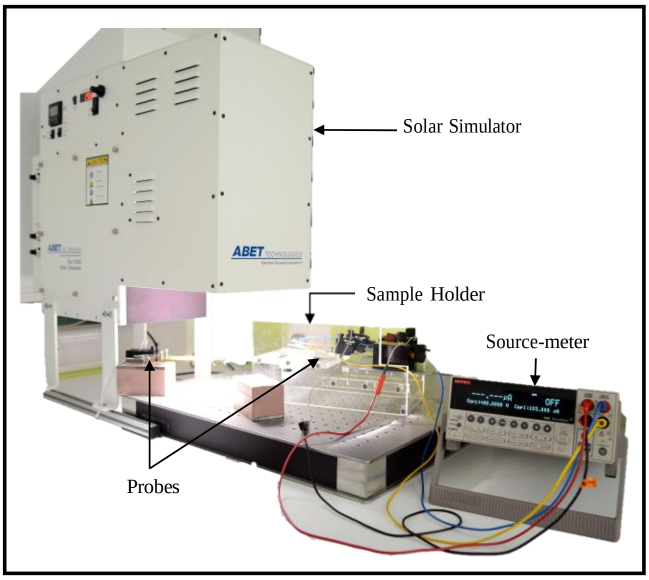

Figure 4-12: Current–voltage measurement setup.

4.2.7 Spectral Response Measurements

The spectral response of a solar cell was studied by the *QE* measurement as a function of wavelength. *SR* is theoretically similar to *QE* where the number of electrons output by the solar cell is compared to the number of photons incident on the device and is usually less than unity:

$$\mu \mathrm{m} = \frac{\mathbf{l\ !}}{h\ \mathrm{K}} \times \text{¥L} \qquad \textbf{(4-8)}$$

where l is the elementary charge, ! is the wavelength in nm, h is the Planck constant and K is the speed of light in a vacuum. ¥L has a strong wavelength dependence due to the spectral behaviour of the optical absorption coefficient of TCOs, CdS and CdTe, as well as depth dependence of the carrier collection probability. The as-measured ¥L is referred to as L¥L where absorption and reflection losses from the transparent layers are not considered.

The spectrally resolved response of the solar cells was measured using the L¥L measurement setup (figure 4-13). L¥L measurements were conducted in the dark at room temperature using a lock-in amplifier. A chopped light source and a monochromator (Bentham Instruments, TM300) generated the probing beam with a scanning step of 5 nm. Certified Si photo-diode with a wavelength ranging between 200 – 1100 nm was used as reference to calibrate the system.

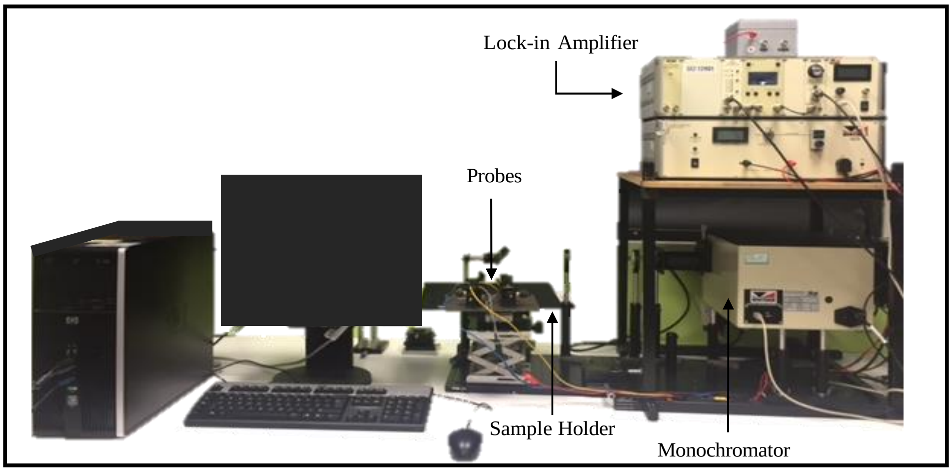

Figure 4-13: External quantum efficiency measurement setup.

4.3 Summary

In summary, this chapter gave an overview of the range of fabrication and characterisation methods used in this thesis. Example of a fabricated device is shown in figure 4-14. The aim of this study is to promote further recrystallization in CdTe thin film for substrate configuration devices by combination of Cl and Na. The next chapter will present and discuss the first step towards achieving this aim by studying the Mo back-contact.

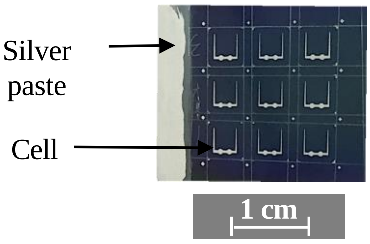

Figure 4-14: Fabricated solar devices, subscribed into nine individual 0.16 cm^2 cells.

CHAPTER 5

5 Mo Back-Contact Study

This chapter focuses on the optimisation of the Mo back-contact layer using DC magnetron sputtering. After a brief introduction in section 5.1, section 5.2 describes the approach to single and bi-layer deposition techniques with film properties detailed in section 5.3. Finally, the performance of the back-contact layer when included in a device stack is discussed in section 5.4.

5.1 Introduction

An important issue with the fabrication of CdTe devices in substrate configuration is the formation of a low resistance back-contact with a high stability. Mo was selected as an appropriate metallic back-contact as its thermal expansion coefficient ($4.8 \times 10^{V\Omega}$ $K^{V\Pi}$at 25 °C) matches that of CdTe ($4.9 \times 10^{V\Omega}$ $K^{V\Pi}$at 25 °C), easy production and compatibility with a variety of substrates. However, the work function difference between Mo (~ 4.36 – 4.95 eV) and CdTe (> 5.7 eV) can result in a severe Schottky barrier for the holes traveling from the absorber to the back-contact [47, 70].

The literature shows that there is a strong correlation between the working gas pressure, DC power and target-substrate distance and Mo film properties [177–179].

During this study, the influence of the Ar pressure, DC power parameters and the substrate rotation speed were investigated to achieve good substrate adherence and conductivity of the Mo films. Substrate adherence is vital as film delamination can result in solar cell performance degradation and device failure.

This polycrystalline layer is also considered to work as a filter for elements from the substrate (*e.g.* glass); for example, this is beneficial for CIGS solar cells as it allows diffusion of Na from the glass into the absorber layer to achieve high-efficiency devices [182]. In addition to Mo film optimisation, influence of impurity (*e.g.* Na) diffusion through the Mo film and absorber layer was explored. Na, a major constituent of SLG, is known to diffuse during thermal processes > 300 °C and has been shown to promote uncontrolled grain enlargement in CdTe absorber layers deposited using vacuum evaporation [48–50].

5.2 Back-Contact Layer Properties

In order to obtain optimised Mo films, four different depositions were implemented either on SLG or quartz substrates ($76 \times 26 \times 1$ mm^3) using DC magnetron sputtering: (1) deposition of single-layer Mo with varying Ar pressure, (2) deposition of single-layer Mo with varying sputtering current (3) bi-layer depositions of Mo film and (4) varying sputtering rotational speed. Set 3 is a combination of sets 1 and 2 with the best optimised depositions parameters where the first layer has excellent adherence and second layer has low resistivity [183]. The bi-layer Mo film also helps smooth the rough surface of the substrate. A smooth substrate surface is beneficial as the change in the surface topography such as spikes or cavities that may lead to shunts between the front and back-contact, and degrade adhesion of the solar cell to the foil substrate [34]. Table 5-1 shows the parameters that were used during the Mo back-contact film deposition.

Table 5-1: Process parameters for the deposition of the Mo films at room temperature.

DC-magnetron Sputtering Conditions	
Mo Target size (cm^2)	330
Substrate	SLG and quartz
Substrate rotation speed (rpm)	2.5 and 5
Base pressure (Torr)	7×10^{-6}
Sputtering current (A)	1.5; 3; 4.5
Sputtering pressure (mTorr)	3; 7; 10
Deposition time (min)	40 – 100

While studying the effects of the varying Mo deposition parameters on the mechanical and adhesion characteristics of Mo films, it is important to recognize that the entire solar cell is a multi-layer structure therefore the back-contact should withstand the subsequent processing steps. The cells were completed by the sequential layer deposition at high temperatures, which could affect the integrity of the substrate. Therefore, the performance of the Mo back-contact with the following configuration: substrate/Mo/CdTe/CdS/TCOs/Ni-Al was tested in parallel with the Mo optimisation studies.

5.3 Results and Discussion

The thickness and the conductivity were measured using stylus profilometer and the four-point probe technique, respectively. The morphology, structure and chemical composition were studied using SEM, XRD and SIMS.

5.3.1 Mo Growth Rate and Resistivity Properties

It is important to take the right precautions while preparing the substrates as cleanliness of the substrate influences adhesion. Three types of adhesive tests such as tape, scratch and solution test were performed on each Mo film to determine the adhesion strength of the films. These specific adhesion steps were followed to mimic the conditions the Mo back-contact should resist during the solar cell fabrication. The steps of the adhesion test were as follows: the sample was placed inside a plastic holder filled with DI water and placed inside the ultrasonic bath for 20 min to mimic the stage where the $CdCl_2$ and $MgCl_2$ residuals are removed. The sample was then dried using N_2 gun. Once this test was successful, the sticky side of the tape was firmly pressed over the sample and peeled off this step mimics the stage where the mask is held in place using tape. If the tape was clear of particles from the deposited Mo film a sharp blade was used to scratch the surface of the film which mimics the stage where deposited CdTe, CdS, ZnO and ITO are removed from a section of the sample and covered with silver paste to create a connection between the front and back-contact. The adhesion test results in table 5-2 show that there is good adherence between the substrate and the Mo film at higher sputtering pressure and current.

The Mo layer thickness was set at nominal value of 1.0 μm with sheet resistance $m_{\square}$ and resistivity π ranging from 0.16 – 0.59 Ω/D and 16 – 66 μΩ·cm, respectively as listed in table 5-2. At deposition current of 3.0 and 4.5 A the resistivity increases with sputtering pressure as is usually observed in sputtered Mo where increased pressure yields less dense films and more intra grain voids, increasing resistivity [184]. It is noticed that at a lower deposition power of 1.5 A, this trend is broken at the highest sputtering pressure, which results in the most conductive film. For a given deposition sputtering pressure, the Mo film resistivity reduces as power increases in agreement with other reports [52, 183, 184]. The measured data is summarized in table 5-2. The data in figure 5-1 shows that at higher sputtering pressure a higher resistivity is achieved. This increase in resistivity with pressure can be explained by a decrease in atoms energy in the gas discharge. Deposited particles on the substrate surface then have a lower mobility, and the as-grown film shows a porous columnar grain growth with interangular voids [181]. Even though a lower resistivity (range: 22.4 – 52.9 μΩcm) is observed at lower sputtering pressure the adhesion of the Mo film to the substrate is weak. However, as shown in table 5-2 the resistivity decreases as the sputtering current increases at a set sputtering pressure. For example, at 10 mTorr the resistivity decreases from 62.2 to 38.9 μΩcm for sputtering currents of 1.6 A and 4.5 A, respectively. Sputtering current is directly proportional to sputtering power, therefore increasing the sputtering power causes Ar ions to bombard the target with higher energy and thus greater numbers of Mo particles are deposited on the substrate, which causes the rapid growth of Mo film. Figure 5-2 shows that the growth rate increases with increasing sputtering current and therefore the resistivity decreases within a small range of 20 – 60 μΩcm for samples of the same thickness.

Table 5-2: Electrical properties of as-grown single-layer Mo thin film deposited at room temperature. The thickness is 1.0 ± 0.1 μm for all films. Adhesion test symbols √ and Ξ correspond to pass and fail, respectively.

Sputtering Current, *I* (A)	Power, (W)	Sputtering Pressure, P (mTorr)	Sheet Resistance, m□ (Ω/D)	Resistivity, ρ (μΩcm)	Adhesion Test
1.4	381	3	0.59	52.9	Ξ
1.6	390	7	0.59	58.5	Ξ
1.6	391	10	0.16	62.2	√
3.0	894	3	0.40	40.4	√
3.0	810	7	0.41	51.3	√
3.0	786	10	0.47	53.7	√
4.5	1390	3	0.27	22.4	Ξ
4.5	1418	7	0.33	33.5	√
4.5	1355	10	0.39	38.9	√

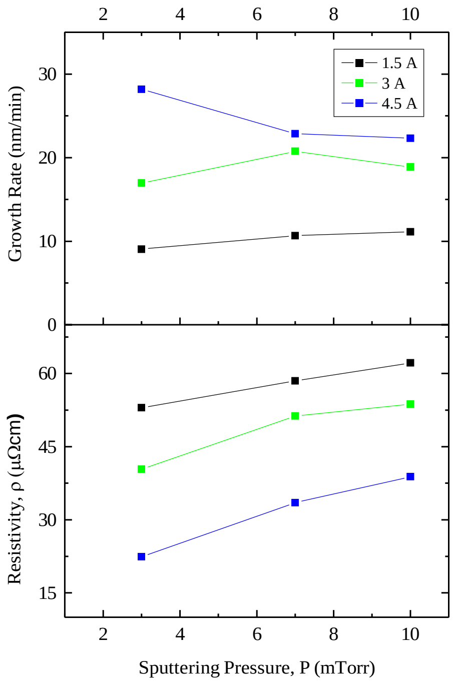

Figure 5-1: Growth rate (top) and resistivity (bottom) against sputtering pressure (3, 7 and 10 mTorr) for as-grown single-layer Mo films at sputtering current of 1.5, 3 and 4.5 A on SLG.

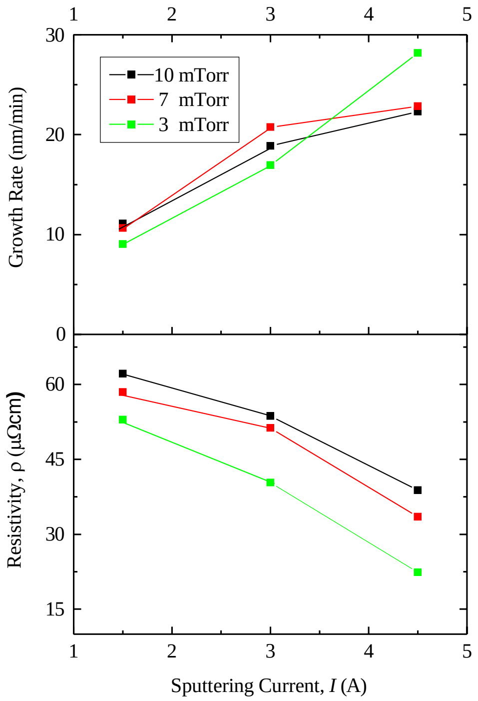

Figure 5-2: Growth rate (top) and resistivity (bottom) against sputtering current (1.5, 3 and 4.5 A) for as-grown single-layer Mo films was deposited at sputtering pressures of 3, 7 and 10 mTorr on SLG.

The bi-layer Mo films are a combination of optimised depositions parameters from the earlier study where the first layer has excellent adherence and second layer has low resistivity. At high sputtering pressure the Mo film has a better adhesion to the substrate and at high sputtering current it has lower resistivity. Therefore, sputtering pressures of 10 and 3 mTorr were used to deposit the first and second layer of the bi-layer Mo films respectively. The electrical properties of the films are listed in table 5-3 where the sputtering time of the layers and sputtering current were varied to observe the change in the resistivity and adherence. The tabulated results show that at a sputtering current of 3 A, the resistivity is 23 % lower when the first layer (10 mTorr) is grown at a faster growth rate. Sputtering time is directly proportional to sputtering current and power; therefore, when the current was decreased to 2 A, the sputtering time was increased. The bi-layer Mo films passed the adhesion test and have an average resistivity of 37 μΩcm.

Table 5-3: Electrical properties of as-grown bi-layer Mo thin films deposited at room temperature. The *1*st and 2nd layers were deposited at sputtering pressures of 10 and 3 mTorr, respectively. The thickness is 1.0 ± 0.1 μm for all films.

Sputtering Current, *I* (A)	Power, (W)	Time (min)		Growth Rate (nm/min)	Sheet Resistance, m□ (Ω/□)	Resistivity , *ρ* (μΩcm)
		1st Layer (10 mTorr)	*2nd Layer (3 mTorr)*			
3	807	20	40	15.3	0.43	39.6
3	804	5	37	23.1	0.33	32.3
2	462	10	74	12.0	0.39	39.3

5.3.2 Morphology Analysis

The surface topology and morphology of the Mo films were studied by SEM. The grains show a triangular shape at 7 and 10 mTorr which are well ordered with small variation in grain size. As shown in figure 5-3 the change in sputtering pressure does not affect the morphology of the Mo films significantly.

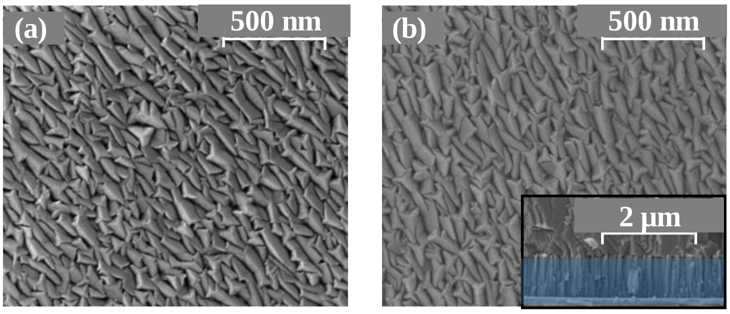

Figure 5-3: SEM micrographs of Mo films deposited on SLG at sputtering current and power of 3 A and 400 W at sputtering pressures of (a) 7 and (b) 10 mTorr (Mo film cross-section is shown in the inset).

5.3.3 Crystallographic Properties

X-ray diffraction was used to analyse the crystallographic properties of the deposited films. The peaks of (110), (211) and (220) planes corresponding to the diffraction angles of 40.5 °, 73.7 ° and 87.5 ° respectively were observed for all samples (figure 5-4). The Mo films have a body-centered cubic structure with a dominant direction of <110> (preferred direction). The (110) and (220) peaks show a similar trend where by decreasing sputtering pressure and increasing sputtering current the intensity of the peak decreases (figure 5-5 a and c). On the other hand, the (211) peak shows the opposite trend (figure 5-5 b).

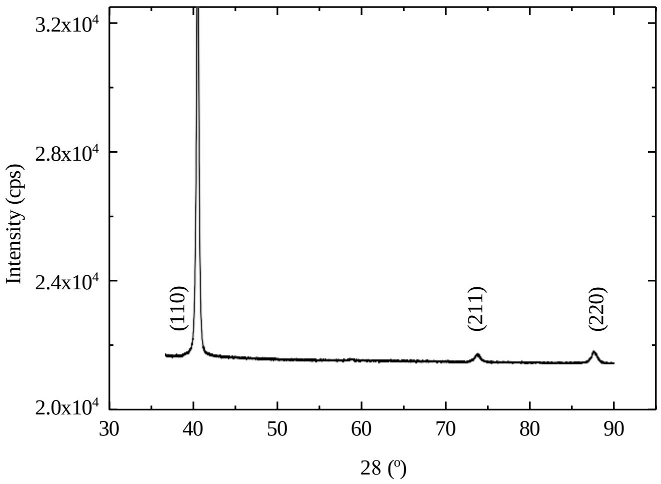

Figure 5-4: XRD pattern for the Mo film (deposited with sputtering conditions: 3 mTorr and 1.4 A) showing (110), (211) and (220) planes which correspond to the diffraction angles of 40.5 °, 73.7 ° and 87.5 °, respectively.

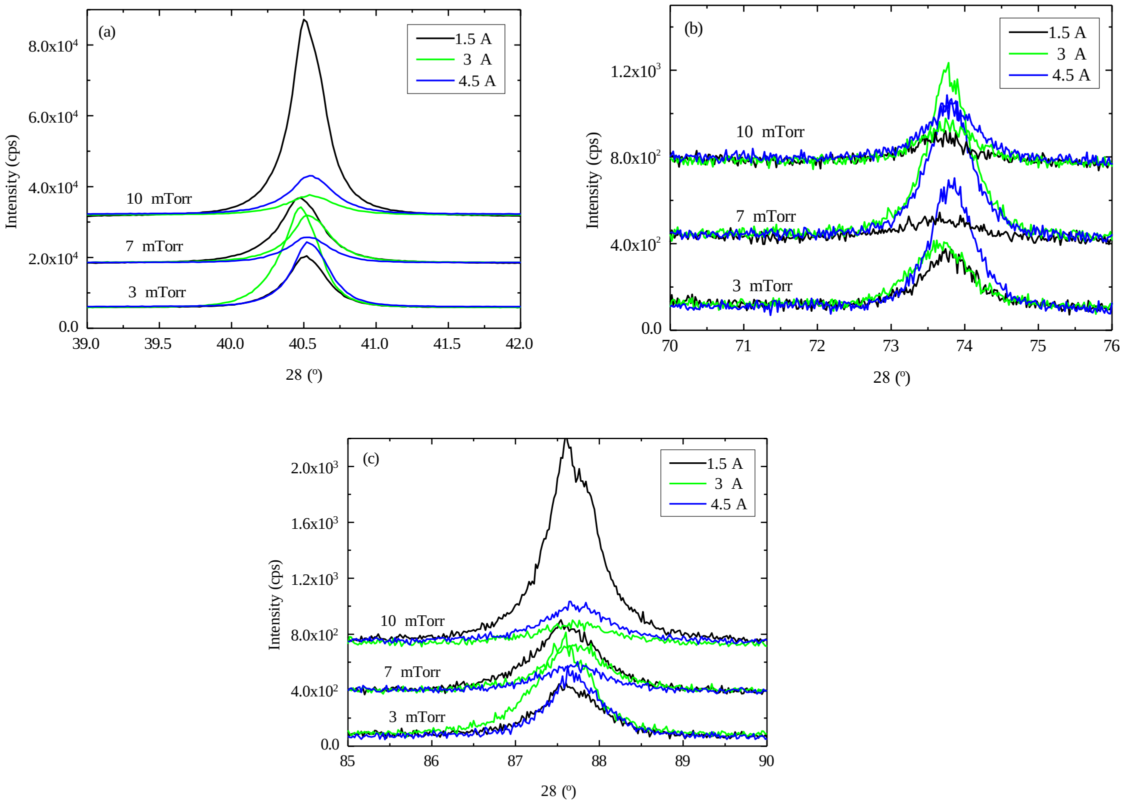

Figure 5-5: XRD peaks of (a) (110), (b) (211) and (c) (220). The Mo film was deposited with the following sputtering conditions: 3, 7, 10 mTorr; 1.5, 3, 4.5 A.

The effects of growth conditions on texture and preferred orientation of the Mo films were investigated by calculating the texture coefficient A_{EFG} [187]:

$$A_{EFG} = \frac{\backslash_{EFG} / \backslash_{p,EFG}}{\frac{1}{d}\sum_{B} \backslash_{EFG} / \backslash_{p,EFG}} \tag{5-1}$$

where *n* is the number of reflections, $\backslash_{EFG}$ is the intensity of the *hkl* reflection and $\backslash_{p,EFG}$ is the intensity of the *hkl* reflection for a completely random sample. A_{EFG} gives a measure of the enhancement of *hkl* reflection in comparison to the reference sample. The preferred orientation of each film, as a whole, was analysed from the standard deviation œ of all A_{EFG} values as compared with the reference [187]:

$$\text{œ} = \sqrt{\sum \frac{1}{d}(A_{EFG} - 1)^{I}} \tag{5-2}$$

The σ values are used to compare the degree of orientation between different samples, so that lower σ values indicate more randomly oriented samples. The reference sample (*i.e.* random sample) would have texture coefficients of 1 and preferred orientation of 0 while for a fully aligned sample the C_{hkl} would be 3 (as 3 peaks were used in the calculation) for that particular direction and 0 for the others. The variation of texture coefficient is shown in table 5-4. The data indicates a strong preferred orientation in the (110) direction for all samples except one sample deposited at sputtering current and pressure of 1.6 A and 10 mTorr. There is a decrease in the values of C_{110} whereas the C_{211} and C_{220} increase and decrease showing a shift in the crystallite orientation.

Table 5-4: Texture coefficients and degree of preferred orientation. The Mo film was deposited with the following sputtering conditions: 3, 7, 10 mTorr; 1.5, 3, 4.5 A.

Sputtering Current, *I* (A)	Power, (W)	Sputtering Pressure, P (mTorr)	Texture Coefficient, C_{hkl}			Degree of Preferred Orientation, σ
			C_{110}	C_{211}	C_{220}	
1.4	381	3	2.19	0.15	0.66	0.87
1.6	395	7	2.22	0.07	0.71	0.90
1.6	401	10	1.39	1.00	0.61	0.32
3.0	894	3	2.25	0.09	0.66	0.92
3.0	810	7	2.01	0.41	0.58	0.71
3.0	786	10	1.98	0.29	0.73	0.71
4.5	1390	3	2.10	0.24	0.66	0.79
4.5	1418	7	1.80	0.56	0.63	0.57
4.5	1355	10	1.86	0.37	0.77	0.63

All of the Mo films have a narrow (110) peak, which indicates that the Mo films are well crystallized during the deposition. The full width at half maximum (FWHM) of the (110) peak was used to determine the crystallite size via Scherrer formula assuming that the films are strain free [188]:

$$L = \frac{K\lambda}{FWHM \times \cos(\theta)} \tag{5-3}$$

where *L* is the crystallite size, *K* is the Scherrer constant (0.9 in this case), λ is the wavelength of the X-ray (0.15406 nm in this case), and θ is the Bragg angle. The crystallite size was calculated and ranged between 30 – 40 nm (data not corrected for instrument broadening). Figure 5-6 shows the range of FWHM averages between 1.4

– 4.5 A sputtering currents, for sputtering pressures of 3, 7 and 10 mTorr. The FWHM increases with sputtering pressure increase and stays within a small range of change with increase in current. Figure 5-7 shows the relation between FWHM and C_{110} texture coefficient where, as the sputtering pressure increases the FWHM decreases and C_{110} increases and becomes more random.

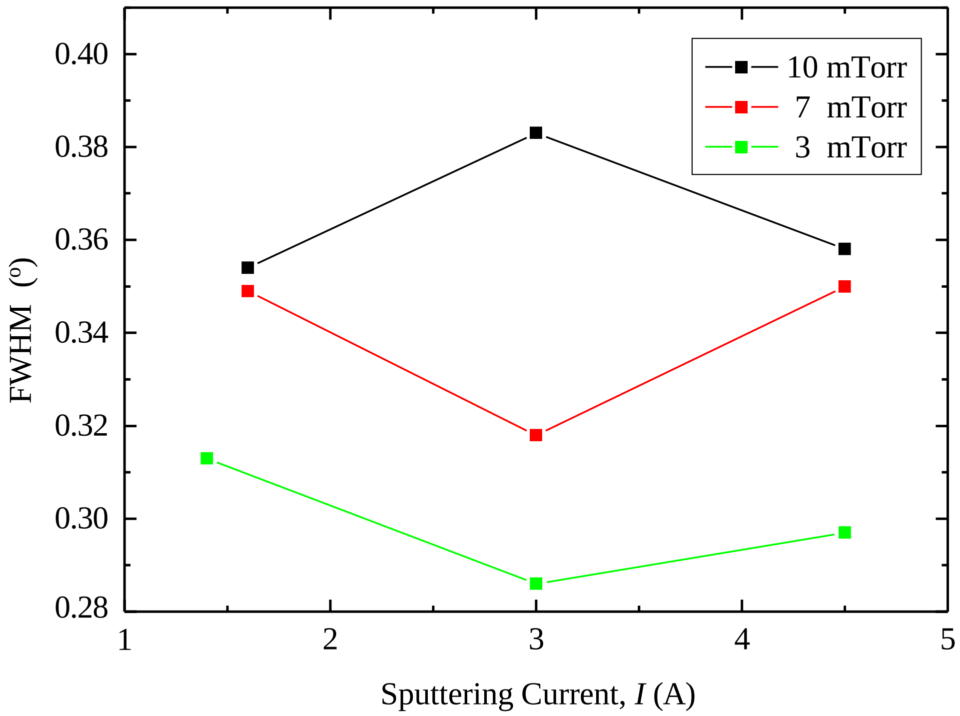

Figure 5-6: (110) FWHM as a function of sputtering current (1.5, 3 and 4.5 A) for the Mo films sputtered at pressures of 3, 7 and 10 mTorr.

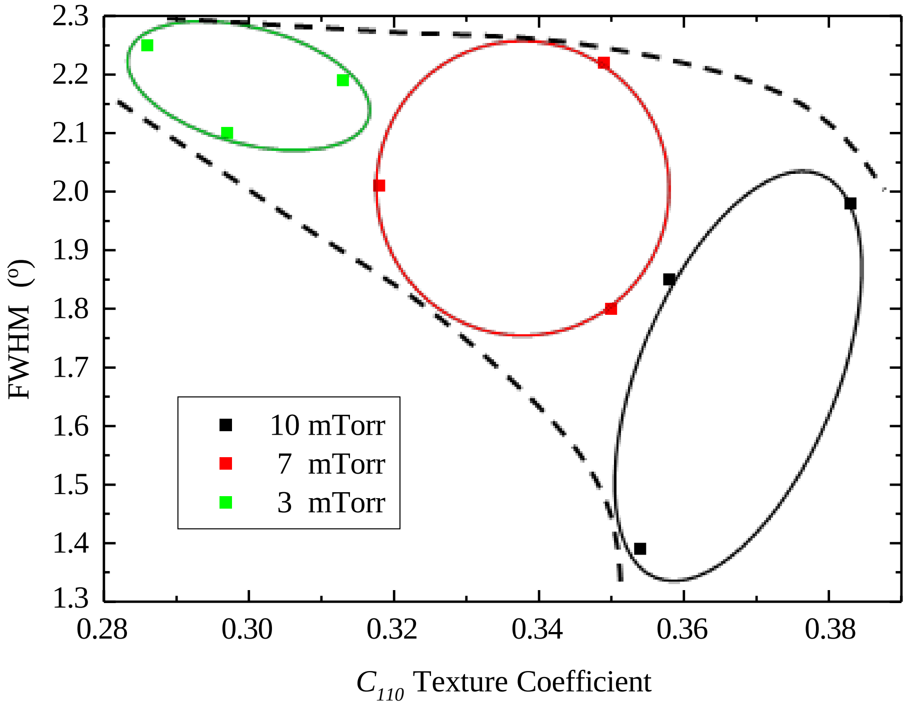

Figure 5-7: (110) FWHM as a function of C_{110} texture coefficient for the Mo films sputtered at pressures of 3, 7 and 10 mTorr. (Sputtering currents of 1.5, 3 and 4.5 A).

From the (110) peak the strain of the Mo cubic structure was calculated for each sample using the following formula [188]:

$$@s™x¨d(\ \%) = \frac{ß-Vß}{ß\_} \times 100 \qquad \textbf{(5-4)}$$

where x is the lattice constant (for Mo x^ = 0.315 nm [188]). The lattice constant determines if the strain is tensile (strain > 0) or compressive (strain < 0). Strain profiles in the sputtered Mo films could be due to few reasons, such as voids, oxygen or argon impurities and crystallographic flaws [189]. Poor adhesion can be caused due to high strain on the films and therefore compromise long term quality. The peak position shifts as the sputtering current is varied which reflects a change in lattice parameter which then explains the strain in the film (figure 5-8). All Mo films are in tensile strain as shown in figure 5-8. At low pressure of 3 mTorr and increasing sputtering current the tensile strain of the film increases. It is also shown that as the sputtering pressure increases the tensile strain increases with an exception at a sputtering current of 4.5 A, where it decreases before increasing again. The increase in sputtering pressure increases the frequency of gas phase collisions, reducing the kinetic energy of sputtered neutral atoms and reflected neutrals bombarding the growing films [188]. At the maximum pressure point the sputtering currents show a similar increased tensile strain.

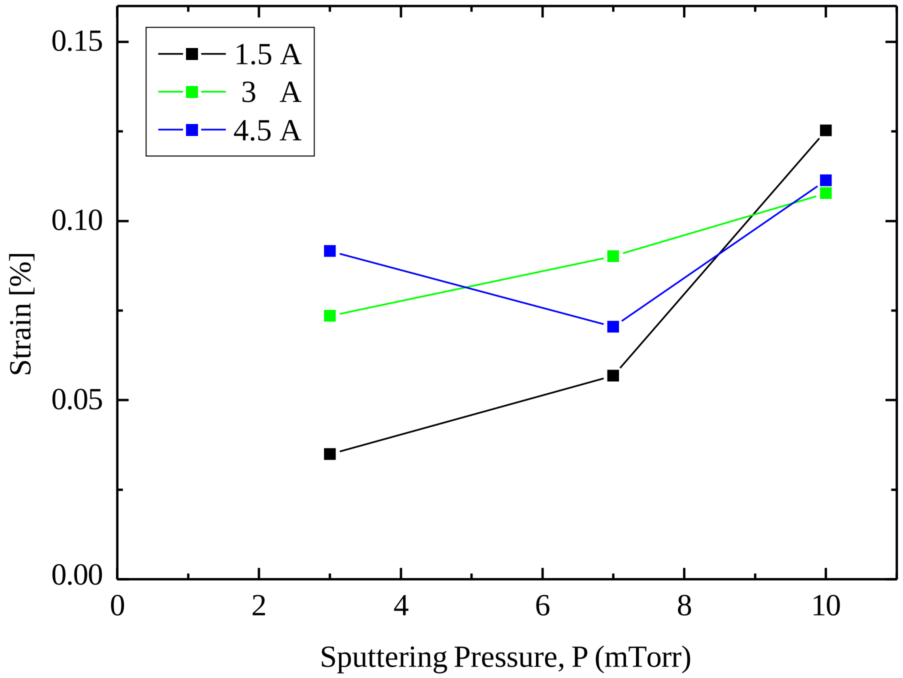

Figure 5-8: Lattice strain of Mo films as a function of sputtering pressure for sputtering currents of 1.5, 3 and 4.5 A.

5.3.4 Depth Profile Analysis

Some Mo films deposited on SLG were annealed in a tube furnace at temperature of 450 °C and 550 °C backfilled with 10 mbar of Ar after evacuating to

10^{-3} mbar to observe the effect of temperature increase on the Mo back-contact and the Na content.

Qualitative SIMS measurements were performed to assess the Na content in the deposited Mo layers and representative scans are shown in figure 5-9 for as-deposited and post annealed films. An average intensity across the film thickness was calculated at the three different Ar pressures and sputtering currents (figure 5-9). These data were normalised with respect to the Mo film at intensity of 1000 cps to be able to compare the Na intensity before and after annealing. The thicknesses of Mo films were ~ 1 µm; therefore, it was also normalised with respect to 1 µm to eliminate further errors.

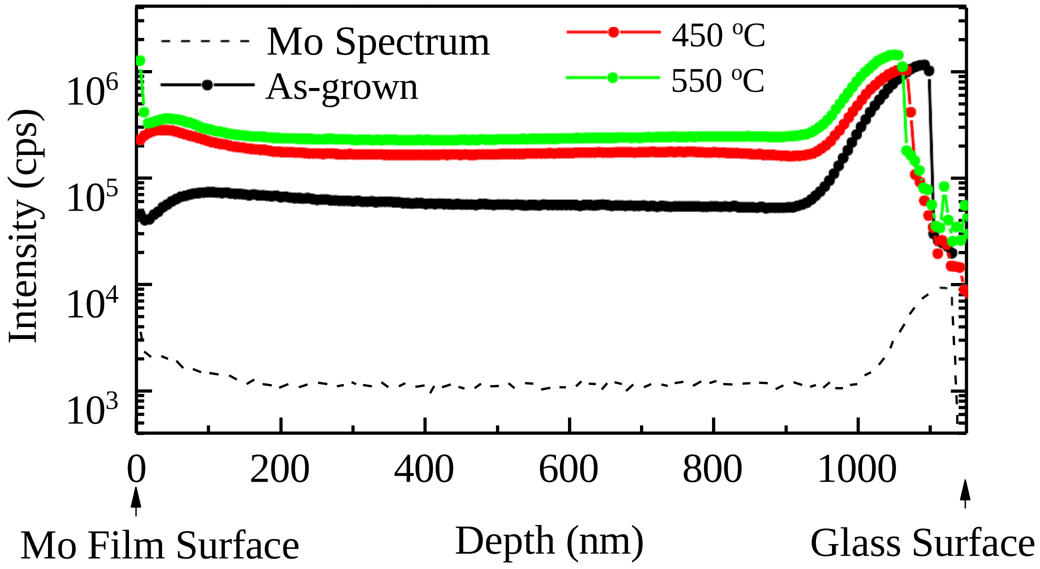

Figure 5-9: Na SIMS depth profiles in Mo films deposited at 10 mTorr and 4.5 A on SLG. The data has been normalised with respect to the Mo signal (dashed line).

The average intensities before annealing are plotted as a function of sputtering power in figure 5-10. It is shown that as sputtering power increases the Na content does not vary significantly; however, the Na content decreases as the sputtering pressure increases. In the as-deposited state, the Na content does not vary significantly with changes in pressure (figure 5-10 and figure 5-11) however a small reduction in Na is seen as the sputtering pressure increases for higher sputtering power (figure 5-10).

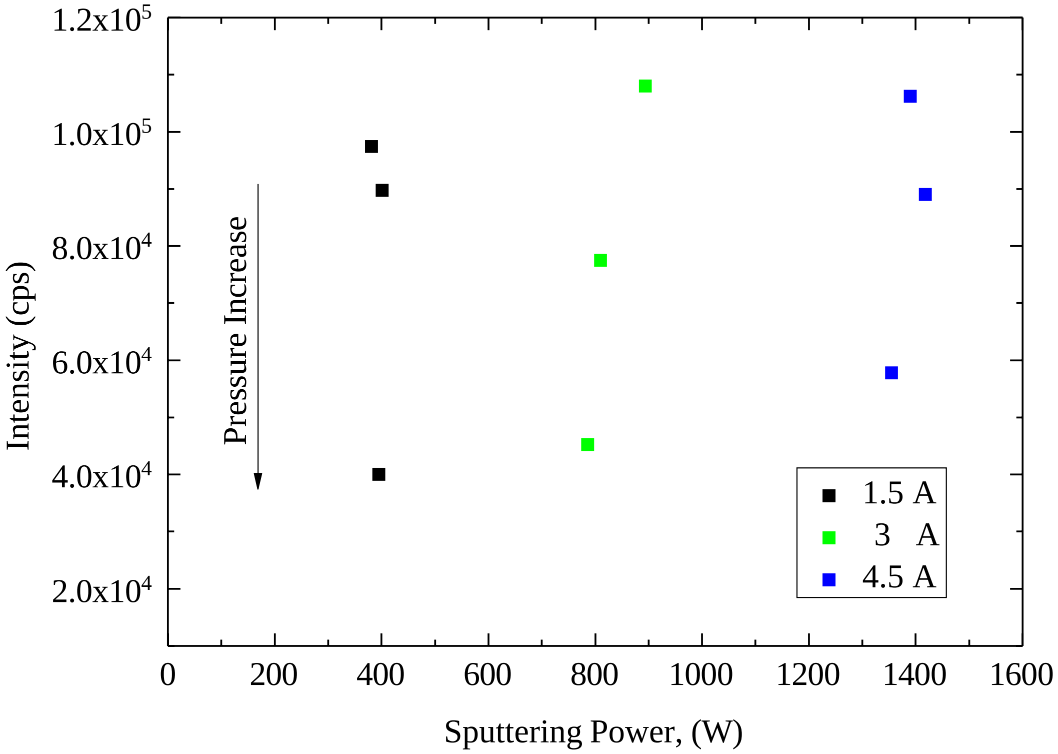

Figure 5-10: SIMS analysis for Na content on the Mo films at sputtering currents of 1.5, 3 and 4.5 A and sputtering pressure of 3, 7 and 10 mTorr before annealing.

Figure 5-11 also displays the resistivity of the as-grown layer and although the parameters investigated here do not produce broad changes in resistivity (see for example [184]) there is a clear relationship between the Na SIMS intensity and film resistivity on all three series of samples: at a given sputtering power, an increase in resistivity yields a lower Na diffusion in the Mo film (dashed and solid black lines, respectively in figure 5-11). In general sputtering of Mo at lower Ar pressure yields denser films with less voids and porous grain [179] thus reducing the film resistivity as mentioned earlier. More interestingly is the fact that Na content in the as-deposited Mo film increases at lower pressure indicating that Na diffusion from the glass is greater for denser films.

Figure 5-11 also includes the Na intensity after heat treatment at 450 °C and 550 °C to mimic the range of CdTe post-deposition chloride treatments used to fabricate state-of-the-art solar cells. As expected it was observed that the Na content increases as the annealing temperature increases due to out-diffusion from the SLG substrate. At the lowest deposition current (figure 5-11 a), the Na content has a decreasing trend with sputtering pressure following annealing. At a deposition current of 3 A, saturation is observed as sputtering pressure increases.

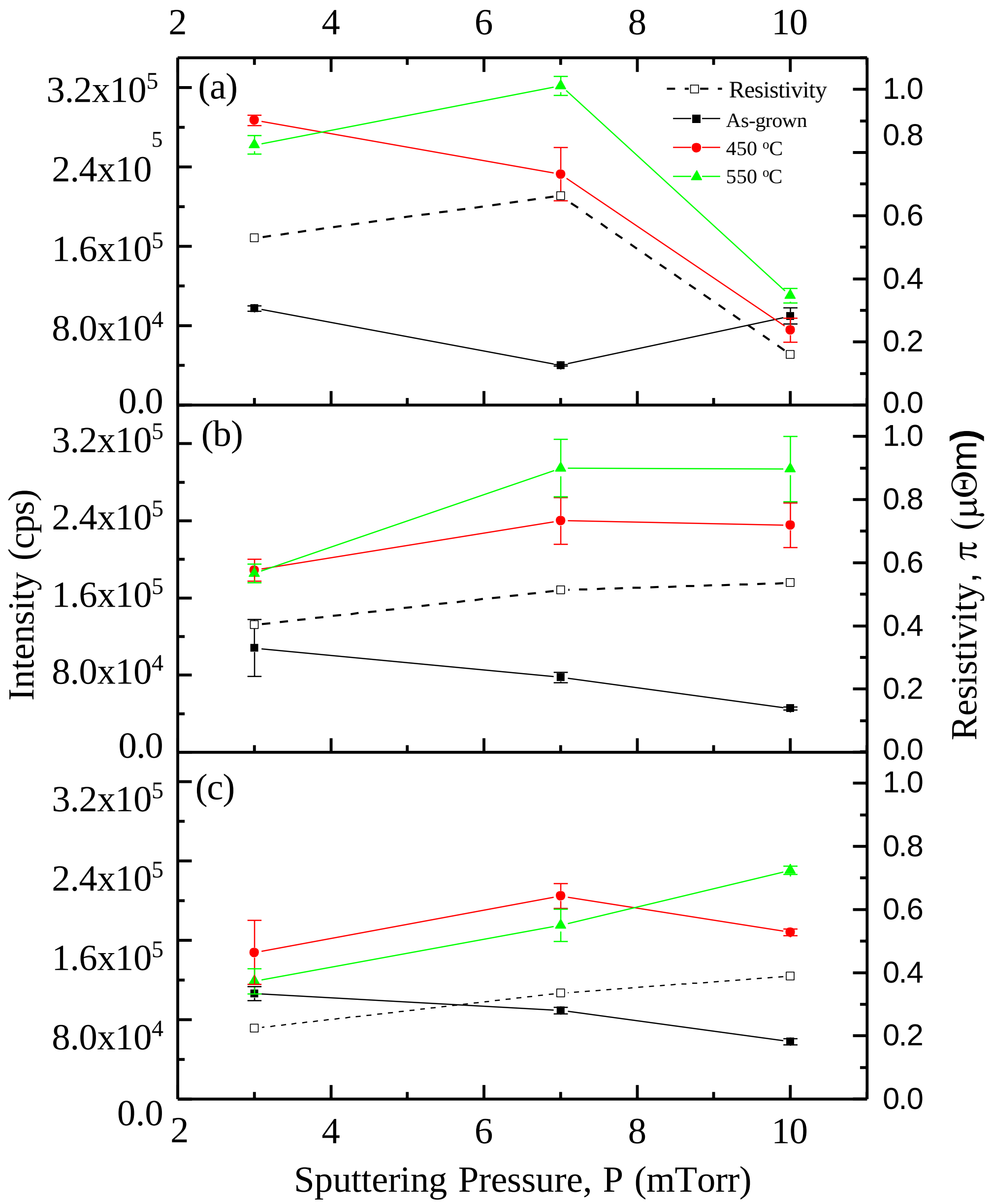

Figure 5-11: SIMS analysis (filled symbols and solid lines) for Na content in the Mo layer at different annealing temperatures at sputtering current of (a) 1.5 A (b) 3 A (c) 4.5 A. The resistivity plots of the as-grown layers are also shown (open symbols and dashed lines). The lines are a guide to the eye.

5.4 Mo Back-Contact Performance

The Mo back-contact films were used in CdTe devices to observe the effect of Na content in the SLG. Arsenic doped CdTe thin films were grown by MOCVD on

Mo coated quartz and SLG substrates in a horizontal reactor, using purified H_2 as the carrier gas and with a growth temperature of 390 °C as described in detail earlier in chapter 4. When necessary, the $CdCl_2$ activation treatment was carried out in situ immediately after the growth of the CdTe film. The samples were further processed into PV devices by depositing the CdS, TCOs and front contact layers. The complete device fabrication procedures are defined in section 4.1. Each substrate was defined by mechanical scribing into nine 0.16 cm^2 devices.

Film delamination can result in solar cell performance degradation and device failure. Even though the same deposition conditions were used to deposit the Mo films on both quartz and SLG substrates, the poor adherence of the Mo films to the SLG substrate caused the films to delaminate (figure 5-12 a). Therefore, for device fabrication only quartz substrates were used.

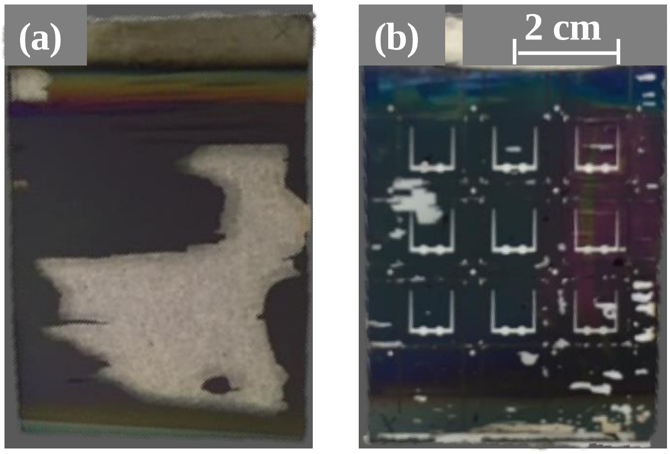

Figure 5-12: Delaminated Mo films deposited with of 10 mTorr and 3 A sputtering conditions (a) on SLG after CdS deposition or (b) on quartz (complete device) after annealing at 550 °C for 30 min.

An efficiency of 0.75 % was measured before annealing for a device with sputtering conditions of 10 mTorr and 3 A, on quartz without $CdCl_2$-treatment. This device has low electrical results of u_{vb} = 240 mV and Y_{ab} = 8.40 mA/cm^2 (table 5-5) as expected for untreated CdTe. The back-contact is formed early in the process for devices with substrate configuration, therefore it is important for it to withstand temperature in processes up to ~ 500 °C. Therefore, the device was annealed at 550 °C for 30 min to mimic the activation step. The overall efficiency was reduced as shown in table 5-5. Even though, annealing should lead to better electrical properties [70], poor results were measured due to the cracks and delamination formed after annealing on the device after annealing (figure 5-12 b). The results show that the Y_{ab} increased from 8.40 to 9.82 mA/cm^2; however, there is a decrease of 100 mV in the u_{vb} . The low electrical results are likely due to fabrication process not being optimised and no activation step. The curves in figure 5-13 show the *J–V* characteristic of the device where a cross-over is observed for the curve under illumination and dark before annealing.

Table 5-5: PVs parameters for the device with and without $CdCl_2$-treatment. The Mo film was deposited with the following sputtering conditions: 10 mTorr; 3 A; before and after annealing. (Peak data average).

	η	Y_{ab}	u_{vb}	*FF*
	(%)	(mA/cm^2)	(mV)	(%)
Without $CdCl_2$-treatment				
Before annealing	0.75	8.40	240	37
After annealing	0.50	9.82	150	34
With $CdCl_2$-treatment				
Before annealing	4.35	14.90	557	52

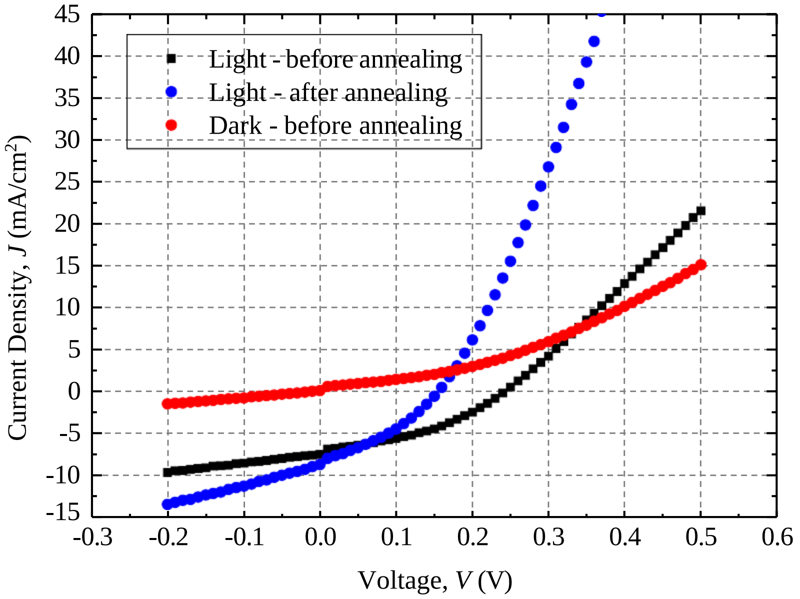

Figure 5-13: *J–V* curve for fabricated device with Mo film sputtering conditions of 10 mTorr and 3 A on quartz substrate under illumination before annealing, dark before annealing and under illumination after annealing at 550 ˚C for 30 min (the step at the zero intercept is an instrument error).

A device with $CdCl_2$-treatment was prepared; table 5-5 summarizes the effect the addition of $CdCl_2$-treatment has on the electrical properties of the device before annealing. It is observed that all the electrical properties of the device have been improved significantly. The overall efficiency of the device when treated by chloride has increased to 4.35 %, with Y_{ab} and u_{vb} of 14.90 mA/cm^2 and 557 mV respectively. Existence of $CdCl_2$ causes grain growth (figure 5-14 b), recrystallization and enhances the *p*-type conductivity of CdTe [154, 188]. The effect of grain growth is further explored in chapter 6.

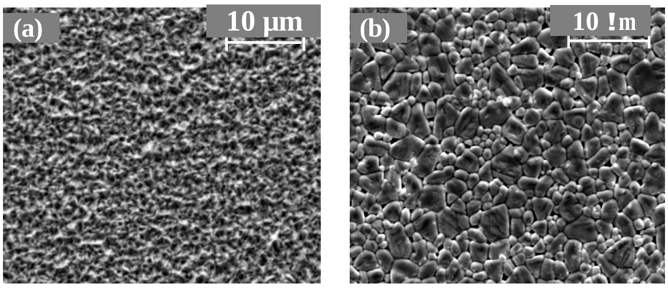

Figure 5-14: SEM micrographs for CdTe samples with Mo film deposited on quartz substrate with sputtering conditions: 10 mTorr; 3 A (a) without $CdCl_2$-treatment and (b) with $CdCl_2$-treatment.

The *J–V* and L¥L curves for the Cl-treated devices are shown in figure 5-15 where a roll-over and cross-over are observed. Roll-over phenomenon occurs when the current increases very slowly with increasing voltage near the u_{vb}; meanwhile the illuminated and dark *J–V* curve cannot overlap after translation due to the negative direction junction which is referred to as cross-over phenomenon. The L¥L curve shows the typical top-hat shape characteristic of a heterojunction cell. At photon energies, greater than the CdS bandgap (< 520 nm), optical absorption in the window layer reduces the number of photos penetrating through to the depletion region. Before the cut-off at 830 nm which corresponds to the energy bandgap of the CdTe absorber layer there is a slope between 600 and 800 nm. Back-contact issues result in a curve distortion, called the roll-over effect, reducing electrical performance. When roll-over and cross-over occur together as shown in the *J–V* curve in figure 5-15 a is generally due to a minority carrier recombination at a back-contact junction [1].

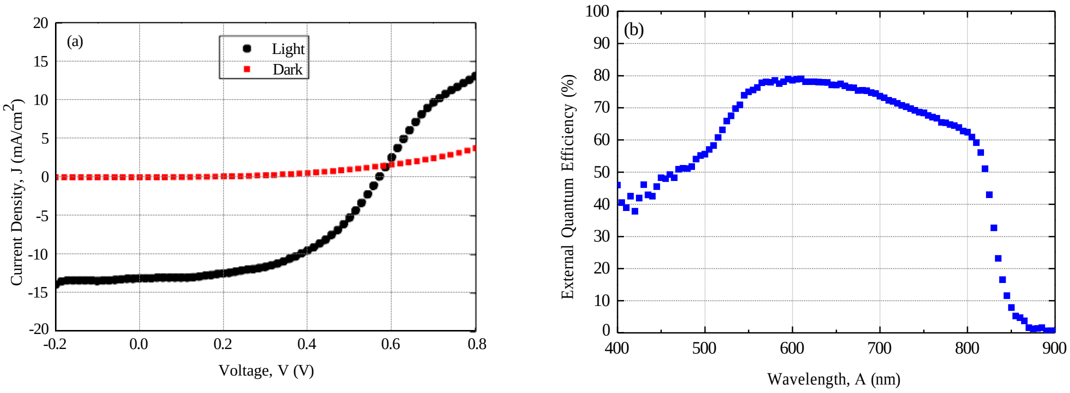

Figure 5-15: (a) *J–V* curve and (b) Ø“Ø for a device prepared on quartz substrate in under illumination and dark post-$CdCl_2$ activation step with Mo film conditions of 10 mTorr and 3 A.

Detailed analysis of the *J–V* behaviour for the curve in figure 5-15 a was done to characterise the diode behaviour and identify the possible cause of the reduced performance of the device. The data may be described by a standard diode model with the forward diode current limited by Shockley Read Hall recombination states within the space-charge region [191]. The *J–V* behaviour of a thin film solar cell can be described by a general single exponential diode equation [192]:

$$\mathrm{Y} = \mathrm{Y_g}\left[\acute{\mathrm{E}}^{\left(\frac{\mathrm{ü(†V≤ö>)}}{\mathrm{NFq}}\right)} - 1\right] + \frac{\mathrm{u} - \mathrm{Ym_r}}{\mathrm{m_{rE}}} - \mathrm{Y\_} \qquad \textbf{(5-5)}$$

where $\mathrm{Y_g}$ is the reverse saturated current density, *A* is the diode quality factor, $\mathrm{Y\_}$ is the light generated current density, $\mathrm{m_r}$ is the series resistance and $\mathrm{m_{rE}}$ is the shunt resistance. It is difficult to determine accurate diode parameters for thin film solar cells especially under illumination conditions. The *A* and $\mathrm{m_r}$ terms are particularly hard to determine as both have similar effects on the shape of the Y–*V* curve, vary with illumination intensity and other possible shunting effects, current limiting effects and changes in collection efficiency which affect the analysis but are not easily quantified. In this study the $\mathrm{m_r}$ and $\mathrm{m_{rE}}$ are assumed to be constants, i.e. the series and shunt terms are ohmic. Also, $\mathrm{Y\_}$ can be voltage dependent, however it is needed that the light generated current is constant and is approximated to the $\mathrm{Y_{rP}}$ ($\mathrm{Y\_} = \mathrm{Y_{rP}}$).

The practical procedure to verify the behaviour of the device and to determine the diode parameters is to use a set of four successive plots, each comparing data measured both in the dark and under illumination. The first plot is a standard Y–*V* curve with sufficient data showing the effects of roll-over and cross-over (figure 5-16 a). The second plot is the derivative $\mathrm{åY/åu}$ against *V* near $\mathrm{Y_{rP}}$ and in reverse bias where the derivation of the diode term in equation 5-5 becomes negligible. Since $\mathrm{m_{rE}}$ is ohmic and $\mathrm{Y\_}$ is constant then $\mathrm{åY/åu}$ will be flat with the value in reverse bias equal to $\mathrm{1/m_{rE}}$ (figure 5-16 b). The $\mathrm{m_r}$ and A are determined by differentiating the diode equation resulting in the relation [192]:

$$\frac{\text{åu}}{\text{åY}} = \mathrm{m}_{\mathrm{r}} + \frac{\mathbf{]Zt}}{\mathbf{l}}\left(\mathrm{Y}+\mathrm{Y}_{-}\right)^{\mathrm{V\Pi}} \quad \textbf{(5-6)}$$

A linear fit to the data gives an intercept of m_{r} and a slope $]\mathrm{Zt}/\mathrm{l}$ from which A can be calculated (figure 5-16 c). A correction factor can be made for the case in which $1/\mathrm{m}_{\mathrm{rE}}$ is not negligible. For the final plot, a semi-logarithmic plot (figure 5-16 d) of $\mathrm{Y} + \mathrm{Y}_{\mathrm{rP}}$ against $\mathrm{u} - \mathrm{Ym}_{\mathrm{r}}$ using the value for m_{r} can be obtained from figure 5-16 c. The intercept then gives $\mathrm{Y}_{\mathrm{g}}$and the slope in this case equals to $\mathrm{l}/]\mathrm{Zt}$ where A can be calculated and compared with the value from the previous plot. The diode parameters obtained from this device is shown in table 5-6. The large value of *A* suggests that the device is dominated by recombination current. An increase in m_{r} is undesirable, as it raises the barrier for the current extraction, also a reduction in m_{rE} is a result of higher recombination within the device.

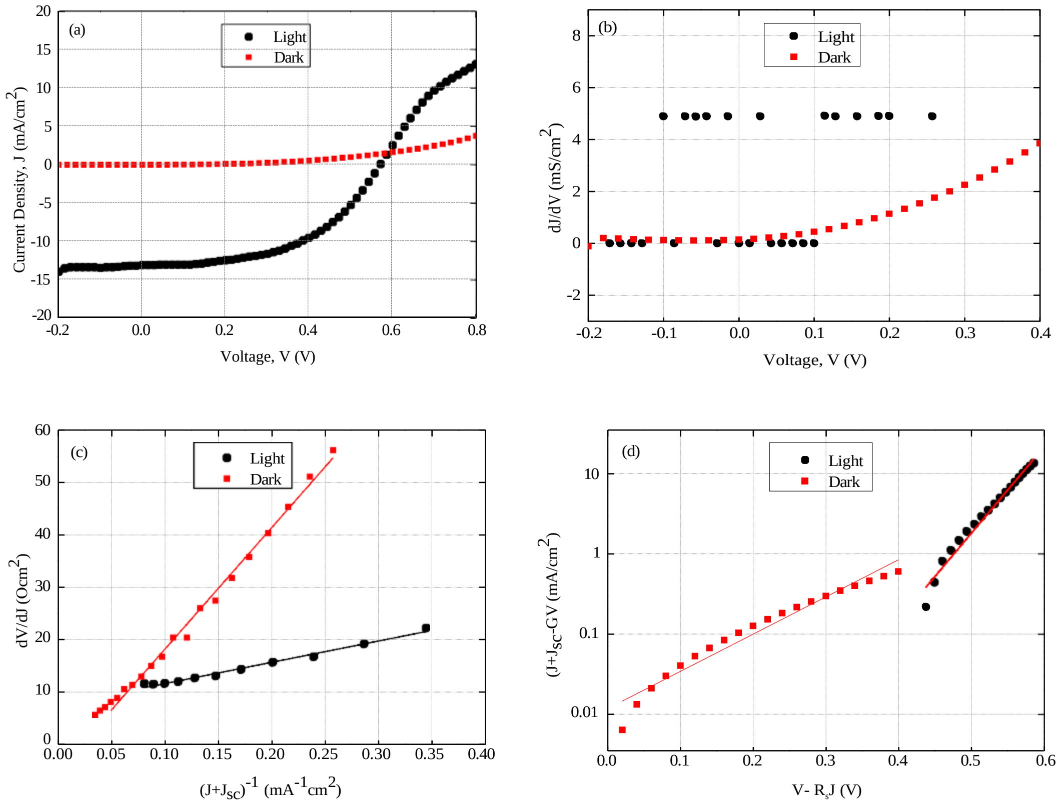

Figure 5-16: The *J–V* characteristics for the CdTe device prepared on quartz substrate under illumination and dark post CdCl₂ activation step (a) standard *J–V* curve, (b) shunt characterisation (”‘/”’), (c) ”’/”‘ with a linear fit to determine ÷û and *A*, (d) ◊ÿ (‘ + ‘ûŸ) with a linear fit to determine ‘/. The Mo film conditions of 10 mTorr and 3 A.

Table 5-6: Diode performance parameters for the highest CdTe device with λλ = 4.35 %.

	Dark	Illumination
Ɣg(?]/K?ᴵ)	1.1×10^{VI}	$3.1\times10^{V\neg}$
A	7.65	1.58
mr(0*cm*^{2})	1.07	7.60
mrE(0*cm*^{2})	5718	255

5.4.1 Mo Back-Contact Efficiency Analysis

Mo films prepared at high sputtering pressure of 10 mTorr showed better adhesion and lower resistivity compared to the samples prepared at lower sputtering pressures. Keeping the sputtering pressure constant at 10 mTorr the sputtering current was varied from 1.8 – 4.5 A to understand the effect power has on overall performance of the device. Table 5-7 shows the electrical properties of the devices prepared with varying sputtering current and constant sputtering pressure. The results show that with increasing sputtering current of 1.8, 3 and 4.5 A the Y_{ab} increases from 10.65, 12.18 to 15.26 mA/cm^2, respectively. On the other hand, with sputtering current increased the u_{vb} increased from 529 to 557 mV before decreasing to 243 mV. The device with a sputtering current of 3 A shows the highest overall efficiency of 4.35 %. The *J*–*V* curves for these devices show poor characteristic (figure 5-17).

Table 5-7: PVs parameters for samples where the Mo film was deposited with the following sputtering conditions: 10 mTorr; 1.8, 3, 4.5 A. (Peak data average).

Sputtering Current, *I* (A)	η (%)	Y_{ab} (mA/cm^2)	u_{vb} (mV)	*FF* (%)
1.8	3.09	10.65	529	55
3	4.35	14.90	557	52
4.5	1.01	15.26	243	25

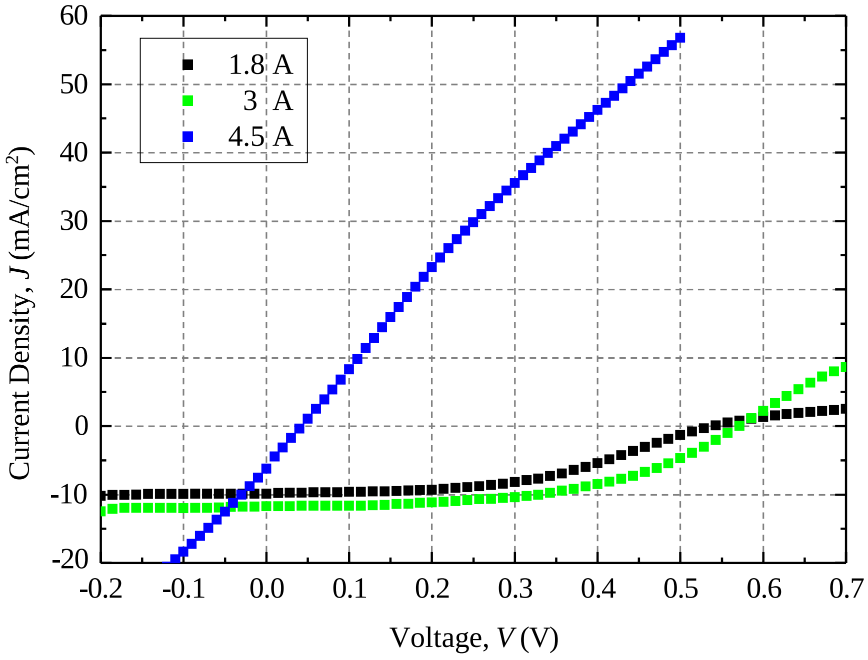

Figure 5-17: *J–V* curve for fabricated device with Mo film sputtering conditions of 10 mTorr and1.8, 3 and 4.5 A on quartz substrate under illumination.

5.5 Conclusion

This chapter focused on optimizing the Mo back-contact layer to achieve a film with low resistivity and good adherence to the substrate. The Mo films obtained a low resistivity ranging between 20 – 60 μΩm for samples of the same thickness (~ 1.0 μm). The films deposited using high sputtering current of 4.5 A had low resistivity and films deposited at lower sputtering current of 1.5 A had a higher resistivity.

The overall performances of the Mo films were investigated by fabricating the CdTe devices by an MOCVD technique. The aim was to fabricate cells with good electrical properties that do not delaminate at high temperatures. Efficiency of 4.35 % was achieved for a sample with Mo film deposition conditions of 10 mTorr and 3 A (on quartz substrate) with $CdCl_2$-treatment. The u_{vb} and efficiency of the devices were decreased by 56 % and 76 % respectively, with respect to increasing sputtering current to 4.5 A.

The depth analysis of the Mo films on SLG showed that as sputtering current increased the Na content did not vary significantly; however, the Na content decreases as the sputtering pressure increased. There is a lack of literature on the role of Na and its effect on CdTe absorber layer. Therefore, the Na content will be investigated by intentionally adding a NaF layer before and after the Mo film by thermal evaporation technique. The next chapter focuses on characterisation of CdTe absorber layer as a function of Na content before and after intentionally adding a NaF layer. The next chapter also investigates the effect of replacing the $CdCl_2$ layer with $MgCl_2$.

CHAPTER 6

6 The Combined Effect of Na and Cl on the CdTe Layer

This chapter focuses on the role of Na and Cl in CdTe thin film photovoltaic absorber deposited on Mo substrates using MOCVD. After a brief introduction (section 6.1), section 6.2 describes the approach to achieving Na diffusion through the as-grown CdTe layer and post $CdCl_2$-treatment as well as the introduction of $MgCl_2$ deposited by a solution method to replace $CdCl_2$. Section 6.3 follows by characterising the layer's morphology, structure and chemical composition.

6.1 Introduction

CdTe is normally deposited on SLG and generally includes barrier layer(s) such as Si_3N_4, Al_2O_3 or SiO_2 to prevent diffusion of impurities from the glass [48, 193, 194]. Na, a major constituent of SLG, is known to diffuse during thermal processes > 300 °C and has been shown to promote uncontrolled grain enlargement in CdTe deposited using vacuum evaporation [48–50]. Impurities and dopants play a major role in PV devices and prime examples are Cl in CdTe and Na in CIGS solar cells. Cl is fundamental to the "activation" of the CdTe film while Na affects grain size, crystal texture and conductivity in CIGS [195, 196]. The presence of Na in CdTe solar cells can result in increased grain size of the absorber layer, increased acceptor density and u_{vb} as it acts as a shallow acceptor in CdTe with low activation energy [48, 193, 197, 198]. The increase in CdTe grain size is still paramount to reducing the volume of grain boundaries and defect concentration to increase device efficiency, and the role of Na merits further investigations.

For CdTe films grown by MOCVD on SLG, an uncontrolled grain enlargement can be resulted, as demonstrated next. Figure 6-1 shows the SEM surface micrographs of $CdCl_2$-treated CdTe films deposited by MOCVD on Mo-coated quartz and SLG substrates. When deposited on quartz (figure 6-1 a) the CdTe grains are small (~ 0.5 μm) and compact whereas when deposited on SLG, grains grow larger (up to 5 μm) but the CdTe film is no longer continuous (figure 6-1 b), creating possible shunting paths in the solar cell structure, likely reducing its output power. It is therefore advantageous to adequately control grain growth while maintaining film continuity.

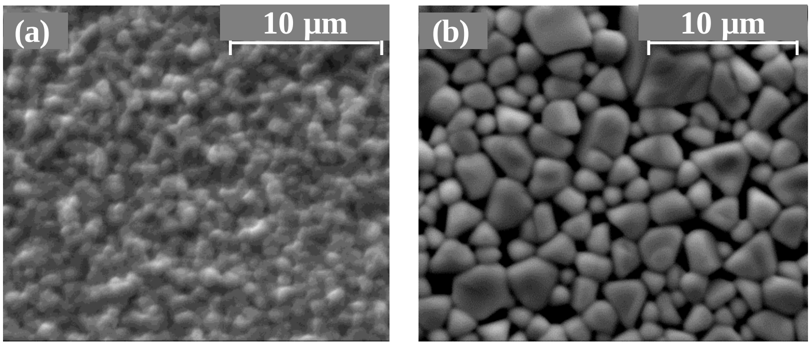

Figure 6-1: SEM micrographs of $CdCl_2$-treated Mo/CdTe films deposited on (a) quartz and (b) SLG substrates (SEM images courtesy of G. Zoppi, Northumbria University).

From the results presented in chapter 5, it is difficult to predict the out-diffusion of Na from the glass especially when one considers the inhomogeneous concentration of constituents in SLG and a more robust approach was chosen, focusing on samples deposited on quartz substrate with an intentionally added NaF layer. Therefore, this study investigates the morphological and structural properties of CdTe grown by MOCVD when NaF is introduced. As well as considering the Na diffusion, this study investigates an alternative Cl-treatment by introducing $MgCl_2$.

6.2 Layer Properties

Mo thin films were deposited on quartz substrates using DC magnetron sputtering with target currents of 2, 3 and 4.5 A, at room temperature and at Ar sputtering pressures of 3, 7 and 10 mTorr whilst rotating at a speed of 2.5 or 5 rpm. $MgCl_2$ was deposited by a solution method as described in chapter 4. Apart from the Cl-treatment step, all other device processing steps were identical to the previous studies unless otherwise stated. The deposition parameters and other film thicknesses for this study are listed in table 5-1.

Table 6-1: Process parameters for the deposition of the Mo films and layer thicknesses.

DC-magnetron Sputtering Conditions	
Mo Target size (cm^2)	330
Substrate	Quartz
Temperature	Room temperature (RT)
Substrate rotation speed (rpm)	2.5; 5
Base pressure (Torr)	7×10^{-6}
Sputtering current (A)	2; 3; 4.5
Ar Sputtering pressure (mTorr)	3; 7; 10
Deposition time (min)	40 – 60
Mo thickness (nm)	1000
NaF thickness (nm)	10
CdTe thickness (nm)	2750

In order to investigate the influence of Na on the properties of the CdTe films, three different sample layouts were prepared using quartz substrates: (i) CdTe/Mo/quartz, (ii) CdTe/Mo/NaF/quartz and (iii) CdTe/NaF/Mo/quartz where NaF, ~ 10 nm was deposited by thermal evaporation at room temperature. Two chloride process variations were compared: (1) the standard $CdCl_2$-treatment and (2) direct deposition of an $MgCl_2$ solution to the CdTe surface before annealing at 420 °C for 20 min.

6.3 Results and Discussion

This two-part results section discusses the effect of NaF addition before showing the effect of $MgCl_2$-treatment. The roughness and thicknesses were measured using a stylus profilometer. The morphology, structure and chemical composition were studied using XRD, SIMS and SEM.

6.3.1 Intentionally Added NaF Layer

Both Na and F have previously been investigated in CdTe superstrate devices with some success. Na is a shallow acceptor (Na_{Cd}) in CdTe [199], while F, like Cl, is a donor (F_{Te}). In the case of F, the literature reports investigations where F is used in conjunction with Cl as a replacement to $CdCl_2$ using CdF_2 [200] or HCF_2Cl [131]. The combined use of CHF_3 treated CdS and HCF_2Cl treated CdTe leads to efficiency as high as 15.8 % [201]. It is likely that both Cl and F are incorporated in the CdTe and demonstrates that F (along with Cl) can contribute to effective *p*-doping of CdTe via the formation of complexes [202]. Extrinsic doping of CdTe using NaF [193] and NaCl [193, 203] leads to degraded device performances due to excessive CdS-CdTe intermixing irrespectively of the halogen (Cl, F) species. The performance of the superstrate device can be maintained if the NaF layer is deposited at the back of the structure, *i.e.* after the CdTe deposition [48], likely protecting the *pn* junction from degradation. On the other hand, when the presence of Na in the structure is carefully controlled the open circuit voltage, a key limitation for CdTe technology, of the device can be improved owing to an increase in acceptor concentration. While a small drop in short circuit current due to a lower transmission of the SLG compared to Na-free glass results in a slightly lower overall efficiency [48, 111, 191]. The detailed chemical analysis by Emziane and co-workers [31, 33, 54, 202] provides further insights on the possible effects of both F and Na. Firstly, when originating from the CHF_3 plasma used in the sputtering of the CdS layer ($[F]=10^{17}$ at/cm^3 for the as-deposited CdS), F segregates at the surface of the CdTe post $CdCl_2$-treatment with a SIMS signal in the absorber itself equal to the background detection limit. Secondly, Emziane found a significant amount of Na to be present in CdTe devices (up to 10^{18} at/cm^3) even when using Na-free substrate and this is due to the large concentration of impurities in the raw $CdCl_2$ powder material.

In the case of CIGS, the rate of Na diffusion from the SLG substrate into the absorber is dependent on the Mo properties themselves [183] and it is expected that similar behaviour should occur in a CdTe thin film deposited on Mo/SLG. In order to optimise the Mo film layer, the influence of sputtering pressure and power (sputtering current) on Na diffusion in Mo films through SLG substrate were first explored (chapter 5). The use of Na, or NaF, is yet to be explored in substrate configuration and this section provides new insights on the effect of NaF on MOCVD-grown CdTe deposited on quartz substrates.

6.3.1.1 Morphology Analysis

Figure 6-2 shows the impact of NaF (~ 10 nm) on the surface morphology of MOCVD-grown CdTe films for the as-gown and $CdCl_2$-treated samples with the following layout: CdTe/Mo/(NaF/)quartz. The micrographs were analysed using the Gwyddion software package to determine the grain size (grain pixel area modelled to a circular shape) distributions and were fitted to a Rayleigh function to obtain average values. Throughout the text “grain size” refers to the diameter of the modelled grain.

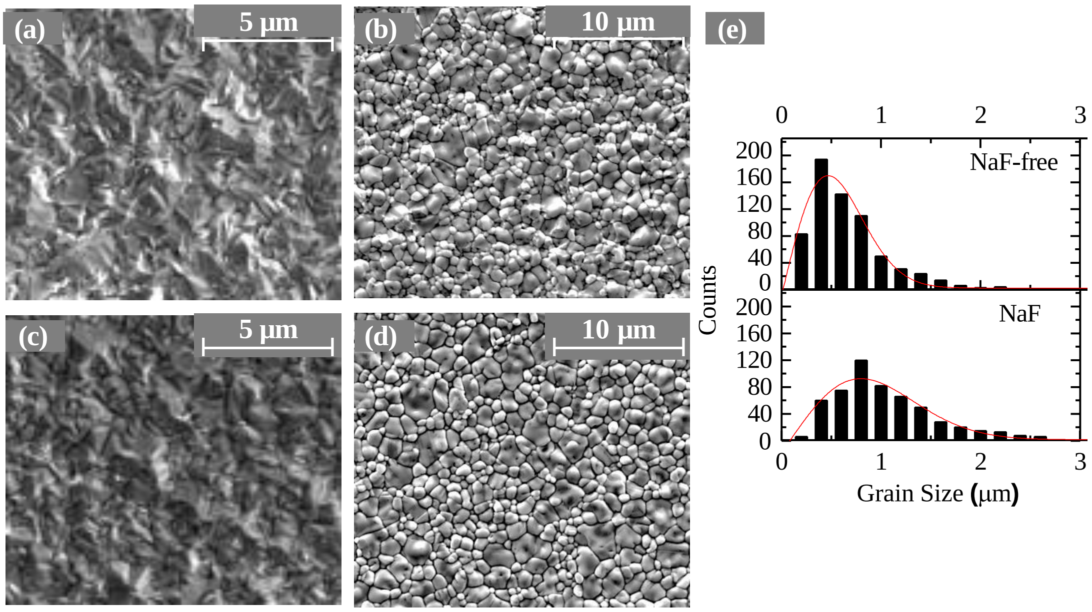

Figure 6-2: SEM micrographs of CdTe thin films with the following configurations: (a, b) Na-free (CdTe/Mo/Quartz), (c, d) CdTe/Mo/NaF/quartz with (a, c) as-grown and (b, d) $CdCl_2$-treated samples. The Mo film was deposited with the following sputtering conditions: 10 mTorr, 3 A and 5 rpm. Grain size (diameter) distribution histograms are shown in (e) for $CdCl_2$-treated films. Top: CdTe/Mo/quartz and bottom: CdTe/Mo/NaF/quartz.

In the as-grown state the grains show very small < 0.2 μm pyramid shaped structures (figure 6-2 a and c), with a marginal increase for the Na containing film (figure 6-2 c). Post $CdCl_2$-treatment, the grains become more rounded with less sharp faceted edges and a grain growth is observed as expected for MOCVD-grown CdTe thin films [187] (figure 6-2 b and d). The histograms in figure 6-2 e show the grain size distributions of the Cl-treated films. The average size for the film grown in the absence of NaF is 400 – 500 nm and 800 – 900 nm when a NaF layer is inserted in the structure.

The films prepared with the layout CdTe/Mo/NaF/quartz were not suitable for further possible processing due to delamination of the CdTe/Mo film during the *pn* junction formation trials (figure 6-3). This is due to the weak adhesion between Mo and NaF, where NaF dissolves in the aqueous solution during chemical bath deposition of CdS (figure 6-3 a).

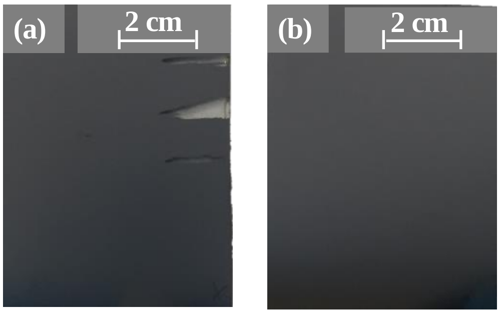

Figure 6-3: CdTe films deposited with the following sputtering conditions: 10 mTorr, 3 A and 5 rpm. The layouts were as follows: (a) CdTe/Mo/NaF/quartz (delaminated) and (b) CdTe/NaF/Mo/quartz, after CdS deposition.

A more robust approach is to deposit the NaF after the Mo back-contact deposition (figure 6-3 b) to preserve the strong adhesion between Mo and the substrate. Figure 6-4 shows the effect of Na on CdTe/NaF/Mo/quartz layout with varying Mo film sputtering pressure (3, 7 and 10 mTorr). Compared to the layout CdTe/Mo/NaF/quartz (figure 6-2 c), there is a clear morphological change: large faceted CdTe grains are formed in the presence of Na even in the as-grown state. Even though the addition of Na enhances grain growth it does not cause widening of grain boundaries unlike previous reports [193]. In the as-grown sample (figure 6-5 a) the CdTe grain size average is 1.9 μm at pressure of 3 mTorr and 1.6 μm for films deposited at higher pressure of 7 and 10 mTorr. The three sets of data showed broad distributions with grain sizes ranging between 0.5 – 4 μm. As with the previous example the $CdCl_2$ annealing step yields more rounded grains and smoother films: the root mean square roughness values of samples shown in figure 6-4 are 225 nm and 195 nm as-grown and post $CdCl_2$-treatment, respectively. On the other hand, the histograms in figure 6-5 b show a reduced average grain size of ~ 1 µm post $CdCl_2$-treatment with a narrower distribution regardless of the back-contact sputtering pressure. The cross-section images, also shown in figure 6-4, do not reveal measurable differences between the three sets of samples.

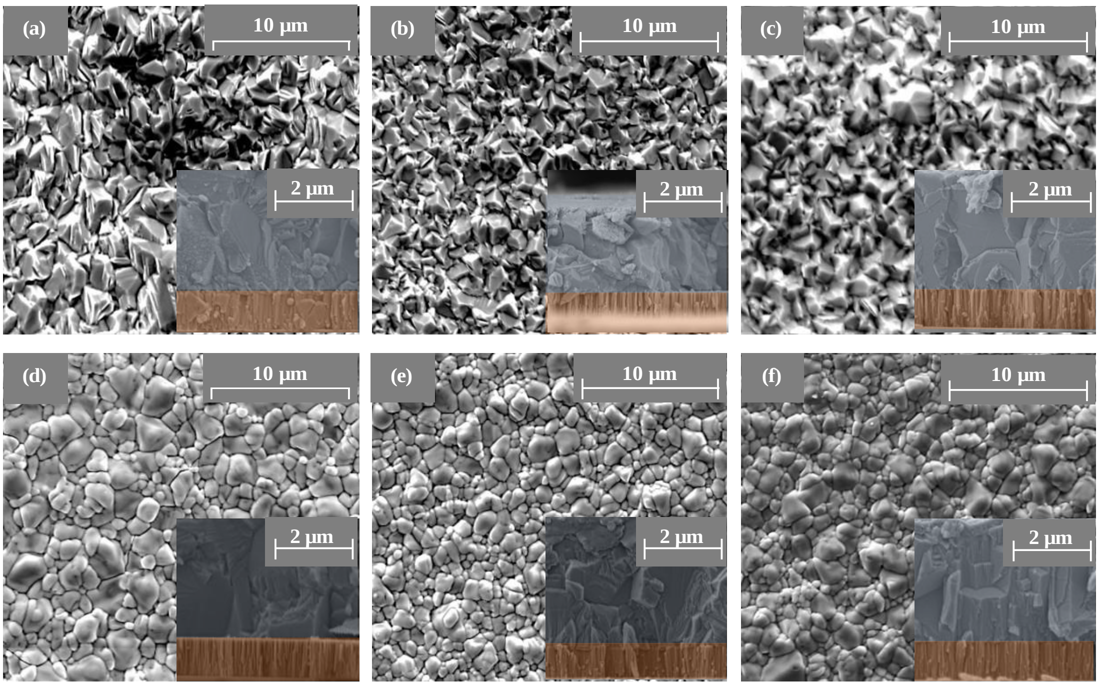

Figure 6-4: SEM micrographs of CdTe thin films as-grown (top row) or post $CdCl_2$-treatment (bottom row) deposited on NaF/Mo/quartz. The Mo film was deposited with the following sputtering conditions: (a, d) 3, (b, e) 7, (c, f) 10 mTorr; 3 A; 5 rpm.

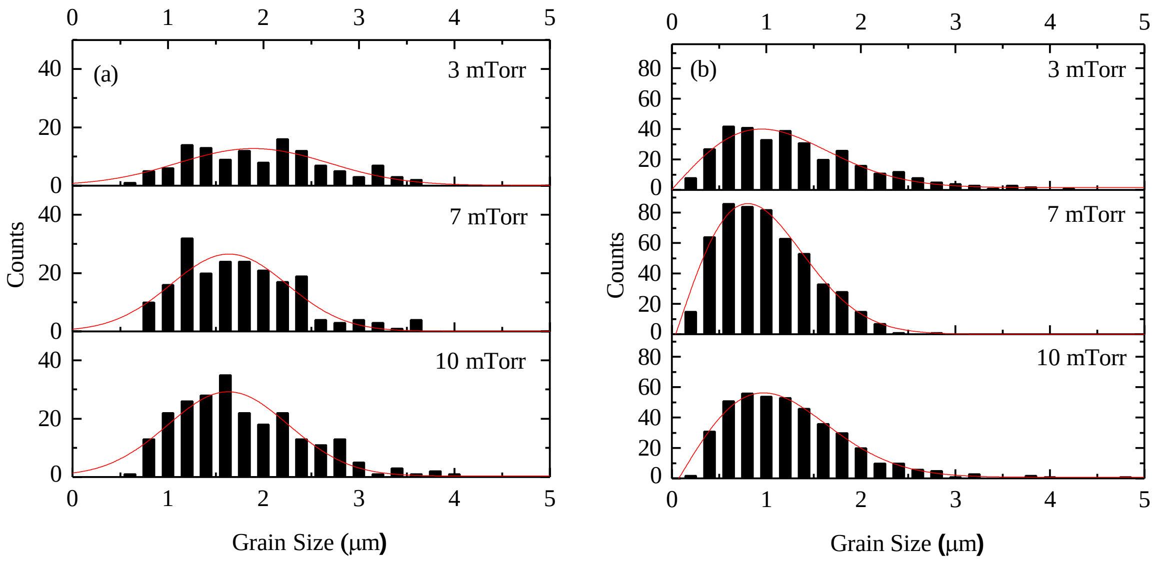

Figure 6-5: Grain size distribution of CdTe films as a function of Mo sputtering pressure for the layout CdTe/NaF/Mo/quartz. (a) as-grown and (b) $CdCl_2$-treated. Note the change of scale between (a) and (b).

Figure 6-6 shows the impact of NaF on the surface morphology of MOCVD-grown CdTe films with varying sputtering current and rotational speed of the as-grown and post $CdCl_2$-treatment samples with the layout of CdTe/NaF/Mo/quartz. The micrographs were analysed by manually measuring the grain size over a couple of parallel planes, this method was also tested for the samples in figure 6-5 and the same average grain size was estimated. Sputtering current and rotational speed do not change the morphology of large faceted CdTe grains which are formed in presence of NaF even in the as-grown state. In the as-grown state (figure 6-6 a, c) the pyramid shaped structures have an average size of > 1.3 μm. Post $CdCl_2$-treatment (figure 6-6), like samples in figure 6-2 b and d there is a grain growth where the grains are rounded with less sharp faceted edges. The consistency in the grain morphology proves reproducibility. For example, a sample deposited with a layer of NaF having sputtering conditions of 3 A and 10 mTorr has a grain size of 1.4 μm (figure 6-6 c) very similar to the previous batch (figure 6-4 c 1.6 μm). Even though post Cl-treatment (figure 6-6) the samples seem to have larger grains; statistically they are much less and therefore more similar in size to samples in figure 6-4 (note the change of scale between the two images). All the samples in table 6-2 showed a small variation of grain size average ranging between 1.3 – 1.9 μm indicating that sputtering current, pressure and rotational speed do not affect the grain size of the CdTe layer significantly. Also, the cross-section SEM images, shown in figure 6-6 do not reveal obvious differences in the sample's morphology.

Table 6-2: Average grain size for as-grown and $CdCl_2$-treated samples. The Mo film was deposited with the following sputtering conditions: 10 mTorr; 2, 3, 4.5 A; 2.5, 5 rpm.

Sputtering Current, *I* (A)	Sputtering Rotational Speed (rpm)	Grain Size (μm)	
		As-grown	**$CdCl_2$-treated**
2	2.5	1.4 ± 0.3	1.8 ± 0.1
3		1.4 ± 0.3	1.6 ± 0.1
4.5		1.5 ± 0.4	1.8 ± 0.2
2	5	1.3 ± 0.1	1.7 ± 0.3
3		1.4 ± 0.1	1.5 ± 0.2
4.5		1.7 ± 0.3	1.7 ± 0.2

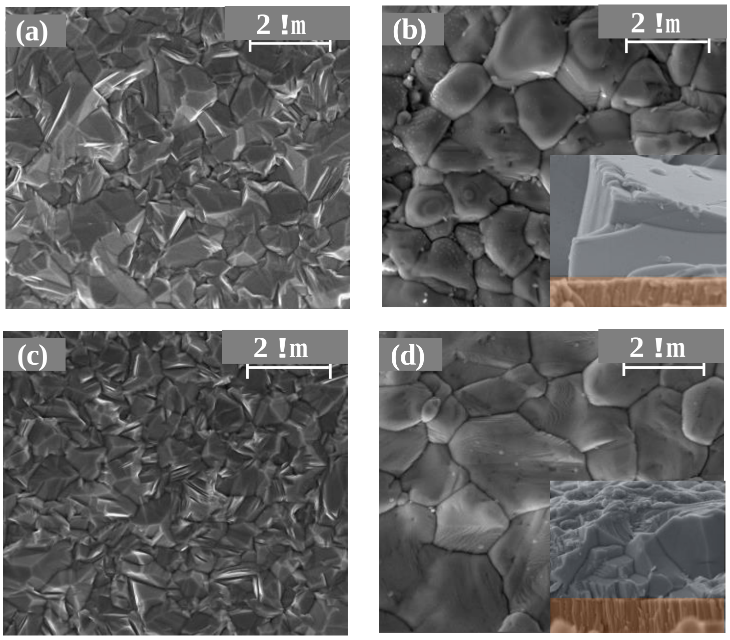

Figure 6-6: SEM micrographs for as-grown (left a, c) and $CdCl_2$-treated (right b, d) CdTe thin films deposited on NaF/Mo/quartz. The Mo film was deposited with the following sputtering conditions: 10 mTorr; 3 A; 2.5 rpm (top row), 5 rpm (bottom row).

6.3.1.2 Depth Profile Analysis

Na SIMS depth profiles are displayed in figure 6-7 a and b for the as-grown CdTe films deposited using the following configuration: CdTe/NaF/Mo/quartz and CdTe/Mo/NaF/quartz. An average count was calculated at the three different Ar pressures for each of the configurations and is shown in figure 6-7 c and d. The greatest Na content is seen at the lowest sputtering pressure (3 mTorr) for both configurations while for higher Mo film deposition pressures the Na profiles are of similar shape and intensity. The layout CdTe/Mo/NaF/quartz yields the greatest variations in Na as a function of sputtering pressure (figure 6-7 d) and this reemphasises the fact that the Mo film controls the rate of diffusion. Samples with configuration: CdTe/NaF/Mo/quartz have a more consistent Na diffusion and good layer adhesion (no delamination). Comparing the Na content for the films with the configuration of CdTe/NaF/Mo/quartz (figure 6-7 a and c) and their average grain size (figure 6-5 a), it is noticeable that the Na content is at its highest where the grain size is the largest (~ 1.9 µm). It is also noticed that there seems to be more Na diffusing into the Mo film at lower sputtering pressures.

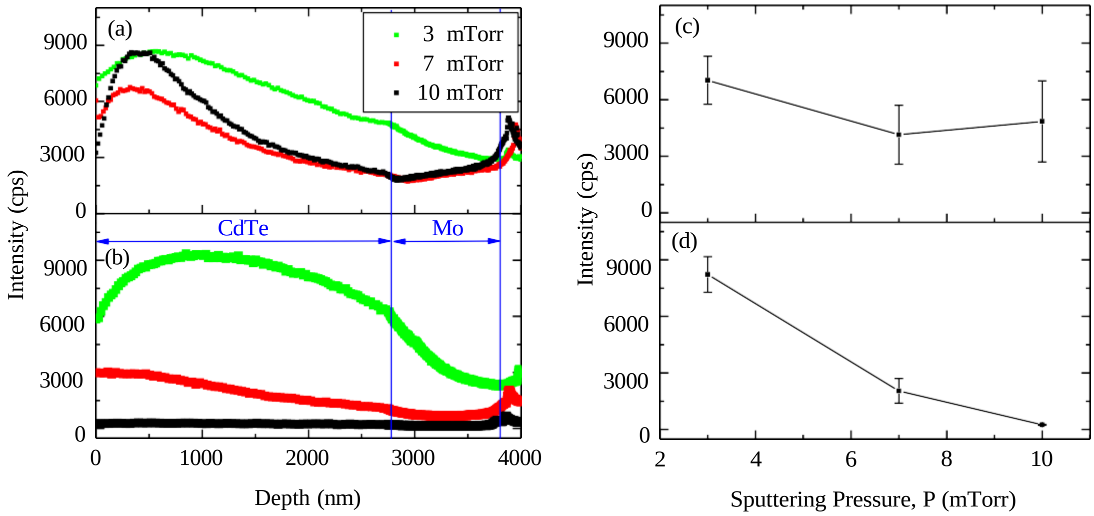

Figure 6-7: SIMS depth profiles showing the Na content in the as-grown CdTe thin films with the following layouts: (a) CdTe/NaF/Mo/quartz and (b) CdTe/Mo/NaF/quartz. The Mo film was deposited with the following sputtering conditions: 3, 7, 10 mTorr; 3 A; 5 rpm. The data was normalised against the Mo signal intensity. Note the linear scale on the intensity axis. The average counts in the CdTe layer are shown in (c) and (d), respectively.

6.3.1.3 Crystallographic Properties

X-ray diffraction was used to analyse the crystallographic properties of the deposited layers. For CdTe, the following peaks for the (111), (220), (311), (400), (331), (422) and (511) planes, which correspond to the diffraction angles of 23.76 °, 39.32 °, 46.43 °, 56.82 °, 62.35 °, 71.22 ° and 76.3 ° were observed for all the set of samples (figure 6-8). All CdTe samples have a face-centred cubic zinc blende structure. In addition to the listed peaks a reflection at 28 = 40.5 ° is observed (represented by "*") which corresponds to the (110) planes of the Mo substrate. Other Mo peaks are observed at 73.6 ° and 87.4 °. In both as-grown and $CdCl_2$-treated, the Na-free samples with layout CdTe/Mo/NaF/quartz display a very low intensity for (220), (400) and (331) peaks (i and ii in figure 6-8) in comparison with the sample CdTe/NaF/Mo/quartz (iii in figure 6-8). <111> is the dominant direction for all films.

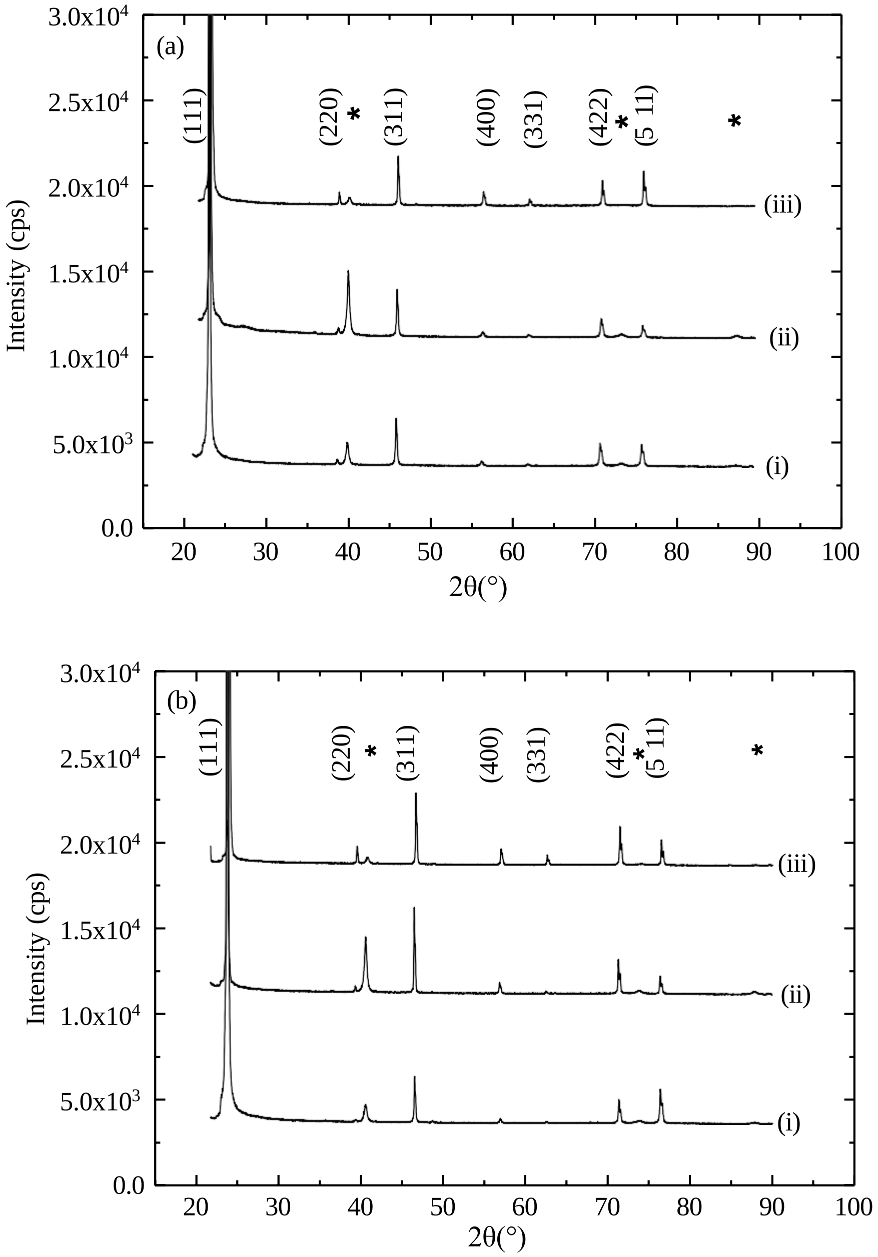

Figure 6-8: XRD patterns for (a) as-grown and (b) $CdCl_2$-treated samples with the following configurations: (i) Na-free, (ii) CdTe/Mo/NaF/quartz, (iii) CdTe/NaF/Mo/quartz. The Mo film was deposited with the following sputtering conditions: 10 mTorr; 3 A; 5 rpm. The peaks corresponding to the Mo film is marked by the asterisks.

The effects of growth conditions on texture and preferred orientation of the samples were investigated by calculating texture coefficient A_{EFG} and preferred orientation œ as explained in chapter 5. The œ values are used to compare the degree of orientation between different samples, so that lower œ values indicate more randomly oriented samples. The calculated σ values post $CdCl_2$-treatment for the Na-free samples ranged between 1.68 – 1.69 indicating less randomly oriented samples compared to the samples with Na that had a σ value ranging between 0.66 – 1.22 (table 6-3) for both as-grown and $CdCl_2$-treated samples. The σ values were randomly oriented for as-grown samples. The texture coefficient $A_{\prod\prod\prod}$ increases post $CdCl_2$-treatment for samples prepared without NaF; however, the opposite was observed when Na is present. Moreover, the decrease in $A_{\prod\prod\prod}$ correlates with an increase in $A_{\Sigma\wedge\wedge}$ and $A_{II\wedge}$. This shows an increased in crystallite orientation in the <400> and <220> directions for samples that have both NaF and $CdCl_2$ deposited even though the favoured preferred orientation of the films is still long the (111) plane.

Table 6-3: Texture coefficients and degree of preferred orientation for as-grown and $CdCl_2$-treated samples with the following configuration: CdTe/Mo/quartz and CdTe/Mo/NaF/quartz. The Mo film was deposited with the following sputtering conditions: 3, 7, 10 mTorr; 3 A; 5 rpm.

	Sputtering Pressure, P (mTorr)	Texture Coefficient, C_{hkl}							Degree of Preferred Orientation, σ
		C_{111}	C_{220}	C_{311}	C_{400}	C_{331}	C_{422}	C_{511}	
As-grown									
NaF	3	1.39	0.04	0.54	3.61	0.14	0.45	0.84	1.15
	7	3.94	0.08	0.39	0.63	0.20	0.55	1.20	1.25
	10	4.00	0.05	0.30	0.48	0.16	0.47	1.54	1.31
Na-free	7	3.05	0.06	0.19	0.99	0.57	0.62	1.52	0.95
	10	4.50	0.03	0.34	0.27	0.10	0.51	1.24	1.48
$CdCl_2$-treated									
NaF	3	3.76	0.05	0.28	0.59	0.18	0.56	1.58	1.22
	7	2.33	0.17	0.80	1.33	0.32	0.91	1.13	0.66
	10	2.86	0.08	0.56	0.71	0.29	0.93	1.57	0.88
Na-free	7	4.93	0.01	0.12	0.06	0.03	0.23	1.63	1.69
	10	5.02	0.01	0.22	0.16	0.06	0.36	1.17	1.68

Figure 6-9 b and c shows the texture coefficient of (400) and (220) peaks respectively, where it is clear that as the intensity of the C_{111} increases (figure 6-9 a), the intensity of the C_{400} and C_{220} decreases in accordance with the variation of preferred orientation. The Na-free sample shows an increase for C_{111} post $CdCl_2$-treatment.

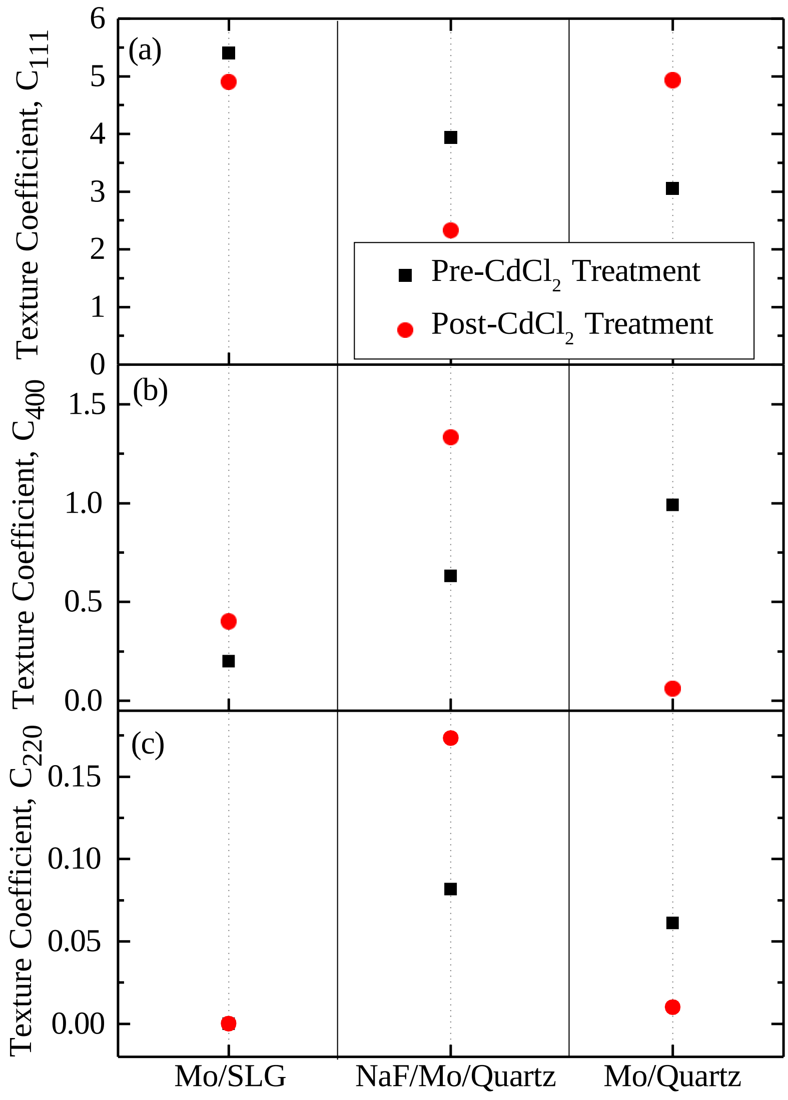

Figure 6-9: Texture coefficient values for (a) (111), (b) (400) and (c) (220) peaks plotted to show the variation of intensity with different deposition layers. The Mo film was deposited with the following sputtering conditions: 7 mTorr; 3 A; 5 rpm.

The FWHM of the (111) peak was used to determine the crystallite size via Scherrer formula [188]. The crystallite size was calculated and ranged between 67 – 83 nm (figure 6-10). As shown in figure 6-10 the crystallite size increases post $CdCl_2$-treatment for all samples. The samples with layout Mo/quartz and Mo/NaF/quartz have similar crystallite size for as-grown and $CdCl_2$-treated samples. Samples with layout NaF/Mo/quartz have larger crystallite size at sputtering pressure of 7 mTorr compared to samples with different layout deposited at the same sputtering conditions.

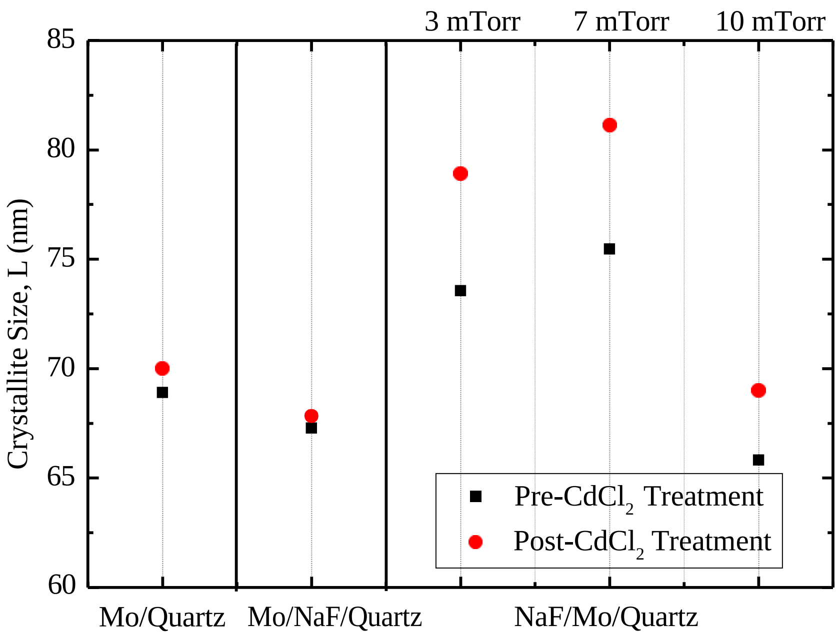

Figure 6-10: Crystallite size for as-grown and $CdCl_2$-treated samples. The Mo film for samples with layout Mo/quartz and NaF/Mo/quartz was deposited with the following sputtering conditions: 7 mTorr, 3 A and 5 rpm. The Mo film for samples with layout NaF/Mo/quartz was deposited with the following sputtering conditions: 3, 7, 10 mTorr; 3 A; 5 rpm.

6.3.2 An Alternative Cl-Treatment

Current studies and developments on CdTe thin films are aiming to reduce the cost of power generation to < 0.5 ¢ per watt [205] and to reduce the environmental influence. One of the main developments in CdTe solar cell fabrication is to anneal the CdTe/CdS *pn* structure in the presence of $CdCl_2$ at ~ 400 °C under H_2. This treatment improves the cell conversion efficiency from < 2 % to typically > 10 % efficiency [11]. This improvement is related to several beneficial structural and electrical changes in both the CdTe and CdS layers. For more than 25 years, processing of CdTe thin film solar cells has necessitated the use of $CdCl_2$ activation step to ensure high conversion efficiencies.

Even though CdTe and CdS are very stable compounds they are insoluble in water and contribute little Cd to the environment. The use of water-soluble $CdCl_2$ powder in the industrial production of CdTe modules is both expensive (about 0.3 ¢ per gram [11]) and causes risks to both the operator and the environment during production. The wholesale cost of $CdCl_2$ is roughly US $ 0.3 per gram and it needs ~ 5 tonnes of $CdCl_2$ per gigawatt of device production; this gives an estimated total cost of US $ 1,500,000 per gigawatt [11]. Nevertheless, the reason for the high cost is the handling and disposal of $CdCl_2$, which requires a specialized industrial plant for the protection of operators and specialist waste disposal. Despite the drawbacks, $CdCl_2$ has been used in CdTe thin films for more than two decades and there is very little effort in identifying an effective replacement. Even though the use of a stable gas such as difluorochloromethane (CHF_2Cl) [131] yielded high efficiency devices; it also presented problems as the gas is linked to ozone depletion and therefore its use was restricted by international agreements. Since a practical alternative was never identified, $CdCl_2$-treatment remained universal in commercial high efficiency CdTe device manufacturing.

Current fundamental material studies are investigating the relative effectiveness of different chloride compounds in inducing the desired materials changes in a CdTe thin film device stack to accelerate process development. Several studies that relate desirable materials changes to $CdCl_2$ activation step include: recrystallization and grain growth of CdTe [154, 206, 207] and CdS [208, 209] layers, *p*-type doping of CdTe [11, 153, 210, 211], S/Te interdiffusion [133, 212], and grain boundary passivation [208, 213]. These reports are often contradictory in terms of identifying which of these is most beneficial in improving the device efficiency [214]. However, a recent study demonstrated the direct replacement of $CdCl_2$ with $MgCl_2$, a non-toxic and cost effective alternative, with no loss in cell performance (efficiencies around 13 % identical to those of a $CdCl_2$-treated control group) [11].

$MgCl_2$ costs about US $ 0.001 per gram (< 1 % of the cost per weight of $CdCl_2$) and can be extracted from sea water [215]. Thus, the cost of CdTe PV modules could drop to below US $ 1 per watt [205]. Since $MgCl_2$ is non-toxic, environmentally safe and widely used material it has vast potential instantly to reduce the cost of power generation by CdTe PVs and to minimize the risks in industrial manufacturing. Both $CdCl_2$ and $MgCl_2$ treated cells have similar hole densities in the active layer (9×10^{14} cm^{-3}) [11] and comparable impurity profiles for Cl and O. A study investigated the use of alternative cheap chlorides such as NaCl, KCl, HCl and $MnCl_2$, however these chlorides led to the introduction of electrically active impurities that produced significantly less efficient devices [11].

This section focuses on observing the potential of substituting $CdCl_2$ with $MgCl_2$ to fabricate CdTe solar devices with presence of intentionally added NaF layer (chapter 4, section 4.1.3.2).

6.3.2.1 Morphology and Depth Profile Analysis

As expected the Mg SIMS depth profiles in figure 6-11 show a high concentration of Mg in the CdTe layer for the $MgCl_2$-treated device by at least two orders of magnitude compared to the $CdCl_2$-treated devices. Even though the Cl content shows a similar pattern (figure 6-11) regardless of the Cl-treatment the $CdCl_2$-treated devices have a higher Cl content compared to the $MgCl_2$-treated device. The $CdCl_2$-treated device where NaF is present has a lower Mg and Cl content compared to the Na-free device. Towards the last micron of the CdTe thickness the $MgCl_2$-treated sample has higher Mg content compared to the Cl content in both $CdCl_2$-treated samples. It is also noticeable that Cl is present in the window and CdS layer of the Na-free device unlike the devices deposited with a layer of NaF (the performance results in section 7.3.1 shows higher efficiencies for Na-free samples).

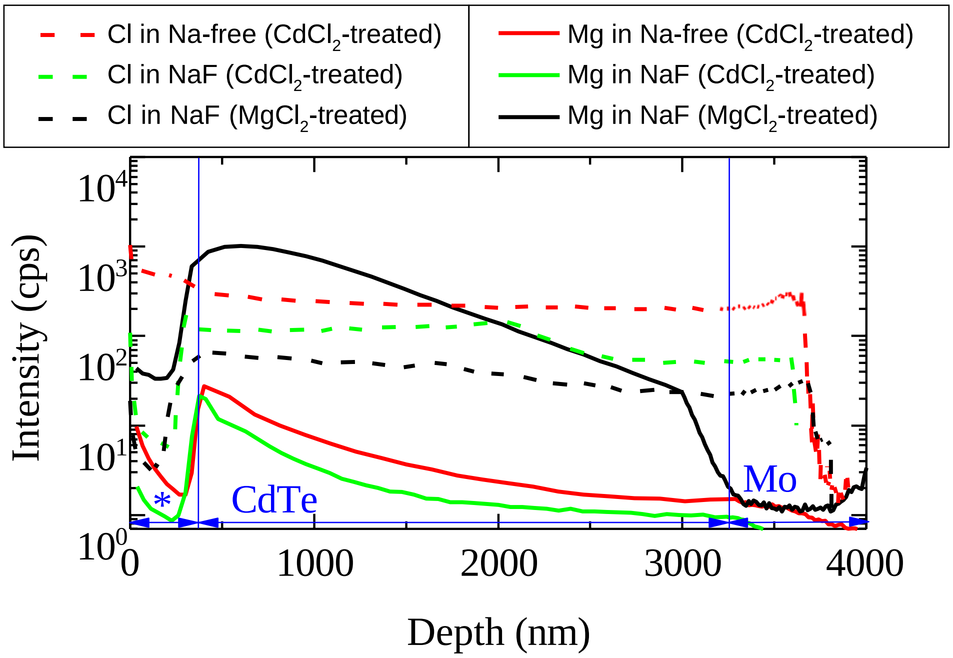

Figure 6-11: SIMS depth profiles showing the Mg and Cl content in the CdTe device for the following samples: $MgCl_2$-treated and $CdCl_2$-treated for samples with and without NaF. The Mo film was deposited with the following sputtering conditions: 10 mTorr; 3 A; 5 rpm. The data was normalised against the Mo signal intensity. The window and CdS layer depth is marked by the asterisks.

Na and F SIMS depth profiles for Cl-treated ($CdCl_2$ or $MgCl_2$) CdTe solar devices with Mo film sputtering conditions of 10 mTorr, 3 A and 5 rpm on quartz with and without NaF are shown in figure 6-12. As predicted the Na-free device shows the lowest content of Na and F throughout the device. For the devices with NaF the $CdCl_2$-treated device shows the highest F content compared to the $MgCl_2$-treated device. The $MgCl_2$-treated device shows high content of Na in the Mo film and similar content of Na in the window and CdS layer as $CdCl_2$-treated device As previously stated in chapter 5 annealing affects the Na diffusion. The varying Na content in the window, CdS and Mo layers could perhaps indicate that the annealing time was not sufficient for Na diffusion. Similar to the $MgCl_2$-treated device the $CdCl_2$-treated device with NaF shows high content of Na in the Mo layer compared to the Na-free $CdCl_2$-treated device. Even though the Na content in the Mo, window and CdS layer of the samples with NaF vary, the Na content in the CdTe layer does not vary significantly for different Cl-treated devices. In fact, for the first micron of the CdTe thickness, the Na content is almost the same.

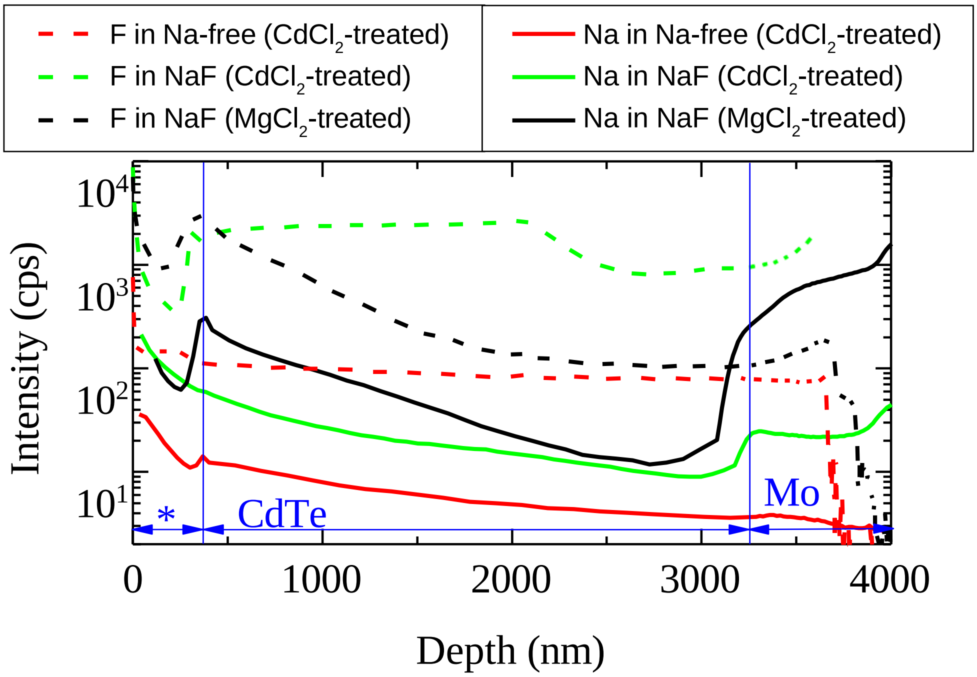

Figure 6-12: SIMS depth profiles showing the Na and F content in the CdTe device for the following samples: Na-free $CdCl_2$-treated, with NaF $CdCl_2$-treated and with NaF $MgCl_2$-treated. The Mo film was deposited on quartz with the following sputtering conditions: 10 mTorr; 3 A; 5 rpm. The data was normalised against the Mo signal intensity. The window and CdS layer depth is marked by the asterisks.

SEM micrographs of $MgCl_2$-treated and $CdCl_2$-treated devices with Mo deposited at sputtering current and pressure of 4.5 A and 10 mTorr respectively, with varying rotational speeds of 2.5 and 5 rpm are shown in figure 6-13. The cross-sections do not reveal a measureable change for samples having different Cl-treatments. Therefore, regardless of the Cl-treatment there is a similar grain growth in both samples with a similar Na content (figure 6-12).

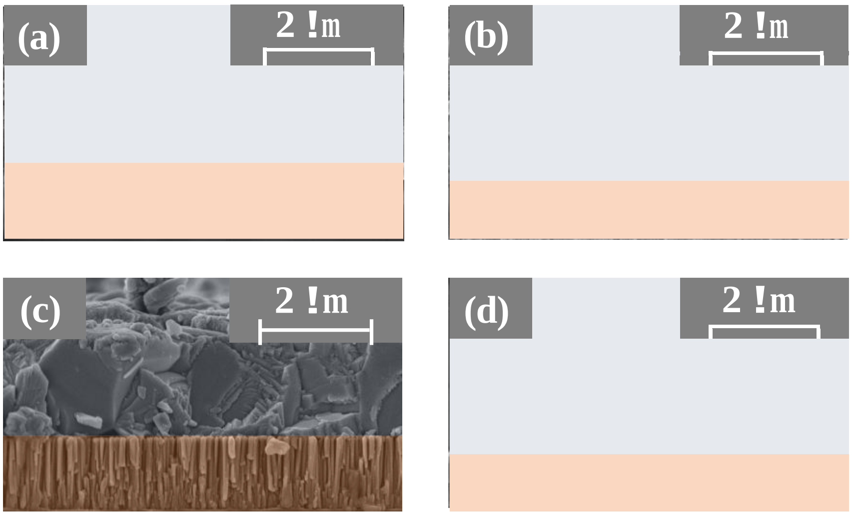

Figure 6-13: SEM micrographs of CdTe solar device cross sections when $MgCl_2$-treated (top row) and $CdCl_2$-treated (bottom row). The Mo film was deposited with the following sputtering conditions: 10 mTorr; 4.5 A; (a, c) 2.5, (b, d) 5 rpm.

6.3.2.2 Crystallographic Properties

XRD was used to analyse the crystallographic properties of the $MgCl_2$-treated samples to show consistency and reproducibility. The CdTe samples in figure 6-14 show the same peaks for as-grown and post $CdCl_2$-treatment similar to samples in figure 6-8. All samples display a very low intensity for (220), (400) and (331) peaks (figure 6-14); however, the (400) peak increases its intensity post $CdCl_2$-treatment. There is also an increase of intensity for (311) and (422) post $CdCl_2$-treatment. <111> is the dominant direction for all films.

Figure 6-15 shows the full device XRD data for the $CdCl_2$ and $MgCl_2$-treated samples. In addition to the listed peaks for CdTe and Mo layers, reflections at 2 8 = 27 ° and 30 ° are observed (represented by "·") which corresponds to the front contact layer peaks.

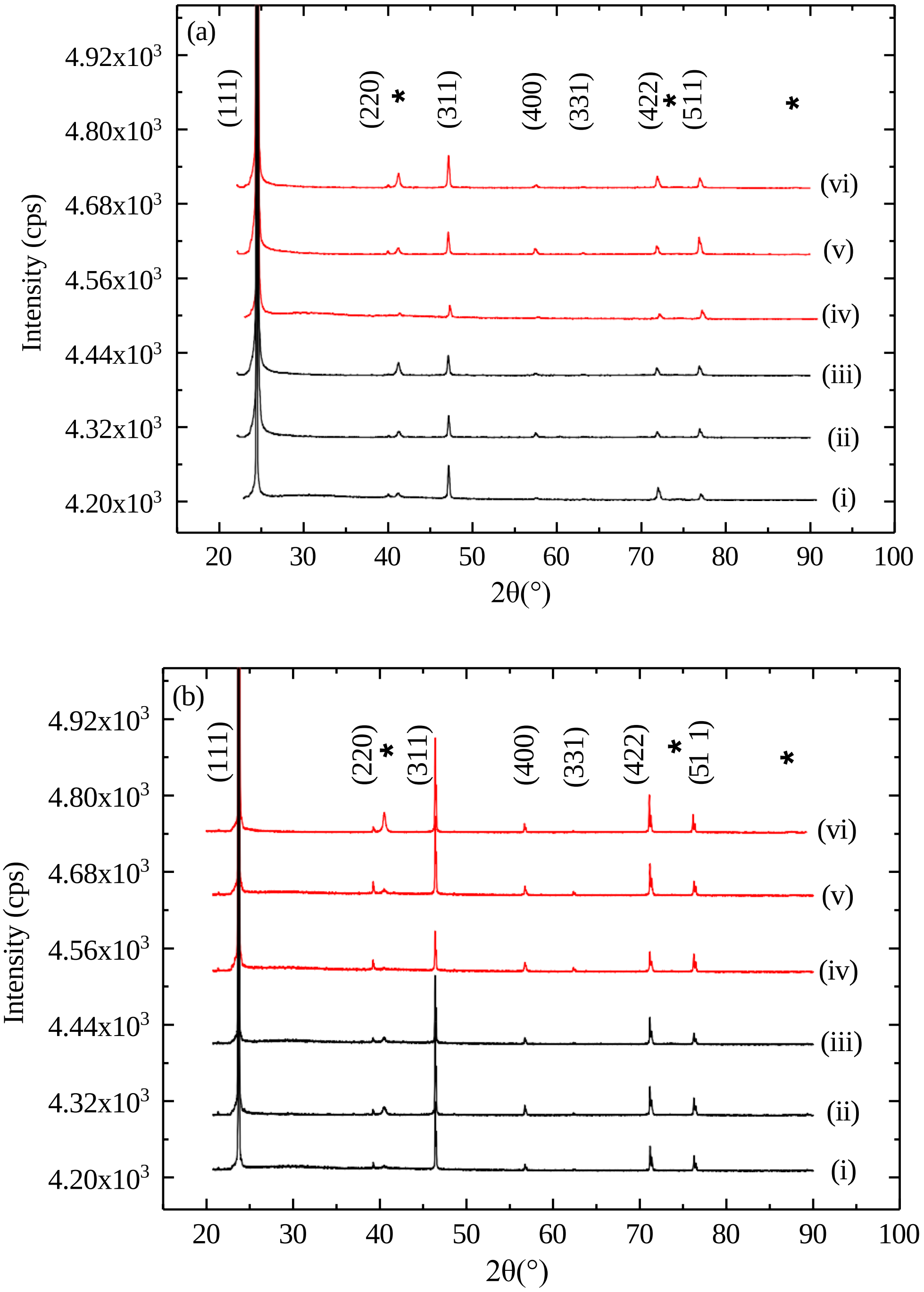

Figure 6-14: XRD patterns for (a) as-grown and (b) $CdCl_2$-treated samples. The Mo film was deposited with the following sputtering conditions: 10 mTorr; (i, iv) 4.5, (ii, v) 3, (iii, vi) 2 A; 2.5 (red), 5 rpm (black). The peaks corresponding to the Mo films are marked by asterisks and ● respectively.

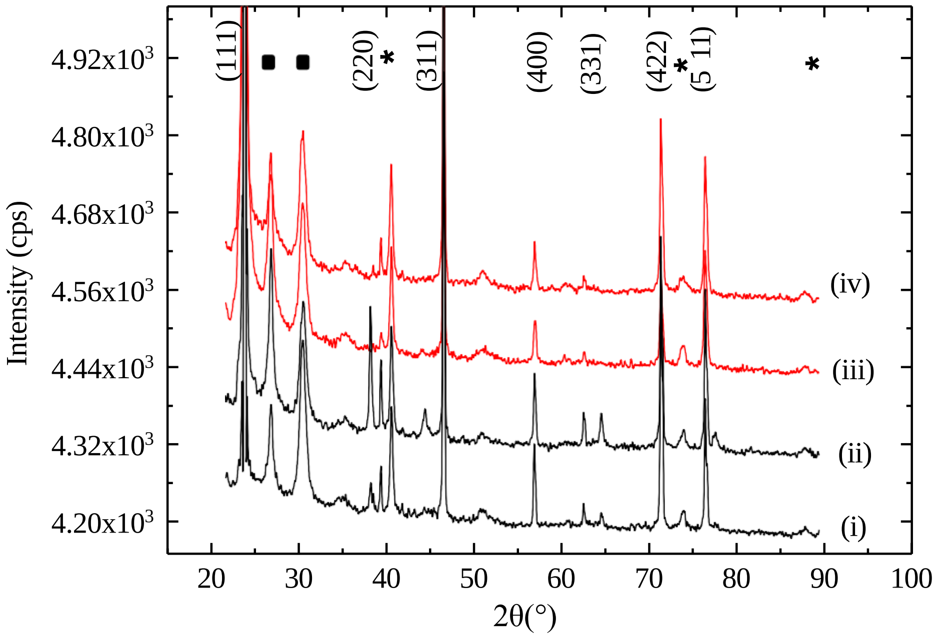

Figure 6-15: XRD patterns of full CdTe solar devices: CdCl$_2$-treated (black) and MgCl$_2$-treated (red). The Mo film was deposited with the following sputtering conditions: 10 mTorr; 4.5 A; (ii, iv) 2.5, (i, iii) 5 rpm. The peaks corresponding to the Mo film and the front contact are marked by asterisks and ■ respectively.

The effects of growth conditions on texture and preferred orientation of the samples were also investigated by calculating the texture coefficient and preferred orientation. The calculated σ values for all the samples ranges between 0.83 – 0.84 indicating a less randomly oriented samples regardless of the Cl-treatment (table 6-4).

Even though the sample prepared at 10 mTorr, 3 A and 5 rpm with NaF from table 6-3 has a similar degree of preferred orientation, to the samples in table 6-4 with the same deposition parameters; the sample in table 6-4 has a preferred orientation along the (511) plane. In fact, all of the samples in table 6-4 have a preferred orientation along the (511) plane.

Table 6-4: Texture coefficient and degree of preferred orientation for as-grown, $CdCl_2$-treated and $MgCl_2$-treated samples. The Mo film was deposited with the following sputtering conditions: 10 mTorr; 2, 3, 4.5 A; 2.5, 5 rpm.

Sputtering Current, *I* (A)	Sputtering Rotational Speed (rpm)	Texture Coefficient, A_{EFG}							Degree of Preferred Orientation, σ
		C_{111}	C_{220}	C_{311}	C_{400}	C_{331}	C_{422}	C_{511}	
As-grown									
2	2.5	0.14	0.17	0.35	1.71	1.03	1.03	2.57	0.83
3		0.14	0.17	0.34	1.71	1.03	1.03	2.58	0.83
4.5		0.13	0.17	0.34	1.71	1.03	1.03	2.58	0.83
2	5	0.14	0.17	0.34	1.71	1.03	1.03	2.57	0.83
3		0.14	0.17	0.34	1.71	1.03	1.03	2.57	0.83
4.5		0.12	0.17	0.35	1.72	1.03	1.03	2.58	0.84
$CdCl_2$-treated									
2	2.5	0.13	0.17	0.35	1.71	1.03	1.04	2.58	0.83
3		0.13	0.17	0.35	1.71	1.03	1.04	2.57	0.83
4.5		0.12	0.17	0.35	1.72	1.03	1.04	2.58	0.84
2	5	0.13	0.17	0.35	1.71	1.03	1.03	2.58	0.83
3		0.13	0.17	0.35	1.71	1.03	1.03	2.58	0.83
4.5		0.14	0.17	0.35	1.71	1.03	1.03	2.57	0.83
$MgCl_2$-treated									
4.5	2.5	0.12	0.17	0.36	1.70	1.01	1.03	2.61	0.84
4.5	5	0.11	0.17	0.38	1.69	1.00	1.05	2.60	0.84

6.4 Conclusion

The effect of Na and Cl on the morphological and structural properties of CdTe thin films deposited on a Mo-coated substrate have been investigated. The microstructural investigation showed that the presence of Na between the back-contact layer and CdTe film leads to a marked increase in grain size of the as-grown CdTe absorber, with average grain sizes up to 1.9 μm compared with < 0.2 μm for Na-free CdTe. Post $CdCl_2$-treatment, the grains are transformed from faceted to round shape with a reduction in grain size (1.0 μm) but still significantly larger than sample processed without Na (0.5 μm). NaF doping is only viable when induced after the Mo back-contact deposition due to poor adhesion between the glass, NaF and Mo layers. Even though NaF does not induce large crystallographic changes, some films show a preferred orientation along the (111) plane and others along the (511) plane.

Replacement of $CdCl_2$-treatment with $MgCl_2$-treatment does not affect the morphology or structure of the films. The combined NaF and Cl-treatment provides a new avenue for the development of MOCVD CdTe thin films which should be further exploited at device level in substrate configuration and this is described in chapter 7.

CHAPTER 7

7 MOCVD Grown CdTe Devices in Substrate Configuration

This chapter focuses on device performance when samples were deposited with sodium and a method to improve the window layer response. After a brief introduction (section 7.1), section 7.2 describes the addition of a CdZnS layer. Finally, section 7.3 follows by analysing the device performance.

7.1 Introduction

CdTe has a bandgap close to the ideal single junction solar cell, however the full benefit cannot be used due to the bandgap of the CdS (2.42 eV). Most of the blue photons are absorbed by the CdS layer; thus, they do not contribute to photocurrent generation. Therefore, without entirely substituting CdS layer, either its thickness should be reduced [100, 214], or its bandgap widened [217].

In addition to the improving the photocurrent, reducing the thickness of the CdS layer will decrease the material usage, growth time and the energy input, for large-scale fabrication [98]. However, a thin CdS layer (50 – 80 nm) can cause possible conversion efficiency reduction, due to the increased risk of creating micro-shunt, at the TCO surface, produced by pin holes. This imposes the use of an additional oxide layer between the TCO and window layer to minimise shunting

[112]. Nevertheless, this will increase the number of fabrication steps and therefore the series resistance for the device.

Combination of doped/alloyed CdS thin films with tuneable bandgap appears to be challenging [218–220] and remains to be fully explored with a view toward thin film PV devices. Thus, an alternative method for widening the window layer bandgap appears to be a possible option towards improving CdTe-based solar cells. This study shows the advantage of window layer bandgap tuning in CdZnS/CdTe devices, achieved by an atmospheric pressure metal organic chemical vapour deposition (AP-MOCVD) method owing to its process tuneability and therefore suitability for alloying, compared to CdS/CdTe devices.

As demonstrated in chapter 6 the presence of NaF in CdTe solar cells can result in increased grain size of the absorber layer. The literature shows that presence of Na in CdTe solar cells can also increase acceptor density and u_{vb} as it acts as a shallow acceptor in CdTe with low activation energy [48, 193, 197, 198]. Therefore, this chapter aims to show how the contribution of CdZnS and NaF can both be beneficial for the device performance. It also shows the potential of replacing $CdCl_2$ with $MgCl_2$ to reduce the device cost and environmental impact.

7.2 Experimental Properties

Mo-coated quartz substrates deposited with a layer of NaF were used in CdTe device fabrication to observe the effect on the electrical properties. Some Na-free devices from chapter 5 are also discussed in this chapter for comparison purposes.

The devices were either deposited by a layer of CdS, or a layer of CdZnS to observe the benefit of window layer bandgap widening. The complete device fabrication procedure is described in chapter 4.

7.3 Results and Discussion

The device performance was analysed using L¥L and *J–V* measurements.

7.3.1 Device Performance

The photovoltaic parameters for NaF and Na-free devices are shown in table 7-1. The device parameters show poor results, indicative of weak diode properties (*J–V* curves under illumination and in dark are shown in figure 7-1 and figure 7-2). The impact of NaF on the device performance is noticeable. Even though the literature [201] shows the use of F in conjunction with Cl can lead to high efficiencies, in this case the use of NaF in conjunction with Cl in the CdTe devices leads to degraded device performance and this could be due to excessive CdS-CdTe intermixing (refer to section 6.3.2 for the Na and F contents in the CdTe device).

The u_{vb} was found to significantly decrease when the devices were processed with NaF. However, the device processed with NaF at 7 mTorr showed an improvement in the u_{vb} compared to the Na-free device. After a slight decrease of the Y_{ab} (7 mTorr, with NaF), it was regained when the Mo film sputtering pressure was increased and despite a small drop in u_{vb}, the devices showed similar efficiencies.

As the sputtering pressure increases, the m_r values decrease for both NaF deposited and Na-free devices. In an ideal case the m_{rE} should be as high and m_r as low as possible. The results in table 7-1 show low range of m_{rE} (14 – 114 Ωcm^2) and high range of m_r (16 – 36 Ωcm^2) for samples deposited with NaF. In comparison, the Na-free devices have higher values of m_{rE} (114 – 400 Ωcm^2) and slightly lower values of m_r (9 – 33 Ωcm^2). Low m_{rE} causes loss in the device by providing an alternate current path for the light-generated current. This diversion reduces the current flow; therefore, reducing the u_{vb}. The m_r has a high impact on the *FF*, therefore as m_r increases the *FF* decreases (table 7-1). Also, in the case where the m_r value is excessively high the Y_{ab} value can be reduced as well.

The CdS/CdTe Device deposited at sputtering pressure of 10 mTorr with a layer of NaF has an efficiency of 4.35 %. The presence of Na reduces the u_{vb} and Y_{ab} and causes the efficiency to drop down to 1.29 %. Despite the expected assumptions, the device with bilayer-Mo showed poor device properties with Y_{ab} of 14.86 mA/cm^2 and u_{vb} of 200 mV (low value of m_{rE} = 14 Ωcm^2), giving it low efficiency of 0.86 % (*J–V* curves in figure 7-1). The fabrication process has not been optimised for CdS/CdTe devices and this is reflected in the PVs parameters.

Table 7-1: PVs parameters for NaF and Na-free, $CdCl_2$-treated CdS/CdTe devices. The Mo film was deposited with the following sputtering conditions: 3 A; 3, 7, 10, 10/3 mTorr; 5 rpm. (10/3 mTorr is a bi-layer device). (Peak data average).

Sputtering Pressure, P(mTorr)		η (%)	Y_{ab} (mA/cm^2)	u_{vb} (mV)	*FF* (%)	Calculated Y_{ab} (mA/cm^2)	m_r (Ωcm^2)	m_{rE} (Ωcm^2)
NaF	3	1.64	13.38	429	29	16.27	36	35
	7	0.88	12.95	286	24	6.17	25	23
	10	1.29	17.68	282	26	15.71	30	114
	10/3	0.86	16.48	200	26	16.40	16	14
Na-free	3	3.20	12.45	529	49	17.38	33	400
	7	0.51	14.04	116	32	7.06	9	114
	10	4.35	14.90	557	52	17.50	13	400

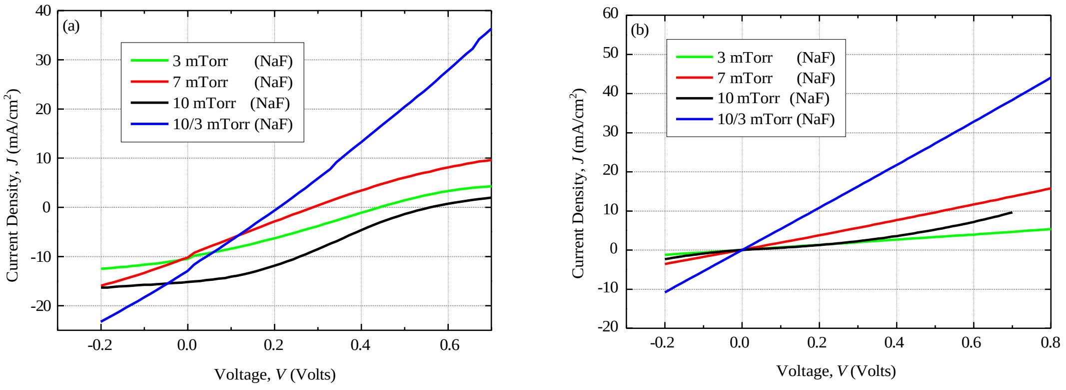

Figure 7-1: *J–V* curves for CdS/CdTe devices fabricated with NaF (a) under illumination and (b) in dark. The Mo film was deposited with the following sputtering conditions: 3 A; 3, 7, 10, 10/3 mTorr; 5 rpm.

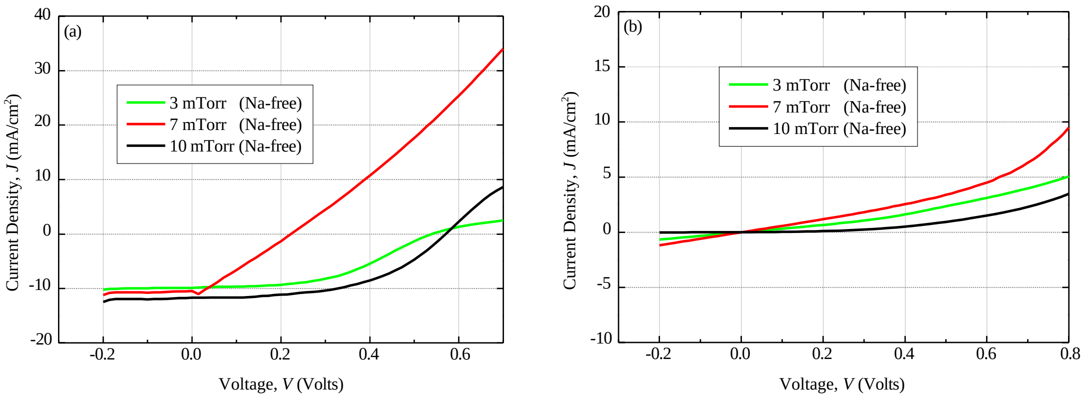

Figure 7-2: *J–V* curves for Na-free CdS/CdTe devices (a) under illumination and (b) in dark. The Mo film was deposited with the following sputtering conditions: 3 A; 3, 7, 10 mTorr; 5 rpm.

Figure 7-3 shows the L¥L curves for the devices listed in table 7-1. The L¥L curves show devices with Mo sputtering pressures of 3 and 10 mTorr to have high responses up to 75 % compared to the device with sputtering pressure of 7 mTorr that has a L¥L response below 30 % (Note: the device with NaF and Na-free deposited at sputtering pressure of 10 mTorr have an artefact arising at ! = 680 nm and ! = 650 nm, respectively due to calibration). Addition of NaF has shifted the curve by 50 nm for devices deposited at sputtering pressures of 3, 7 and 10 mTorr. The maximum L¥L response for Na-free samples is at ! ~ 580 nm whereas the maximum response for devices with NaF is at ! ~ 630 nm. Even though the CdS LR results tabulated in table 7-2 show a slight decrease in the bandgap with NaF, the devices are still within a close range (3.2 – 3.4 eV).

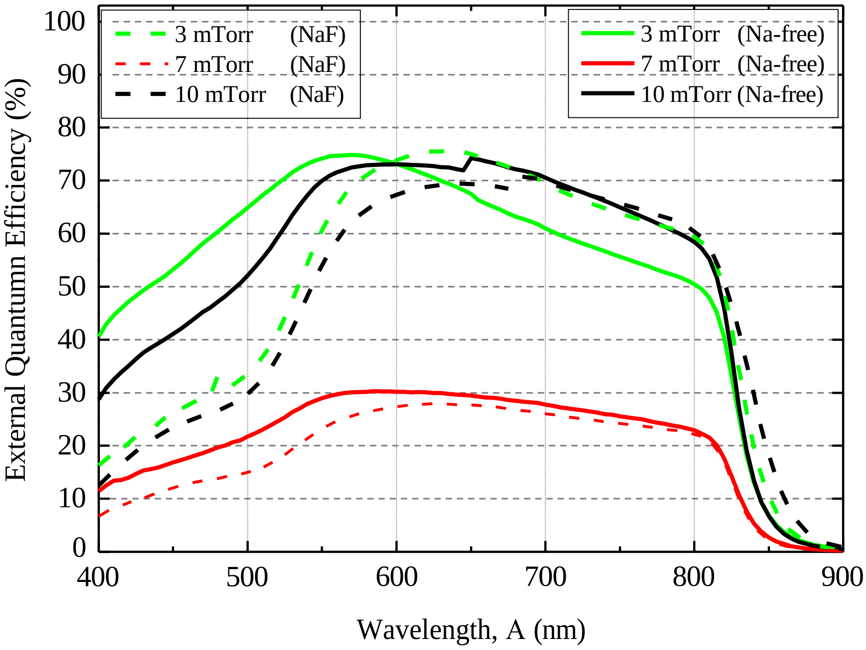

Figure 7-3: Ø“Ø for CdS/CdTe devices with and without NaF. The Mo film was deposited with the following sputtering conditions: 3, 7, 10 mTorr; 3 A; 5 rpm.

Table 7-2: The energy bandgap of CdS (Ø∞) was determined from the Ø“Ø spectra in figure 7-3, by the extrapolating the linear portion of the curve [<> × fifl(‡ − Ø“Ø)]ˆ **against <>.**

	Sputtering Pressure, P (mTorr)	Bandgap, L_R (eV)
NaF	3	3.3
	7	3.2
	10	3.2
Na-free	3	3.4
	7	3.3
	10	3.4

The Y_{ab} achieved by a solar cell can be estimated from the L¥L spectrum. Therefore, L¥L is commonly used to describe the different types of losses responsible for a reduction in the measured Y_{ab}. To obtain the Y_{ab}, the AM1.5

spectrum is initially divided into subgroups following the step size of L¥L measurement (5 nm). Then the incident power in each group was obtained by integrating the solar spectrum in the group wavelength range. The number of incident photons in each group was calculated by:

$$\text{d,?„É™ ´U f}h\text{´s´d@} = \frac{\text{¨dsÉk™xsÉå @´[x™ @fÉKs™,? (ò/?}^{\text{I}}\text{)}}{h\text{K/! (Y)}} \tag{7-1}$$

When the reflection and transmittance losses are not considered the L¥L is the number of collected electrons divided by the number of incident photons. Therefore if:

$$\text{L¥L} = \frac{\text{K,™™Éds åÉd@¨sÆ} \big/ \text{K}h\text{x™kÉ ´U ´dÉ É[ÉKs™´d}}{\text{f´≠É™ åÉd@¨sÆ ´U ¨dK¨åÉds f}h\text{´s´d@} \big/ \text{ÉdÉ™kÆ ´U ´dÉ f}h\text{´s´d}} \tag{7-2}$$

then substituting 7-1 into 7-2, the Y_{ab} from the subgroup is given as:

$$Y_{\text{rnMRpgnD}} = \text{d,?„É™ ´U f}h\text{´s´d@} \times \text{L¥L} \times \text{K}h\text{x™kÉ ´U ´dÉ É[ÉKs™´d} \tag{7-3}$$

The Y_{ab} from a solar cell is then found by summing up all the subgroup values. The calculated Y_{ab} values are listed in table 7-1. For devices with NaF the calculated Y_{ab} is high at 3 mTorr and low at 10 mTorr compared to the Y_{ab} measured from the *J–V* curve. Lower calculated Y_{ab} could be due to the following: barrier for the photo-current which is large under low light intensity but becomes lower by photo doping of the buffer at AM1.5 illumination [221], and large number of micro shunts. If the device is illuminated only on a limited area, the non-illuminated area acts as a shunting load. In an active device, this load is in parallel with the input resistance of the L¥L current amplifier. Even if the total m_{rE} of the device is high, the local m_{rE} from the active device portion could be small. Therefore, the Y_{ab} is drained throughout the shunting load. Reducing the device area to the area of illumination could increase the L¥L [14]. The Na-free samples have a higher calculated Y_{ab} compared to the measured Y_{ab}. This is when a barrier for the photo-current exists. Due to a limited thermionic emission current, the small current density of a L¥L measurement can pass the barrier. In contrast, the high current density under AM1.5 illumination cannot pass the barrier [221]. Both Na-free and NaF deposited devices with sputtering pressure of 7 mTorr have a low calculated Y_{ab} that is an order of magnitude lower and this due to poor L¥L response.

As show in the L¥L measurements (figure 7-3) of NaF deposited devices the optical absorption at ! < 550 nm is poor which is mainly due to the window layer bandgap. Therefore, the next section of the study focuses on an alternative method for widening the window layer bandgap by adding a CdZnS layer along with other deposition variations in attempt to improve the device performance. A summary of the electrical properties of these devices are shown in table 7-3.

On average the u_{vb} was found to be higher at lower sputtering rotational speed; however, the highest u_{vb} of 445 mV was observed at 4.5 A and 5 rpm for $CdCl_2$-treatment + CdZnS. The $CdCl_2$-treatment + CdZnS devices showed a higher Y_{ab} value compared to the devices that were not deposited with a layer of CdZnS. The lowest Y_{ab} (6.43 – 10.22 mA/cm^2) was observed for devices with $MgCl_2$-treatment + CdS. The m_r and m_{rE} values for these devices were calculated as described in chapter 5 and are listed in table 7-3. The devices have high values of m_r

causing the *FF* reduction and low values of m_r cause reduction of u_{vb} . Figure 7-4 and figure 7-5 show the poor results of the *J–V* curves measurements for the following devices: $CdCl_2$-treatment + CdZnS and $CdCl_2$-treatment + CdS.

Table 7-3: PVs parameters for the following CdTe devices: CdCl$_2$-treatment + CdZnS, CdCl$_2$-treatment + CdS and MgCl$_2$-treatment + CdS. The Mo film was deposited with the following sputtering conditions: 10 mTorr; 2, 3, 4.5 A; 2.5, 5 rpm with a layer of NaF. (Peak data average).

Sputtering Current, *I* (A)	Sputtering Rotation Speed (rpm)	η (%)	!"# (mA/cm^2)	%&# (mV)	*FF* (%)	Calculated !"# (mA/cm^2)	▾((Ωcm^2)	▾O (Ωcm^2)
CdCl$_2$-treatment + CdS								
2	2.5	2.54	10.65	436	55	11.5	18	27
3		2.99	15.26	418	46	16.7	18	145
4.5		1.77	14.85	318	37	16.2	20	67
3	5	2.2	13.83	364	44	14.8	21	57
4.5		0.9	13.71	173	38	13.8	12	26
MgCl$_2$-treatment + CdS								
4.5	2.5	1.66	10.22	364	45	8.4	14	145
4.5	5	0.62	6.43	264	36	5	25	133
CdCl$_2$-treatment + CdZnS								
2	2.5	2.88	19.05	427	35	19	40	73
3		3.57	26.08	409	33	18.4	25	29
4.5		1.49	16.26	300	31	18	29	24
2	5	1	18.18	173	32	12.1	11	10
3		0.66	12.8	155	33	14.8	14	15
4.5		3.6	20.18	445	40	15.9	26	145

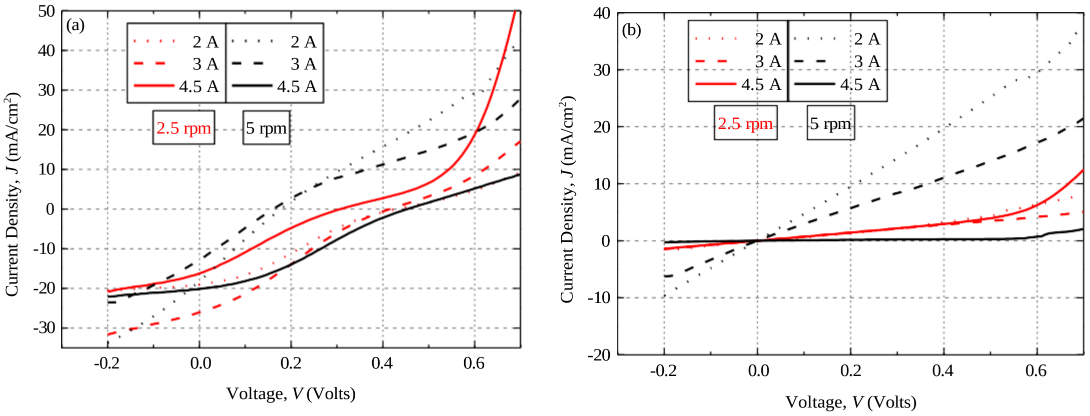

Figure 7-4: *J–V* curves for $CdCl_2$-treatment + CdZnS devices (a) under illumination and (b) in dark. The Mo film was deposited with the following sputtering conditions: 10 mTorr; 2, 3, 4.5 A; 2.5, 5 rpm.

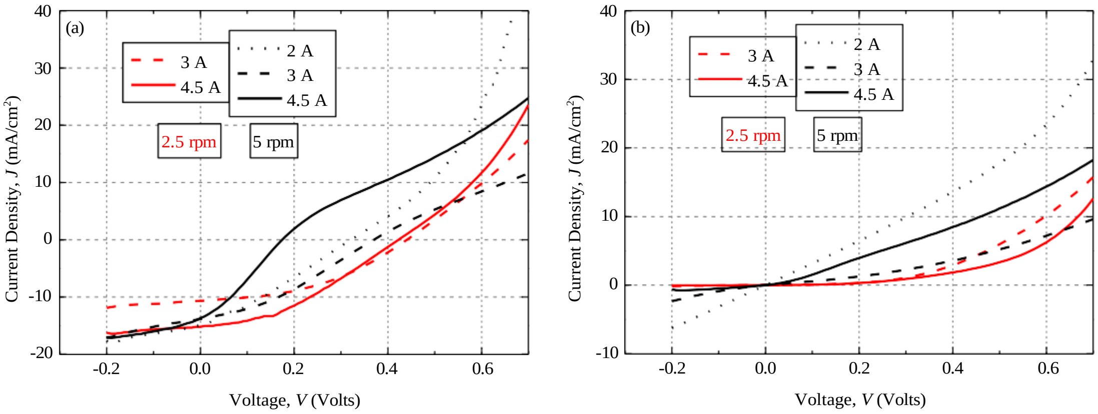

Figure 7-5: *J–V* curves for $CdCl_2$-treatment + CdS devices (a) under illumination and (b) in dark. The Mo film was deposited with the following sputtering conditions: 10 mTorr; 2, 3, 4.5 A; 2.5, 5 rpm.

Figure 7-6 a and b show the !"! curves for the following devices: $CdCl_2$-treatment + CdZnS and $CdCl_2$-treatment + CdS, respectively. The curves show the typical top-hat shape characteristic of a heterojunction cell. Comparing the !"! curves in figure 7-6 a and b, it is obvious that the addition of Zn has improved the optical transmission in the following wavelength range: 400 < # < 550 nm. For wavelength range of 350 < # < 450 nm in figure 7-6 a the response is not uniform.

This could be due to either the CdZnS layer thickness or variation in Zn concentration. Changing the Zn concentration changes the CdZnS bandgap. Patidar *et al.* [222] showed that increasing the Zn concentration causes the energy bandgap, !$, to increase. Therefore, the !$ for the !"! spectra in figure 7-6 were calculated by the extrapolating the linear portion of the curve $[h(\times \ln(1 - !"!)]^2$ against $h($. The !$ results tabulated in table 7-4 show a close range of !$ (3.21 – 3.35 eV) for all the devices (figure 7-6 a). Therefore, this non-uniformity in the !"! is not due to Zn concentration but due to the CdZnS layer thickness. Also, the curves in figure 7-6 b have a !$ of 2.55 eV.

Devices with sputtering rotational speed of 2.5 rpm in figure 7-6 a show the highest !"! (~ 70 %). Even though devices without CdZnS (figure 7-6 b) show !"! higher than 40 %, their optical absorption at # < 550 nm is very poor compared to CdZnS deposited devices. All devices in figure 7-6 show a similar pattern at higher wavelengths (# > 700 nm); which responds to the absorber and back-contact layer.

The !"! curves (figure 7-6) were used to calculate the 345 values (table 7-3). The calculated 345 values vary for CdCl$_2$-treatment + CdZnS devices where the 345 values show a higher range (18 – 19 mA/cm^2) at sputtering rotational speed of 2.5 rpm than 5 rpm (12 – 16 mA/cm^2). The CdCl$_2$-treatment + CdS and devices have a close range of measured and calculated 345 where the measured are higher than calculated 345 values. The devices in table 7-3 showed a close range of calculated 345.

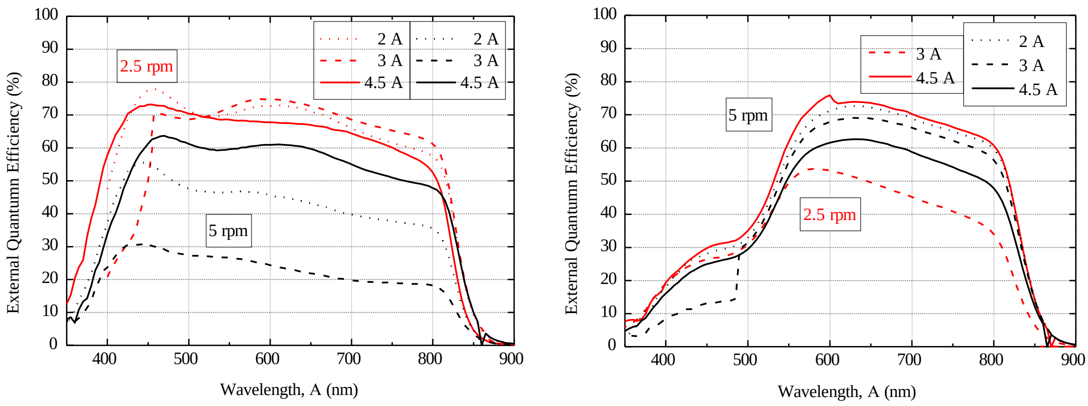

Figure 7-6: 676 **for devices with (a) $CdCl_2$-treatment + CdZnS and (b) $CdCl_2$-treatment + CdS. The Mo film was deposited with the following sputtering conditions: 10 mTorr; 2, 3, 4.5 A; 2.5, 5 rpm.**

Table 7-4: The energy bandgap (68**) was determined from the** 676 **spectra in figure 7-6 a, by the extrapolating the linear portion of the curve** [9: × ;<(= − 676)]$^{>}$ **against** 9:**.**

Sputtering Current, *I* (A)	Sputtering Rotation Speed (rpm)	Bandgap, !$ (eV)
$CdCl_2$-treatment + CdZnS		
2	2.5	3.21
3		3.25
4.5		3.35
2	5	3.24
3		3.28
4.5		3.21

Figure 7-7 and figure 7-8 shows the !"! and *J*–*V* curves for $CdCl_2$-treatment + CdS and $MgCl_2$-treatment + CdS devices. $CdCl_2$-treated devices show a better performance compared to $MgCl_2$-treated devices. It should be noted that the jump in the $MgCl_2$-treated device at 5 rpm is not real and it is due to the pre-amplification setting. Devices with sputtering rotational speed of 2.5 rpm showed a maximum response of 70 % and 40 % for $CdCl_2$-treatment + CdS and $MgCl_2$-treatment + CdS devices, respectively. The calculated 3_{45} for the $MgCl_2$-treated devices (figure 7-7) is half of the 3_{45} for $CdCl_2$-treated devices (table 7-3). The low calculated 3_{45} depends on the **!"!** curve, the device was illuminated only on a limited area, where the non-illuminated area could act as a shunting load. Since the $MgCl_2$-treatement was not uniform across the device and this could have been a limiting factor for the device to have the maximum **!"!** response and therefore causing the 3_{45} to be drained. The **$?_{@}$** and **$?_{@A}$** calculated from the *J–V* curves in figure 7-8 show high and low values, respectively. This is not desirable and it explains the poor device performance and low values of *FF* and B_{C5} .

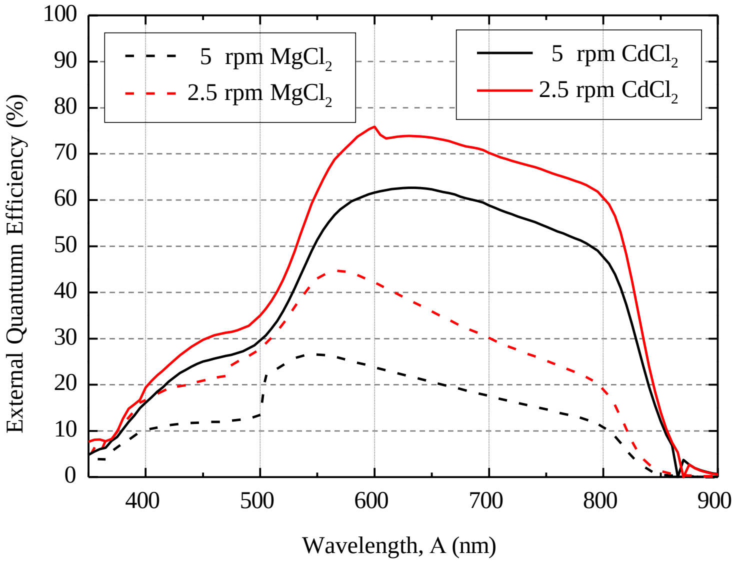

Figure 7-7: 676 **for $CdCl_2$-treatment + CdS and $MgCl_2$-treatment + CdS devices. The Mo film was deposited with the following sputtering conditions: 10 mTorr; 4.5 A; 2.5, 5 rpm.**

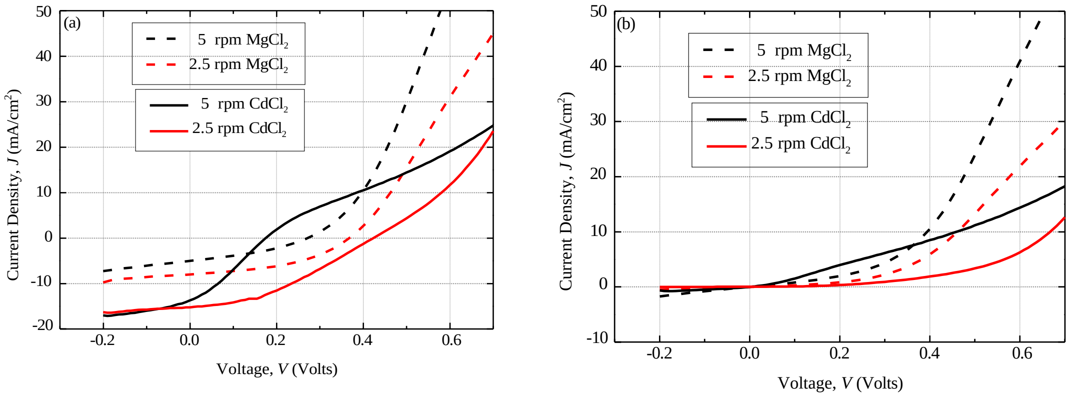

Figure 7-8: *J–V* curves for $CdCl_2$-treatment + CdS and $MgCl_2$-treatment + CdS devices (a) under illumination and (b) in dark. The Mo film was deposited with the following sputtering conditions: 10 mTorr; 4.5 A; 2.5, 5 rpm.

7.4 Conclusion

Overall the fabricated devices had low efficiency (< 5 %) arising from weak *J–V* parameters. The devices showed weak diode characteristics and possible lack of interdiffusion at the *pn* junction arising from the low temperature deposition of the CdS layer. The results showed that the addition of NaF shifted the optical transmission maximum to wavelength of 630 nm compare to Na-free devices where the maximum response occurred at 580 nm.

In addition, CdZnS deposited devices with NaF further improved the optical absorption, by improving the absorption at range of 400 < # < 550 nm. The investigation to replace the $CdCl_2$-treatment with $MgCl_2$-treatment produces devices with low electrical properties and it requires further optimization.

CHAPTER 8

8 Conclusions and Outlook

This chapter summaries the work done during this study, followed by suggestions for the future.

8.1 Thesis Summary

This thesis detailed the fabrication of CdTe thin film solar cells. In particular, this study aimed to promote further recrystallization in CdTe thin film for substrate configuration devices by combination of Cl and Na. An overview of the range of fabrication and characterisation methods used were described in chapter 4.

Chapter 5 focused on the optimisation of the Mo back-contact layer using DC magnetron sputtering by fabricating single and bi-layer Mo films. The following sputtering conditions were used to deposit the Mo films: time 30 – 100 min, current 1.5 – 4 A and Ar-mass flow rate 25 – 70 sccm (Ar pressure 3 – 10 mTorr) at room temperature. As a result, Mo films with a low resistivity ranging between 20 – 60 μΩcm for samples of similar thickness (~ 1.0 µm) were obtained. The films deposited using sputtering currents of 4.5 and 1.5 A had low (22 – 39 μΩcm) and high (52 – 62 μΩcm) resistivity, respectively. Also, the depth characterisation of the Mo films on SLG showed that as sputtering current increased the Na content did not vary significantly; however, the Na content decreased as the sputtering pressure increased.

It is important to recognize that the entire solar cell is a multi-layer structure therefore the back-contact should withstand the subsequent processing steps. The performance of the Mo back-contact film when included in a device stack by fabricating the CdTe devices using MOCVD technique was investigated. The stack had the following configuration: substrate/Mo/CdTe/CdS/TCOs/Ni-Al. An efficiency of 4.35 % was achieved for a sample with Mo film sputtering deposition conditions of 10 mTorr and 3 A with $CdCl_2$-treatment on quartz substrate. Even though, the B_{C5} and efficiency of the devices were decreased by 56 % and 76 % respectively, with respect to increasing sputtering current to 4.5 A; devices with good adhesion to the substrate at high temperatures were fabricated.

The lack of literature on the role of Na and its effect on CdTe absorber layer was the motivation for the next part of this study. Chapter 6 investigated the Na content in CdTe based thin films by intentionally adding a NaF layer before and after the Mo film by thermal evaporation technique. This chapter also investigated the role an alternative Cl-treatment in CdTe thin film by introducing $MgCl_2$ to replace $CdCl_2$.

For this part of the study the Mo thin films were deposited on quartz substrates using DC magnetron sputtering with target current of 2, 3 and 4.5 A, at room temperature and at Ar sputtering pressures of 3, 7 and 10 mTorr whilst rotating at a speed of 2.5 or 5 rpm. Apart from the Cl-treatment step, all other device processing steps were identical to the previous studies. The Na investigation used three different sample layouts which were prepared using quartz substrates: (i) CdTe/Mo/quartz, (ii) CdTe/Mo/NaF/quartz and (iii) CdTe/NaF/Mo/quartz where NaF, ~ 10 nm was deposited by thermal evaporation at room temperature. Two Cl-treatments were compared: (1) the standard $CdCl_2$-treatment and (2) direct deposition of an $MgCl_2$ solution. The microstructural investigation showed that the presence of Na between the back-contact layer and CdTe film increased the grain size of the as-grown CdTe absorber, with average grain sizes up to 1.9 μm compared with < 0.2 μm for Na-free samples. Post $CdCl_2$-treatment, the grains transformed from faceted to round shape with a reduction in grain size (1.0 μm) but still significantly larger than Na-free samples (0.5 μm). Due to poor adhesion between the glass and the Mo film the NaF must be deposited after the Mo back-contact. It was concluded that even though introduction of NaF did not induce large crystallographic changes, some films showed a preferred orientation along the (111) plane and others along the (511) plane.

Replacement of $CdCl_2$-treatment with $MgCl_2$-treatment as an alternative Cl-treatment did not affect the morphology or structure of the films. Even though $MgCl_2$-treatment produced working devices, the efficiencies were limited. Therefore, the investigation to replace the $CdCl_2$-treatment with $MgCl_2$-treatment requires further optimisation.

Finally, chapter 7 investigated the device performance of completed Mo-coated quartz substrates deposited with a layer of NaF from chapter 6 (some Na-free devices from chapter 5 were also discussed in this chapter for comparison purposes). It also briefly investigated the approach to improve the window layer performance by using CdZnS instead of CdS. Therefore, the devices were either deposited with a layer of CdS, or a layer of CdZnS using AP-MOCVD and the benefit of window layer bandgap widening was explored.

Overall the fabricated devices had low efficiency (< 5 %) arising from weak *J–V* parameters. Some devices showed weak diode characteristics and possible lack of interdiffusion at the *pn* junction arising from the low temperature deposition of the CdS layer. The results showed that the addition of NaF shifted the optical transmission maximum to wavelength of 630 nm compare to Na-free devices where the maximum response occurred at 580 nm. In addition, the CdZnS deposited devices with a layer of NaF further improved the optical absorption.

8.2 Suggestions for Future Works

Further to the work describe in this thesis, few questions remain and additional studies are needed to further develop the investigated work on CdTe thin film solar cells.

- Inclusion of Na after the Mo back-contact layer has showed improvement in calculated 3_{45} compared to the Na-free devices. However, poor results of B_{C5} and *FF* create limitation for the performance of the device. Therefore, further optimisation is required to improve the overall electrical properties of the devices.
- Introducing a buffer layer between the absorber and the metallic part of the back-contact. This buffer layer can either lower the Schottky barrier height as severe Schottky barrier can occur since CdTe and Mo have a large work function difference or the barrier can be narrowed by the inclusion of a *p*-type layer with high acceptor density, allowing the holes to tunnel through the barrier. These can be overcome with the addition of a thin layer of Cu or Mo oxide to create a quasi-ohmic electrical back-contact.

- Introducing an alternative back-contact material that withstands all the subsequent deposition and annealing steps for activation, as well as the formation of the *pn* heterojunction with minimized recombination losses.
- Investigate other methods of chloride steps such as: $CdCl_2$-treatment of the CdTe-CdS layer stack, $CdCl_2$-treatment after both CdTe and CdS, double $CdCl_2$-treatment or, $MgCl_2$-treatment after $CdCl_2$-treatment.
- The $MgCl_2$ post deposition treatment of CdTe thin film devices should be optimised with respect to the structures that have been proved to be suitable for high efficiency devices.
- The effect of the annealing treatment on electronic properties and diffusion of impurities should also be further studied.

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List of Publications and Conference Presentations

A. Amirkhalili, V. Barrioz, S. J. C. Irvine, N. S. Beattie, and G. Zoppi, “A combined Na and Cl treatment to promote grain growth in MOCVD grown CdTe thin films,” *J. Alloys Compd.*, vol. 699, pp. 969–975, 2017.

A. Amirkhalili, V. Barrioz, S. J. C. Irvine, N. S. Beattie, and G. Zoppi, "Sodium Induced Microstructural Changes in MOCVD-grown CdTe Thin Films," in *32nd European Photovoltaic Solar Energy Conference and Exhibition*, Munich, Germany, 2016, pp. 1076-1080.

A. Amirkhalili, V. Barrioz, S. J. C. Irvine, N. S. Beattie, and G. Zoppi, "Sodium Induced Microstructural Changes in MOCVD-grown CdTe Thin Films," in *32nd European Photovoltaic Solar Energy Conference and Exhibition*, Munich, Germany, 20th June 2016. (Oral Presentation)