An Ultrafast 1 x *M* All-optical WDM Packet-Switched Router based on the PPM Header Address

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Abstract: *This paper presents an all-optical 1 x M WDM router architecture for packet routing at multiple wavelengths simultaneously, with no wavelength conversion modules. The packet header address adopted is based on the pulse position modulation (PPM) format, thus enabling the use of only a single-bitwise optical AND gate for fast header address correlation. It offers multicast as well as broadcast capabilities. It is shown that a high speed packet routing at 160 Gb/s can be achieved with a low channel crosstalk (CXT) of ~ -27 dB at a channel spacing of greater than 0.4 THz and a demultiplexer bandwidth of 500 GHz.*

Keywords: Wavelength division multiplexing, packet switching, pulse position modulation, address correlation, symmetric Mach-Zehnder, optical switch.

1. Introduction

The rapidly increasing Internet traffic together with a high digital resolution video broadcasting (video-on-demand) requires access to an ultrahigh speed optical communication networks. All-optical packet switched networks [1, 2] offering flexibility and capability to deal with the bursty traffic is one solution to deal with the increasing demand for bandwidth. However, to fully utilize the potential of such networks, packet header processing and routing decision should be carried out in the optical domain rather than in the electrical domain to avoid the speed bottleneck imposed by the slow response of currently available electronic devices. Recently developed ultra high-speed Boolean logic gates (such as AND, OR and XOR) operating above 40 Gb/s have become the key enabling technology for realising all-optical routers [3-5]. At present, packet header recognition is carried out by sequentially correlating the incoming packet header address with every entry of a local routing table. For a small size network with reasonable size routing table sequential correlation is viable both in terms of processing speed and implementation complexity. However, for a large size network with a very large size routing table of hundreds or thousands of entries, the cost, complexity and processing time does become a real issue. The latter will lead to a noticeable increase in the packet processing time at every router, which could be significantly reduced by a non-conventional signal formatting. In [6] PPM header processing (PPM-HP) scheme has been used to convert both the header address and routing table entries from a return-to-zero (RZ) format to a PPM format for a single wavelength routing system. Here for the first time we propose a WDM based all-optical router employing the PPM-HP. The advantages of this scheme are (i) significantly

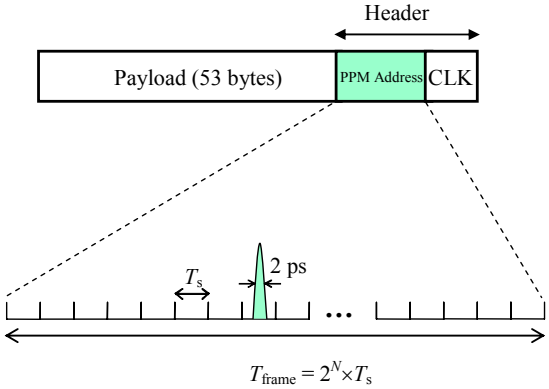

Figure 1: An optical packet with the PPM header address

reduced routing table entries, where each entry contains more than one PPM based header address, (ii) considerably reduced correlation processing time by using merely a single bitwise AND gate instead of a large number of gates with a low response-time, (iii) offering multiple transmitting modes (unicast, multi-cast and broadcast) embedded in optical layer, (iv) less complexity due to exclusion of the PPM address conversion module [7], and (v) using fewer components compared with the existing all-optical routing employing wavelength conversions [8-10] and all-optical flip-flops [11, 12]. The paper is organized as follows: after introduction, the correlation principle as well the PPM-HP node architecture is outlined in Section 2. The WDM router architecture incorporating PPM header address format is described in Section 3. Simulations results and discussion of the proposed WDM router are presented in Section 4. Finally, Section 5 will conclude the paper.

2. PPM Routing Table (PPRT)

A typical packet is composed of a header (clock and address) and payload bits. The clock signal is normally one bit and is used for synchronization within the router. In [6] both the header address and the routing table entries are based on the PPM format has been proposed as an alternative to the conventional non-return-to-zero (NRZ) and RZ signal formats [7]. A PPM based header address is composed of 2^N time slots T_s and a pulse of $\leq T_s$ duration, where N is the input address bit resolution. The position of the pulse corresponds to the target address decimal metric, see Figure 1. For example, a target address of "0011" with a decimal value of 3 is represented in a PPM format as "0001000000000000". It has been shown that PPM based routing scheme improves address correlation time compared with the conventional routing tables [6].

Table 1: The conventional and PPM based routing tables

Address patterns (N=4)	Output Port (M=3)	PPRT entries with 16 slots
0 0 0 0 0 0 0 1 0 1 0 0 1 0 0 1 1 0 1 1 1 1 1 1	1	E_1 Decimal values 0 1 4 9 11 15 PPM pulses
0 0 0 0 0 0 1 0 0 1 1 0 0 1 1 1 1 1 0 1 1 1 1 0	2	E_2 Decimal values 0 2 6 7 13 14 PPM pulses
0 0 0 0 0 0 0 1 0 0 1 1 0 1 0 1 1 0 0 0 1 0 1 0 1 1 0 0	3	E_3 Decimal values 0 1 3 5 8 10 12 PPM pulses

Table 1 illustrates a routing table for a traditional 4-bit binary address, where 16 possible addresses are grouped into M groups based on the intended target output ports. Here M = 3 representing the number of output ports. The 3rd column shows the PPRT entries E_m (m = 1,2,...M) of length $2^N \times T_s$ for each group. Note that the number of entries is reduced from 16 to 3 compared to the conventional RT, thus resulting in a reduced header address correlation time. A packet header address matching one or more patterns in a group can be switched to more than one output ports. At a very high bit rate R_b (in this case 160 Gb/s) generating a PPM pulse with an ultra short T_s is a challenging task, therefore here we kept T_s to be equal to T_b = 6.25 ps.

3. WDM Router Architecture

Figure 2 shows a block diagram of a $1\times M$ WDM router architecture composed of a $1\times L$ demultiplexer, L PPM-HPs, and M $L\times 1$ multiplexers, where L is the number of wavelengths. At the input, WDM packets at multiple-wavelengths (λ_1, λ_2 … and λ_L) are fed into a bank of PPM-HP modules via a WDM demultiplexer. Packets with the PPM format header address at specific wavelengths are processed at the PPM-HP modules before being

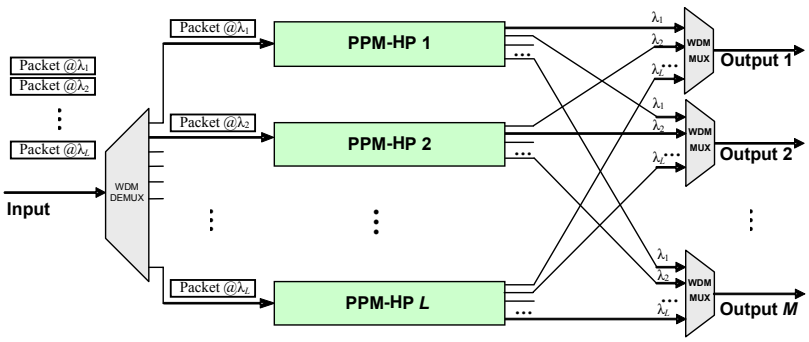

Figure 2: The WDM router architecture for $L = 2$ and $M = 3$

broadcasted to all $L\times1$ multiplexers. In contrast to existing schemes this architecture uses fewer number of laser sources since there is no need for wavelength conversion modules.

Figure 3 illustrate a schematic block diagram of $1\times M$ PPM-HP module. It is composed of an asynchronous clock extraction module (CEM), a PPM header address extraction module (PPM-HEM), a PPM routing table (PPRT), AND gates, a number of fibre delay lines (FDLs), a number of symmetric Mach-Zehnder based all-optical switches (OS), and an OS control module (OSC). The incoming optical packet $P_{in}(t)_{\lambda i}$ is applied via 1×3 splitter to the CEM, PPM-HEM and OS with the delays of 0, τ_{CEM} (required time for the clock extraction) and τ_{tot} (total required time for PPM address correlation), respectively. τ_{CEM} and τ_{tot} are the delayed required for clock extraction and PPM address correlation, respectively. The CEM, PPM-HEM and PPRT modules configurations are the same as those adopted in [6]. The extracted clock signal $c(t)$ and its delayed version $\alpha c(t - \tau_{PPRT})$ are applied to the PPM-HEM and PPRT, respectively. α is the 1×3 splitting coefficient. A PPRT is constructed by applying the delayed clock signal

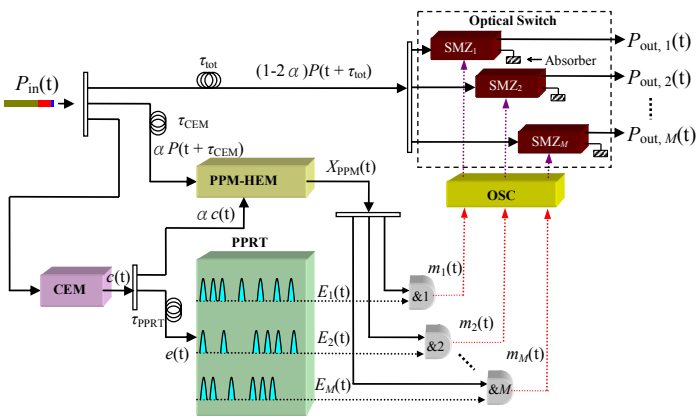

Figure 3: The schematic diagram of PPM-HP

Table 2: Simulation parameters

Parameter and description	Value
Data packet bit rate – $1/T_b$	160 Gb/s
Packet payload length	53 bytes (424 bits)
Wavelength 1 (f_1)	1552.52 nm (193.1 THz)
Wavelength 2 (f_2)	1544.52 nm (194.1 THz)
Data pulse width – FWHM	2 ps
PPM slot duration T_s ($=T_b$)	6.25 ps
Average transmitted power P_{in}	2 mW
Optical bandwidth	500 GHz
Splitting factor α	0.25
Number of control pulses	60
Average control pulse power	10 mW
Inject current to SOA	150 mA
SOA length	500 μm
SOA width	3×10^{-6} m
SOA height	80×10^{-9} m
SOA n_{sp}	2
Confinement factor	0.15
Enhancement factor	5
Differential gain	2.78×10^{-20} m^2
Internal loss	40×10^{2} m^{-1}
Recombination constant A	1.43×10^{8} s^{-1}
Recombination constant B	1.0×10^{-16} m^{3}s^{-1}
Recombination constant C	3.0×10^{-41} m^{6}s^{-1}
Carrier density transparency	1.4×10^{24} m^{-3}
Initial carrier density	3×10^{24} m^{-3}

through a number of fibre delay lines as in [6]. The packet header address, in PPM format, at the output of the PPM-HEM is correlated with the PPRT entries using a bank of all-optical AND gates. The correlated output pulses are applied to the OS via OSC to ensure the input packet is delivered to the intended output port. If more than one PPM pulse is located at the same position in more than one (or all) PPRT entries, then the input packet is broadcasted to multiple outputs (i.e. multicast) or all outputs (i.e. broadcast), respectively.

4. Results and Discussion

The proposed WDM router is simulated by using the Virtual Photonics simulation package (VPI^{TM}). Table 2 shows the all main simulation parameters. Six WDM optical packets with addresses of #0, #1, #3, #6, #9, #14 (decimal values), and #0, #4, #7, #10, #13, #15 are transmitted at wavelengths of λ_1 and λ_2, respectively. Packets are sequentially transmitted at 160 Gb/s with 1 ns inter-packet guard interval. Each packet is composed of a 1-bit clock, a 16-bit PPM address, and a 53-byte payload (ATM cell size) [13]. The time waveforms of six input WDM packets and their switched versions at the outputs are illustrated in Figure 4. Figure 4(a) shows the multiplexed and demultiplexed packets

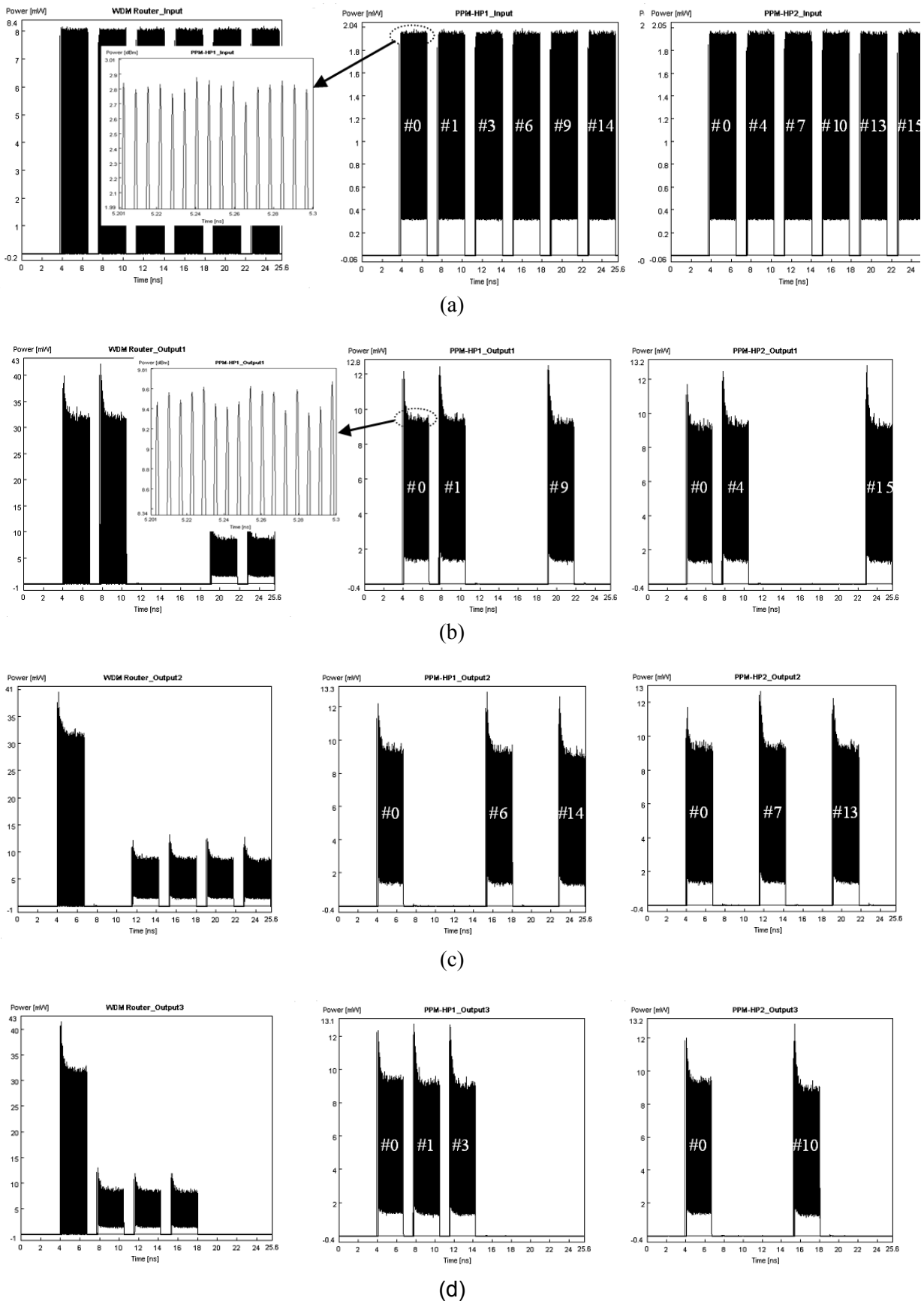

Figure 4: (a) packets at the inputs of the WDM router and PPM-HP1&2 (the inset shows the power fluctuation observed at the input of PPM-HP1), (b) packets observed at the output 1 of the WDM router and PPM-HP1&2 (the inset shows the power fluctuation observed at the output 1 of PPM-HP1), (c) packets observed at the output 2 of the WDM router, PPM-HP1&2, and (d) packets observed at the output 3 of the WDM router and PPM-HP1&2

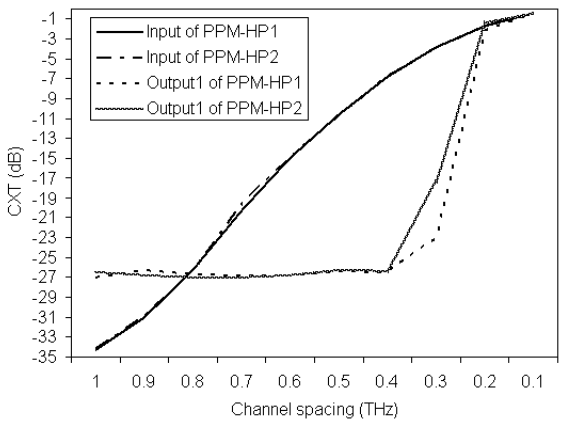

Figure 5: The channel crosstalk (CXT) observed at input of PPM-HP1&2 and output1 of PPM-HP1 & 2 against the channel spacing (the bandwidth of the WDM multiplexers and demultiplexer is 500 GHz)

waveforms at the input of the WDM router and PPM-HP1 & 2, respectively. The reason for pulses lower intensity being above the minimum level is due to a very narrow FWHM of 2 ps overlapping within a bit period of 6.25 ps. The overlap can be avoided by reducing the FWHM or the bit rate. Packets are switched to their corresponding output ports according to the PPRT in Table I. Packets at specific wavelengths observed at the outputs of the PPM-HP1&2 and the WDM ports are displayed in Figures 4(b), (c) and (d). The intensity overshot observed at the start of switched packets is due to the gain saturation of the SOA within the OS when injected with a packet stream, where the proceeding bits will experience a lower amplification gain. This can be minimized by decreasing the power of the input packet. There is a small intensity fluctuation of less than 0.3 dB with the packet stream as shown in the insets of Figures 4(a) and (b). Packet waveform with a larger intensity fluctuation may not be regenerated at the receiver employing a fixed threshold detector [14]. The intensity fluctuation can be further reduced by applying a series of control pulses to the OS to keep the switching window wide open to allow the entire packet to go through. Note that in Figures 4(b), (c) and (d), packets with addresses #0 and #1 are switched to all outputs (i.e. broadcast) and multiple outputs (i.e. multicast), respectively.

Channel crosstalk (*CXT*) is an important issue in DWDM core networks that will result in transmission and node functionality impairment [15], and is defined as:.

$$CXT = 10\log_{10}\left(P_{nt} / P_t\right) \quad (1)$$

where P_{nt} is the peak output signal power of all non-target channels (undesired wavelength) and P_t is the average output signal power of the target channel (desired wavelength). Two packets at λ_1 (packet 1 with address #4) and λ_2 (packet 2 with address #4) are sequentially applied to the input of the WDM router. The *CXT* observed at the input and output1 ports of PPM-HP1 & 2 for a range of channel spacing $\Delta f = f_2 - f_1$ is depicted in Figure 5. For 1 THz > Δf > 0.8 THz, CXT_{input} is much lower than the $\text{CXT}_{\text{output}}$ and increasing linearly for Δf < 0.8 THz. The CXT_{output} level is constant at -27 dB for 1 THz > Δf > 0.4 THz and increasing exponentially for Δf < 0.4 THz. Minimum level of CXT_{output} is limited by the contrast ratio of the extracted clock signals from the CEM.

Note that the $\text{CXT}_{\text{output}}$ is much lower than the CXT_{input} for 0.8 THz > Δf > 0.4 THz. The improvement in the CXT at the outputs of the PPM-HP is explained as follow. Signal emerging from the demultiplexer at wavelengths other than the desired wavelength display a very power level (< 0.4 mW), thus not affecting the CEM, PPM-HEM and AND gates (i.e. generating no additional control pulses to switch the entire packet to the output port of the OS). Packet therefore is directed to the non-target output port (i.e. the absorber port) of the optical switch.

4. Conclusions

The paper has presented an all-optical 1×*M* router architecture for a WDM core network. The PPM format adopted for the packet header address and the routing table entries offers fast correlation time and avoids the speed limitation imposed by the non-linear element based optical AND gates. Simulation results obtained show that this router can operate at 160 Gb/s with 0.3 dB of power fluctuations observed at the output ports and a channel CXT of ~ -27 dB at a channel spacing of greater than 0.4 THz and a demultiplexer bandwidth of 500 GHz.

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