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Applications of the Genetic Algorithm Optimisation Approach in the Design of High Efficiency Microwave Class E Power Amplifiers

Qing Lu

A thesis submitted in partial fulfilment of the requirements of the University of Northumbria at Newcastle for the degree of Doctor of Philosophy

Research undertaken in the Faculty of Engineering and Environment UK

2012
Abstract

In this thesis Genetic Algorithm Optimisation Methods (GA) is studied and for the first time used to design high efficiency microwave class E power amplifiers (PAs) and associated load patch antennas.

The difficulties of designing high efficiency PAs is that power transistors are highly non linear and classical design techniques only work for resistive loads. There are currently no high efficient and accurate procedures for design high efficiency PAs. To achieve simplified and accurate design procedure, GA and new design quadratic equations are introduced and applied.

The performance analysis is based on linear switch models and non linear circuitry push-pull methods. The results of the analytical calculations and experimental verification showed that the power added efficiency (PAE) of the PAs mainly depend on the losses of the active device itself and are nearly independent on the losses of its harmonic networks. Hence, it has been proven that the cheap material PCB FR4 can be used to design high efficiency class E PAs and it also shown that low Q factor networks have only a minor effect on efficiency, allowing a wide bandwidth to be obtained.

In additional, a new procedure for designing class E PAs is introduced and applied. The active device (ATF 34143) is used. Good agreement was obtained between predicted analyses and the simulation results (from Microwave Office (AWR) and Agilent ADS software). For the practical realization, class E PAs were fabricated and tested using PCB FR4. The practical results validate computer simulations and the PAE of the class E PAs are more than 71% and Gain is over 3.8 dB when input power ($P_{in}$) is equal to 14 dBm at 2 GHz.
Acknowledgement

I would like to thank my director of studies, Professor S. Danaher for his advice, guidance, support and constant enthusiasm throughout this work. I would also like to thank him for proof reading this thesis, and for giving me the opportunity to undertake my studies within his research group in the first place.

Sincere thanks also go to Professor Z. Ghassemlooy, Professor E. Korolkiewicz and Professor A. Sambell of Edinburgh Napier University, who are my first, second and third supervisors in that order, for providing invaluable help and advice throughout this work. Thanks must also go to the entire academic and technical members, especially Dr Edward Bentley, Dr David Johnson and Mr Wichian Ooppakaew for helping me out from time to time.

I would also like to thank my colleagues in the Optical Communications Research Group, both past and present, for sharing a few laughs with me and generally making my time in Newcastle a very enjoyable experience.

I specially thank my family, especially my wife – Xiao Liu, for their constant support, patience, understanding and encouragement throughout the duration of this work.
Declaration

I declare that the work contained in this thesis has not been submitted for any other award and it is my own work.

Name:

Signature:

Date:
To my dear Mum
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<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$c$</td>
<td>Speed of light in free space</td>
</tr>
<tr>
<td>$C_{block}$</td>
<td>DC block capacitor</td>
</tr>
<tr>
<td>$C_{ds}$</td>
<td>Drain-source capacitance</td>
</tr>
<tr>
<td>$C_{gs}$</td>
<td>Gate-source capacitance</td>
</tr>
<tr>
<td>$C_{gd}$</td>
<td>Gate-drain capacitance</td>
</tr>
<tr>
<td>$C_{pg}$</td>
<td>Pad capacitance at gate</td>
</tr>
<tr>
<td>$C_{pd}$</td>
<td>Pad capacitance at drain</td>
</tr>
<tr>
<td>$C_s$</td>
<td>The external capacitor for the active device</td>
</tr>
<tr>
<td>dB</td>
<td>Decibel</td>
</tr>
<tr>
<td>$f_s$</td>
<td>Design frequency</td>
</tr>
<tr>
<td>$f_0$</td>
<td>Resonant frequency for load networks</td>
</tr>
<tr>
<td>$G$</td>
<td>Green’s function</td>
</tr>
<tr>
<td>$G_1$</td>
<td>Radiation conductance</td>
</tr>
<tr>
<td>$G_{12}$</td>
<td>Mutual conductance</td>
</tr>
<tr>
<td>$g_m$</td>
<td>Transconductance</td>
</tr>
<tr>
<td>$H$</td>
<td>Thickness of the substrate of the microstrip line</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
</tr>
<tr>
<td>$I_{dc}$</td>
<td>DC drain current</td>
</tr>
<tr>
<td>$I_{max}$</td>
<td>Maximum current</td>
</tr>
<tr>
<td>$I_n$</td>
<td>$N^{th}$ component of the drain current</td>
</tr>
<tr>
<td>$J$</td>
<td>Current density</td>
</tr>
<tr>
<td>$k_{m,n}$</td>
<td>Wavenumber of $TM_{mn}$ modes in dielectric</td>
</tr>
<tr>
<td>$k_0$</td>
<td>Phase constant in free space ($\beta$)</td>
</tr>
<tr>
<td>$L$</td>
<td>Length of the microstrip line</td>
</tr>
<tr>
<td>$L_{choke}$</td>
<td>AC choke inductor</td>
</tr>
<tr>
<td>$L_d$</td>
<td>Drain bonding lead inductance</td>
</tr>
<tr>
<td>$L_g$</td>
<td>Gate bonding lead inductance</td>
</tr>
<tr>
<td>$L_s$</td>
<td>Source bonding lead inductance</td>
</tr>
<tr>
<td>$\Delta L$</td>
<td>Line extension due to fringing fields</td>
</tr>
<tr>
<td>$P_{dc}$</td>
<td>DC input power</td>
</tr>
<tr>
<td>$P_{out}$</td>
<td>AC output power</td>
</tr>
<tr>
<td>$R_d$</td>
<td>Drain bonding lead resistance</td>
</tr>
<tr>
<td>$R_{ds}$</td>
<td>Drain-source resistance</td>
</tr>
<tr>
<td>$R_g$</td>
<td>Gate bonding lead resistance</td>
</tr>
<tr>
<td>$R_i$</td>
<td>Gate charging resistance</td>
</tr>
</tbody>
</table>
$R_L$  
Load Resistance

$RL$  
Return loss

$R_{off}$  
Resistance of an active device when switched off

$R_{on}$  
Resistance of an active device when switched on

$R_s$  
Source bonding lead resistance

$tan \delta$  
Dielectric loss tangent

$T$  
Thickness of the copper patch

$V_n$  
$N^{th}$ component of the drain voltage

$V_{dc}$  
DC source voltage

$V_{gs}$  
Gate-source current

$V_{ds}$  
Drain-source voltage

$V_{dd}$  
Drain bias voltage

$V_{gg}$  
Gate bias voltage

$V_p$  
Pinch-off voltage

$V_{out}$  
Output voltage

$Y$  
Characteristic admittance

$W$  
Width of the microstrip line

$Z_{in}(n_{fs})$  
Harmonic impedance for the load
$Z_L$  Load impedance

$Z_0$  Characteristic impedance

$Z_S$  Source impedance

$\alpha$  Attenuation constant

$\zeta_n$  Phase of the $n^{th}$ harmonic component of the drain current

$\psi_n$  Phase of the $n^{th}$ harmonic component of the drain voltage

$\lambda$  Wavelength

$\theta$  Electrical length

$\gamma$  Propagation constant

$\varepsilon_0$  Permittivity of free space

$\varepsilon_r$  Relative permittivity of dielectric or dielectric constant

$\varepsilon_{reff}$  Effective permittivity of dielectric or dielectric constant

$\eta_0$  Impedance of free space

$\lambda_0$  Free-space wavelength

$\mu_0$  Absolute permeability

$\sigma_c$  Conductivity of conductor
## Glossary of Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>ac</td>
<td>Alternate current</td>
</tr>
<tr>
<td>ADS</td>
<td>Advanced design system</td>
</tr>
<tr>
<td>AIA</td>
<td>Active integrator circuit</td>
</tr>
<tr>
<td>AR</td>
<td>Axial ratio</td>
</tr>
<tr>
<td>CP</td>
<td>Circularly polarised</td>
</tr>
<tr>
<td>dc</td>
<td>Direct current</td>
</tr>
<tr>
<td>FET</td>
<td>Field effect transistor</td>
</tr>
<tr>
<td>GA</td>
<td>Genetic Algorithm</td>
</tr>
<tr>
<td>LP</td>
<td>Linearly polarised</td>
</tr>
<tr>
<td>Mline</td>
<td>Microstrip line</td>
</tr>
<tr>
<td>PA</td>
<td>Power amplifier</td>
</tr>
<tr>
<td>PAE</td>
<td>Power added efficiency</td>
</tr>
<tr>
<td>PCB</td>
<td>Print circuit board</td>
</tr>
<tr>
<td>PSO</td>
<td>Particle swarm optimisation</td>
</tr>
<tr>
<td>RF</td>
<td>Radio frequency</td>
</tr>
<tr>
<td>SA</td>
<td>Simulated annealing</td>
</tr>
<tr>
<td>v</td>
<td></td>
</tr>
<tr>
<td>Tline</td>
<td>Ideal lossless transmission line</td>
</tr>
<tr>
<td>--------------</td>
<td>---------------------------------</td>
</tr>
<tr>
<td>VSWR</td>
<td>Voltage standing wave ratio</td>
</tr>
<tr>
<td>WLAN</td>
<td>Wireless local area network</td>
</tr>
</tbody>
</table>
Parameters of Substrates

1) PCB FR4 Substrates

Substrate’s thickness: $H = 1.575 \text{ mm}$;

Loss tangent: $\tan \delta = 0.019$;

Dielectric constant: $\varepsilon_r = 4.3$;

Thickness of the copper patch: $T = 0.035 \text{ mm}$.

2) Duroid 5870 Substrates

Substrate’s thickness: $H = 1.575 \text{ mm}$;

Loss tangent: $\tan \delta = 0.0012$;

Dielectric constant: $\varepsilon_r = 2.33$;

Thickness of the copper patch: $T = 0.035 \text{ mm}$.
Chapter 1 Introduction

1.1 Background

Nowadays, high efficiency, low cost, broad bandwidth and size limitation are the challenges in modern wireless communication systems, which implies higher efficiency, cheap material application, low $Q$ factor and active integrated circuits need to be designed [1-13]. Furthermore, it required simplifying the procedure of circuit design and to increase the efficiency of power consumption [14-25].

To avoid these losses and save energy, it is necessary to design high efficiency power amplifiers (PAs) [23, 26-32], especially class E PAs, which can achieve significantly higher efficiency than for conventional class B or C PAs [33-35].

The first high efficiency class E PA was proposed by Sokal et al in 1975 [36] where an external capacitor was placed at the output and in parallel with the active device. A series resonant load circuit with a high $Q$ factor was used to obtain the required optimum impedance at the design frequency and very high impedances at the harmonics of the design frequency [2, 37, 38]. To reduce losses caused by transients in the voltage waveform the rise of the output voltage was delayed until after the active device was turned off and the output
voltage reached its minimum value with a slow turn on. Raab [39] by modelling the active device as a lossless switch derived the design equations assuming 50% duty cycle. Kazimierczuk [4] analysed this amplifier circuit for a range of $Q$ factor and duty cycle, while Gaudio [40] produced an exact analysis, where the characteristics of the active device were included. In [28] explicit design equations were derived where the effect of a finite value of the choke inductance was taken into account. Grebennikov [17, 28, 41] showed that the efficiency of power conversion reduces when the operation frequency is higher than the maximum frequency and if the VSWR of the load decreases. In [42, 43] Jaeger investigated how the losses in the load network and the finite switching time affect the efficiency of power conversion. A push-pull power amplifier with the two transistors driven with a phase difference of $180^0$ was used to improve the efficiency by reducing the even harmonics in the load resistor. In [26] a symmetrical push-pull amplifier had a load resistor connected in parallel with a capacitor and the active device was driven ‘on’ and ‘off’ within in each of the half-operating period.

There has been a continuous interest from researchers and industrial sectors in the application of high efficiency PAs. Recently, most of the challenges of design of high efficiency PAs are to simplify the design procedure and even increase the efficiency of the current PAs. [44, 45]

1.2 Aims and Objectives

From the above explanation and analysis, it can be seen that it is hard to design high efficiency PAs. Not only are relevant concepts of design of high efficiency PAs using nonlinear transistors lacking, but also lacking is a normal design procedure which increases both the cost and research period. To avoid this complexity, in this project a novel procedure
of design of high efficiency PAs has been described to reduce the research cost, and shorten the design period. This has been achieved by using a novel optimum Genetic Algorithm (GA) based method [46, 47].

In the design of power amplifiers, there are a large number of design parameters but an insufficient number of equations to obtain a unique solution, nor even to satisfy all the identified objectives. Consequently once the relative importance of the objectives has been decided it is possible to use stochastic search methods such as simulated annealing (SA) [48, 49], particle swarm optimisation (PSO) [50, 51] or GA [52, 53] to obtain a global solution from the multi-dimensional space. SA models a slow cooling process of metals in a liquid state; PSO models the social behaviour of a school of fish or flock of birds while GA models evolution and genetic recombination in nature. All the above optimization methods provide good solutions, without the necessity of applying rigorous mathematics to obtain closed form analytical solutions. It has been decided as discussed in the abstract to use GA to obtain optimum designs. In Chapter 2 the basic principles and implementation of GA are initially reviewed. Then GA is applied to optimise the design of a probe fed dual frequency matched patch antenna and the results of this research have been published [54].

To achieve high efficiency of the current class E PAs, the losses of required harmonic networks will be investigated. A new concept will be described, which has proved that high Q harmonic networks are not necessary [55]. This allowed a low $Q = 1.9$ to be used and efficiency of $85\%$ to be obtained. At microwave frequencies lumped elements of the load network are normally replaced by transmission lines. It is also shown in [56] the conditions to obtain good efficiency can be obtained by using a transmission line harmonic load network to satisfy the requirements up to the third harmonic. In chapter 3 the derivations of the published equations are reviewed for voltage/current waveforms and the required load
impedance at the design frequency to obtain maximum efficiency. Then new equations are derived for the voltage/current waveforms and for the optimum impedance at the design frequency.

To reduce the research cost, shorten the design period and save the energy of the wireless communication systems, a novel procedure for design of a high efficiency class E amplifier will be introduced in chapter 7. This uses the data sheet of an active device (ATF 34143) to obtain the turn-on resistance, $R_{on}$, and then the shunt capacitance, $C_s$, will be determined by using the obtained the $R_{on}$. The design of matching networks for the class E amplifier will be introduced and the simulation results will be given.

To reduce the fabrication cost, a cheap material (PCB FR4) substrate will be used to design the PAs and antennas. This will be the biggest challenge in this project and the final results will be compared with the other results, which were applied by using expensive materials, e.g. Duroid 5870 substrate.

1.3 Research Motivation and Contribution of the Thesis

1. Creation of GA optimisation methods for wireless communication systems design;

2. Creation of novel methods of reducing the losses of the active device (MESFET) and the load harmonic networks of the high efficiency class E PAs;

3. Implementation of GA for high efficiency class E PAs design;

4. Invention of a new research and design procedure of designing the harmonic network of the high efficiency class E PAs;
5. Practical results validate the above creations and inventions.

1.4 Organization for the Thesis

Chapter 2 initially reviews the basic concepts and the implementation of GA. In the case of a dual frequency antenna there are two objectives, as matching is required to be obtained at the two design frequencies. They are then used in the GA, to determine the optimum dimensions of the patch and the position of the probe feed, to satisfy the requirements for the return loss at each frequency. An excellent agreement is obtained between the predicted, modelled and practical results and based on this work a paper has been published [54].

In Chapter 3 the concepts of ideal class E power amplifiers are investigated. The active device is modelled as a switch in series with the $R_{on}$ resistance and an ideal harmonic load is assumed. For the ideal case when $R_{on}$ is equal to zero 100% efficiency of power conversion was obtained. It is found that if $R_{on}$ is finite the effect is to reduce input dc power, ac output power and cause the current/voltage waveforms to overlap.

In Chapter 4, the performance of the output stage for the class E amplifier is investigated, where the active device is still modelled as a switch in series with $R_{on}$. In [57] to reduce this loss caused by the harmonic currents, a high $Q$ factor of the circuit is used. However if a high $Q$ factor is used the efficiency bandwidth is reduced.

In Chapter 5 ideal lossless transmission lines (Tlines) are used in the initial design of harmonic networks for high efficiency power amplifiers and then practically realised using microstrip lines (Mlines). To reduce such complex analysis, the losses in a Mline are modelled as a Tline in series with a resistance. A novel method is proposed to determine this resistance as a function of the length of the Mline, which is realised using both inexpensive
PCB FR4 and expensive Duroid 5870 substrates (see Appendix D). Then for the above two line models, harmonic networks are designed up to the second and third harmonics and the obtained losses at the design frequency are compared. Finally, the effect of the losses with different harmonic networks on class E PAs is investigated.

In Chapter 6, the active device models are reviewed and the selected MESFET ATF34143 is described. A novel procedure for design of a high efficiency class E amplifier is introduced. Finally, the implementation and practical measurement are given by comparison.

Finally, Chapter 7 gives a summary of the thesis with overall conclusions and the suggestions for the future works.

These contributions are summarised in Fig. 1.1 and have led to the following publications and awards:
Figure 1.1: Summary of thesis contributions
1.5 List of Publications and Awards

**Journal Papers:**


**Conference Papers:**


Presentations:

Oral Presentations:


**Posters Presentations:**


2. “GA for Dual frequency patch antenna final”, 2009


**Research Related Awards:**

- 2011: Best PhD research student, Northumbria University, UK.

- 2011: IEEE UK-RI Communications Chapter Sponsorship (NOC 2011), Newcastle upon Tyne, UK.

- 2010: Best PhD research student, Northumbria University, UK.

- 2007: Best Poster Award, IET Competition, Durham, UK.
Chapter 2 Review of Genetic Algorithms and Case Study

2.1 Introduction

In the design of power amplifiers, antennas and their integration there are a large number of design parameters but an insufficient number of equations to obtain a unique solution or even to satisfy all the identified objectives. Consequently once the relative importance of the objectives has been decided it is possible to use stochastic search methods such as simulated annealing (SA) [48, 49], particle swarm optimisation (PSO) [50, 51, 58] or GA [52, 53, 59-64] to obtain a global solution from multi-dimensional space. SA models a slow cooling process of metals in a liquid state; PSO models the social behaviour of a school of fish or flock of birds while GA models evolution and genetic recombination in nature. All the above optimization methods provide good solutions without the necessity of applying rigorous mathematics [65] to obtain closed form analytical solutions. It has been decided as discussed in the abstract to use GA to obtain optimum designs. In this chapter the basic principles and implementation of GA is initially reviewed [61, 66-71]. Then GA is applied to optimise the design of a probe fed dual frequency matched patch antenna and the results of this research have been published [54].
2.2 Review of the Implementation for the Genetic Algorithm

The step by step implementation of the iterative process of the GA proposed by Holland [52] is shown in Fig 2.1,

![Flow chart of the GA Implementation](image)

Figure 2.1: Flow chart of the GA Implementation [52]

**Step 1:** The maximum, \( U \), and minimum, \( L \), values of each analogue parameter are specified to ensure that a suitable solution can be obtained. The number of bits or genes used to code the analogue parameters depends on the required accuracy of the final solution.

**Step 2:** The binary string of bits for each analogue variable are then sequentially co-joined into a global string called a chromosome. If there are ‘\( m \)’ bits in each chromosome each level \( a_i \), is specified by (2.1),

\[
\alpha_i = \frac{L + U - L}{2^{m-1}} n \quad n = 0, 1, 2 \ldots 2^{m-1}. \tag{2.1}
\]
Step 3: A selected number, \( n \), of chromosomes called a population is randomly selected out of the total number of chromosomes.

Step 4: The digital form of each selected chromosome is converted into an analogue form and the fitness determined, \( f(x_n) \). The total fitness function, \( F(x_n) \), is the sum of the chromosome. Fitness is evaluated,

\[
F \ x_n = \sum_{n=0}^{m-1} f(x_n). \tag{2.2}
\]

Step 5: The selection probability, \( P_{sn} \), of each chromosome for the next generation is determined,

\[
P_{sn} = \frac{f(x_n)}{F(x_n)} \tag{2.3}
\]

Step 6: The area of each segment in the roulette wheel shown below is proportional to the probability, \( P_{sn} \), of each chromosome,

![Roulette wheel selections: Before spin of the wheel.](image)

Figure 2.2: Roulette wheel selections: Before spin of the wheel.
Step 7: The roulette wheel is spun ‘n’ times and for each spin a chromosome is selected. Those chromosomes with high probability or having segments with a larger area are more likely to be selected more times. Those segments or the chromosomes not selected are not used in the next stage of the optimisation,

![Roulette wheel selection](image)

Figure 2.3: Roulette wheel selections: After spin of the wheel ten times.

Step 8: The random element of GA is further enhanced by using a crossover process where a number of bits or genes of selected pairs of chromosomes are exchanged.

To obtain the optimum solution rapidly the criteria for selecting pairs of chromosomes and genes is shown followed,

a) Mutation rate is biased towards least significant genes.

b) The mutation rate is gradually reduced.

c) The fitness function is gradually biased towards the optimum solution.

The iteration of the above process is run until a convergence is obtained to produce an optimum solution.

In the next section the GA optimisation method is applied to the design of a probe fed dual frequency patch antenna where there are four design variables and two objective functions.
2.3 Review and Basic Design Equations of a Patch Antenna

Patch antennas [44, 72-74] are used in many communication systems as they are compact, have low profile and their manufacturing costs are reduced by using printed circuit technology. The main disadvantage of these types of antennas is that they have narrow bandwidth and hence one approach is to increase the bandwidth so that more channels can be transmitted in wireless communication systems [10, 54, 55, 75, 76]. The alternative approach is to design the antenna to transmit information in multi frequency bands or at least in dual mode with different polarisations [73, 77]. Dual band patch antennas can be obtained using slots, stacked patches and shorting pins [78, 79].

In this section GA is used to obtain optimum dimensions, $a$ and $b$, of a rectangular patch antenna and the position of the probe feed $(X_p, Y_p)$ are shown in Fig. 2.4 for the antenna to be matched at two modes, $TM_{10}$ (1.9 GHz) and $TM_{01}$ (2.4 GHz),

![Figure 2.4: TM10 and TM01 modes of a patch antenna and four possible feed positions.](image-url)

16
The equation for the probe feed impedance \[ Z_{pf} = j2\pi f\mu H - \frac{\cos k + \cos k a - 2X_p}{2b\sin k} \]

\[ + \frac{b^2}{W_p^2 \pi^3} \sum_{n=1}^{\infty} \sin \frac{n\pi}{b} Y_p + \frac{W_p}{2} - \sin \frac{n\pi}{b} Y_p - \frac{W_p}{2} \left[ \cosh \frac{an}{b} \pi + \cosh \frac{a - 2X_p}{b} \pi \right] \]

\[ \frac{n^2 - \frac{bk}{\pi}}{n^2 \sinh \frac{an}{b} \pi \left( n^2 - \frac{bk}{\pi} \right)} \]  \hspace{1cm} (2.4)

The thickness of the dielectric substrate is \( H \), \( k^2 = \frac{\omega^2}{\mu \varepsilon_0 \varepsilon_{reff}} (1 - j/Q) \). \( Q \) is the total quality factor, \( W_p \) is the diameter of the probe feed and \( W_p^2 \) is the area of the probe feed which is assumed to be square.

In this design it is convenient to use effective dimensions of the patch and effective permittivity. The effective dimensions are defined in terms of wavelengths so that fringing electric fields present at the edges of the antenna are ignored. The electric field at the edges of the patch is partly in air and partly in the dielectric. It is convenient to replace the air and the dielectric substrates by one substrate having a single or an effective relative permittivity.

The effective dimensions of the patch and the effective permittivity for the TM\(_{10}\) and TM\(_{01}\) modes are shown below [72], where \( H \) is the thickness of the substrate.

\[ \varepsilon_{reff} a = \frac{\varepsilon_r}{2} + \frac{\varepsilon_r - 1}{2} 1 + \frac{12H}{b} \frac{-\frac{1}{2}}{\frac{1}{2}} \]  \hspace{1cm} (2.5)

\[ \varepsilon_{reff} b = \frac{\varepsilon_r}{2} + \frac{\varepsilon_r - 1}{2} 1 + \frac{12H}{a} \frac{-\frac{1}{2}}{\frac{1}{2}} \]  \hspace{1cm} (2.6)
From the above equations it can be seen that it is very difficult to apply analytical methods to determine the required four design variables, \( a, b, \varepsilon_{\text{reff}}(a) \) and \( \varepsilon_{\text{reff}}(b) \). Therefore, GA is used as shown in the following section, to obtain the optimum dimensions of the patch and the co-ordinates off the feed position.

\[
a = \frac{c}{2f_1 \varepsilon_{\text{reff}}(b)}; \quad (2.7)
\]

\[
b = \frac{c}{2f_2 \varepsilon_{\text{reff}}(a)}. \quad (2.8)
\]

2.4 Implementation of GA in the Design of Patch Antennas

In this section the range of the values of the four variables are initially derived and then three different objective functions are evaluated in the GA to find the optimum design of patch antennas.

Both the effective permittivity \( \varepsilon_{\text{reff}}(a) \) and \( \varepsilon_{\text{reff}}(b) \) are less than the relative permittivity of the FR4 PCB substrate \( \varepsilon_r = 4.3 \). Using the value of 4.3 in (2.7) and (2.8) then \( a = 38 \text{mm} \) and \( b = 29 \text{mm} \). However as \( \varepsilon_{\text{reff}}(a) \) and \( \varepsilon_{\text{reff}}(b) \) are both less than 4.3 these dimensions were increased to \( a_{\text{max}} = 42 \text{mm} \) and \( b_{\text{max}} = 37 \text{mm} \). The minimum values chosen are, \( a_{\text{min}} = 34 \text{mm} \) and \( b_{\text{min}} = 29 \text{mm} \).

The feed position is located in the first quadrant (see Fig.2.2) and hence the range of the feed co-ordinates assume are \( X_{p\text{max}} \approx \frac{a_{\text{max}}}{2} = 20 \text{mm} \), \( X_{p\text{min}} = 0 \), \( Y_{p\text{max}} \approx \frac{b_{\text{max}}}{2} = 16 \text{mm} \) and \( Y_{p\text{min}} = 0 \).
The return losses \((RL, RL_1, RL_2)\) at 1.85 GHz and \(RL_2\), at 2.4 GHz shown below are required to be optimised in order that the antenna is matched at the two frequencies,

\[
RL_1 = S_{11} \; 1.85 \text{ GHz} = 20 \log \frac{Z_{pp \; 1.85 \text{ GHz} -50}}{Z_{pp \; 1.85 \text{ GHz} +50}} \text{ dB}; 
\]

\[
RL_2 = S_{11} \; 2.4 \text{ GHz} = 20 \log \frac{Z_{pp \; 2.4 \text{ GHz} -50}}{Z_{pp \; 2.4 \text{ GHz} +50}} \text{ dB}. 
\]

GA can only determine the optimum design parameters by searching for either the minimum or maximum value of only one objective function. In this design as there are two objective functions given by (2.9) and (2.10) an optimum solution cannot be obtained directly. To ensure that the obtained return loss at each frequency is optimum, three different overall objective functions shown below were derived and used to determine the required values of the four design parameters.

\[
\text{Objval } A = RL_1 \; 1.85 \text{ GHz} + RL_2 \; 2.4 \text{ GHz} ; \quad (2.11a)
\]

\[
\text{Objval } B = RL_1 \; 1.85 \text{ GHz} + RL_2 \; 2.4 \text{ GHz} - RL_1 \; 1.85 \text{ GHz} - RL_2 \; 2.4 \text{ GHz} ; \quad (2.11b)
\]

\[
\text{Objval } C = 10 \times RL_1 \; 1.85 \text{ GHz} + RL_2 \; 2.4 \text{ GHz} - RL_1 \; 1.85 \text{ GHz} - RL_2 \; 2.4 \text{ GHz} . \quad (2.11c)
\]
For 20 and 100 iterations the obtained dimensions of the patch, feed position and the return loss at each frequency are shown in the Table 2.1,

<table>
<thead>
<tr>
<th></th>
<th>Objval A</th>
<th>Objval B</th>
<th>Objval C</th>
</tr>
</thead>
<tbody>
<tr>
<td>IT</td>
<td>20</td>
<td>100</td>
<td>20</td>
</tr>
<tr>
<td>a</td>
<td>39.2</td>
<td>39.2</td>
<td>39.3</td>
</tr>
<tr>
<td>b</td>
<td>30.1</td>
<td>30.1</td>
<td>30.2</td>
</tr>
<tr>
<td>Xp</td>
<td>12.6</td>
<td>12.6</td>
<td>12.4</td>
</tr>
<tr>
<td>Yp</td>
<td>8.9</td>
<td>8.7</td>
<td>8.9</td>
</tr>
<tr>
<td>RL₁ (1.85 GHz)</td>
<td>8.46</td>
<td>17.5</td>
<td>28.8</td>
</tr>
<tr>
<td>RL₂ (2.4 GHz)</td>
<td>72</td>
<td>65.7</td>
<td>18.7</td>
</tr>
</tbody>
</table>

Table 2.1: Obtained dimensions, probe position and return loss for the three objective functions after 20 and 100 Iterations.

After 100 iterations the return losses at the two frequencies are, Objval A ($RL_1 = 17.5$ dB, $RL_2 = 65.7$ dB) and Objval C ($RL_1 = 56.1$ dB, $RL_2 = 23.0$ dB). The return losses at the two frequencies are very different and hence not suitable in a practical design. However for Objval B both returns losses are very good and very close to each other ($RL_1 = 36.7$ dB, $RL_2 = 35$ dB). Hence these optimum dimensions for the patch and the feed position shown below are used in the fabrication of the patch antenna,

$$a = 39.2 \text{ mm}, \quad b = 30.2 \text{ mm}, \quad X_p = 12.4 \text{ mm and } Y_p = 8.7 \text{ mm}.$$
2.5 Comparison of Predicted, Modelled and Practical Results of the Designed Antenna

The photograph of the fabricated antenna is shown in Fig. 2.5 was fabricated and tested,

![Photograph of the fabricated patch antenna.](image)

Figure 2.5: Photograph of the fabricated patch antenna.

The frequency responses of the return loss obtained using the Agilent network analyser (N5230A) and from the GA programme are shown in Fig. 2.6. At 1.85 GHz frequency there is an excellent agreement and at 2.4 GHz there is a difference of 2 % between the predicted and the practical results.
Figure 2.6: Predicted and practical results for the return loss

The simulated polar patterns using AWR software of the antenna at 1.85 GHz and 2.4 GHz are shown in Fig. 2.7 where a good Radiation Pattern of the patch antenna between the two has been obtained.
In this chapter a literature review and a detailed implementation of GA were discussed. Then in the GA optimisation three objective functions were evaluated in the design of a dual frequency matched antenna. For two of the objective functions the obtained return loss was very different at the two frequencies however the third objective function produced excellent and very close results for the return loss. The above result shows how important it is to choose the most suitable objective function. The optimum dimensions for the patch and for the feed position obtained were used to fabricate the antenna. The measured return loss the two frequencies was approximate -30 dB and there was a very good agreement between the predicted and practical results. Therefore, the GA optimization methods could be used to design of high efficiency power amplifiers (PAs) and active integrated antennas (AIAs) in next few chapters.

Figure 2.7: Polar patterns at (a) 1.85 GHz and (b) 2.4 GHz

2.6 Summary

In this chapter a literature review and a detailed implementation of GA were discussed. Then in the GA optimisation three objective functions were evaluated in the design of a dual frequency matched antenna. For two of the objective functions the obtained return loss was very different at the two frequencies however the third objective function produced excellent and very close results for the return loss. The above result shows how important it is to choose the most suitable objective function. The optimum dimensions for the patch and for the feed position obtained were used to fabricate the antenna. The measured return loss the two frequencies was approximate -30 dB and there was a very good agreement between the predicted and practical results. Therefore, the GA optimization methods could be used to design of high efficiency power amplifiers (PAs) and active integrated antennas (AIAs) in next few chapters.
Chapter 3 Literature Review and Theory of Class E Power Amplifiers

3.1 Introduction

A high efficiency class E power amplifier was first proposed by Sokal et al [36] where an external capacitor was placed at the output and in parallel with the active device. A series resonant load circuit with a high $Q$ factor was used to obtain the required optimum impedance at the design frequency and very high impedances at the harmonics of the design frequency. To reduce losses caused by transients in the voltage waveform the rise of the output voltage was delayed until after the active device was turned off and the output voltage reached its minimum value with a slow turn on. Raab [39] by modelling the active device as a lossless switch derived the design equations assuming 50% duty cycle. Kazimierczuk [4] analysed this amplifier circuit for a range of $Q$ factor and duty cycle, while Gaudio [40] produced an exact analysis where the characteristics of the active device were included. Grebennikov [17, 28] showed that the efficiency of power conversion reduces when the operation frequency is higher than the maximum frequency and if the VSWR of the load decreases, which will be proved in this project. In [42, 43] Jaeger investigated how the losses in the load network and the finite switching time affect the efficiency of power conversion. A
push-pull power amplifier with the two transistors driven with a phase difference of 180° was used to improve the efficiency by reducing the even harmonics in the load resistor. In [81] a symmetrical push-pull amplifier had a load resistor connected in parallel with a capacitor and the active device was driven ‘on’ and ‘off’ within in each of the half-operating period. This allowed a low $Q = 1.9$ to be used and efficiency of 85 % was obtained [19]. At microwave frequencies lumped elements of the load network are normally replaced by transmission lines. It is also shown in [3, 35, 81, 82] the conditions to obtain good efficiency can be obtained by using transmission line harmonic load network to satisfy the requirements up to the third harmonic. In this chapter the derivations of the published equations are reviewed for voltage/current waveforms and the required load impedance at the design frequency to obtain maximum efficiency. Then new equations are derived for the voltage /current waveforms and for the optimum impedance at the design frequency.

### 3.2 Review of the Derivation of the Voltage / Current Waveforms and Optimum Load Impedance for a Class E Amplifier

This section reviews the equations for the voltage and current waveforms assuming the turn on resistance of the active device, $R_{on}$, is equal and not equal to zero [57, 83]. The conditions to eliminate transients in the voltage/ current are applied. Then with $R_{on}$ not equal to zero new equations are derived where the conditions for transients in the voltage and current waveforms are relaxed.
3.2.1 Derivations of the Equations Assuming $R_{on}$ the Turn on Resistance of an Active Device are Equal to Zero

A simple equivalent output circuit of an ideal class E amplifier is shown in Fig. 3.1 where a practical active device is modelled by a switch and a turn on resistance, $R_{on}$, and an external capacitor, $C_s$, is placed at the output terminals of the active device. Applying the below conditions ensures that the overlap of voltage and current waveforms is minimised [16].

Figure 3.1: Model of an ideal class E amplifier

a) $L_{choke}$ is lossless and large so that only dc current, $I_{dc}$, flow through it.

b) $C_s$ is an external linear capacitance and much larger than the inherent non-linear capacitance of the active device.
c) The switch has an infinite ‘off’ resistance and a linear ‘on’ resistance which is assumed to be zero in this section.

d) Duty cycle is 50 %;

e) To ensure that only a current at the design frequency flows in the load resistor $R_L$ the input impedance of the load harmonic network at the design and harmonic frequencies are given below,

\[
Z_{in}(f_s) = Z_{opt} = R_{opt} + j X_{opt}; \quad (3.1a)
\]

\[
Z_{in} n f_s = \infty \quad \text{for } n = 2,3 \ldots; \quad (3.1b)
\]

f) The load current $I_R(t)$ at the design frequency is given by (3.2) where the amplitude, $a$, and phase, ‘$\varphi$’, need to be determined to ensure that the voltage/current waveforms do not overlap and maximum efficiency is obtained,

\[
i_R(t) = a I_{dc} \sin \omega_s t + \varphi. \quad (3.2)
\]

When the switch is open in Fig. 3.1 during the period $0 < t < T_s/2$ the current in the capacitor $C_s$ is,

\[
C_s \frac{d\psi_s(t)}{dt} = i_c(t) = i_s(t) = I_{dc}(1 - a \sin \omega_s t + \varphi); \quad (3.3)
\]

Integrating (3.3) shows that the switch voltage is given by (3.4),

\[
v_s(t) = \frac{I_{dc}}{\omega_s C_s} \omega_s t + a \cos \omega_s t + \varphi - \cos \varphi. \quad (3.4)
\]
To obtain the constants, $\phi$ and $a$ the following two conditions are used for the switch voltage waveform [84] which ensures transients in the voltage and current waveforms are eliminated.

1) The switch voltage $v_s$, $0 = v_s \frac{T_s}{2} = v_s \frac{T_s}{2} = 0$ which ensures that when the switch closes the transient response in the voltage waveform is eliminated as is the $\frac{1}{2}CV^2$ loss in the capacitor. For this condition from (3.4) in can be shown that $acos\phi = \frac{\pi}{2}$;

2) The other requirement is that at $t = \frac{T_s}{2}$ the switch voltage must be gradually decreasing and hence $\frac{dv_s}{dt} \frac{T_s}{2} = 0$ and for this condition the current in the capacitor is zero. Therefore the transient response in the current waveform is eliminated as are $\frac{1}{2}Li^2$ losses in the inductor. Substituting this condition in (3.4) it can be shown $asin\phi = -1$.

From the above two conditions, it can be readily shown that $a = 1.862$ and $\phi = -32.32^0$.

The equations over the whole period for the switch voltage and current waveforms are summarized in (3.5a) and (3.5b).

\[
\begin{align*}
v_s(t) &= \frac{l_{dc}}{\omega_s C_s} \omega_s t + a \cos \omega_s t + \phi - \cos \phi \\
&\begin{cases} 
0 & (0 \leq t \leq \frac{T_s}{2}) \\
\frac{T_s}{2} & (\frac{T_s}{2} \leq t \leq T_s)
\end{cases}
\end{align*}
\]  

(3.5a)

\[
\begin{align*}
i_s(t) &= l_{dc} \left(1 + \sin \omega_s t + \phi \right) \\
&\begin{cases} 
0 & (0 \leq t \leq \frac{T_s}{2}) \\
\frac{T_s}{2} & (\frac{T_s}{2} \leq t \leq T_s)
\end{cases}
\end{align*}
\]  

(3.5b)

Integrating (3.5a) it can be shown that

\[
V_{dc} = \frac{l_{dc}}{\pi \omega_s C_s};
\]  

(3.6)
Values \( V_{dc} = 5 \text{ V}, \ C_s = 1 \text{ pF}, f_s = 2 \text{ GHz} \) will be used in all the relevant equations in this and next chapter. The above equations are plotted in Fig. 3.2 showing that the two waveforms do not overlap and meet the above two conditions.

To obtain the optimum input of the load network it is necessary to determine the parameters of the switch voltage at the design frequency (see (3.7)) from (3.5a). From the Fourier analysis it can be shown that the amplitude and phase for the below equation are, \( a_v = 0.28 \) and \( \varphi_v = 16.57^\circ \).

\[
V_s(t) = a_v I_{dc} \sin(\omega_s t + \varphi_v).
\]  

(3.7)
Using (3.2) and (3.7) the optimum input impedance of the ideal load harmonic is given below [36],

\[ Z_{opt} = \frac{a_v e^{j\phi_v}}{ae^{j\phi}} = \frac{0.28015}{2\pi f_s C_s} e^{j49.0524^\circ} = R_{opt} + jX_{opt}. \]  

(3.8)

For the above values of \( C_s \) and \( f_s \), the real and imaginary parts of the optimum impedance are plotted in Fig 3.3 over the frequency range 1.4 to 2.6 GHz.

![Graph](image)

Figure 3.3: the optimum input impedance of the ideal load harmonic Vs design frequency \((f_s)\)

### 3.2.2 Derivations of the Equations for Voltage/Current Waveforms for \( R_{on} \) not equal to Zero

A practical active device does not behave as an ideal lossless switch \((R_{on} \neq 0)\) and in this section based on [16] the effect of ‘\( R_{on} \)’ on the switch voltage/current waveforms is investigated. The details of the derivation for the voltage and current waveforms are given in Appendix B1.
For $R_{on} \neq 0$ it is convenient to define $v_{s1}(t)$ as the switch voltage during the period $(0 \leq t \leq T_s/2)$ when the switch is open and voltage $v_{s2}(t)$ in the period $(T_s/2 \leq t \leq T_s)$ when the switch is closed. To derive the equations for the voltage/ current waveforms and for the parameters ‘$a_r$’ and, ‘$\varphi_r$’, the following two conditions are applied.

1. $v_{s1}(0) = v_{s2}(T_s)$ to ensure that the voltage waveform is periodic;
2. $v_{s1}(T_s/2) = v_{s2}(T_s/2) = 0$ to ensure that transients in the voltage and current waveforms are eliminated.

For the ‘on’ state ($T_s/2 \leq t \leq T_s$) when the switch is closed the current in $R_{on}$ is $I_{dc}(1 - a_r \sin(\omega_s t + \varphi_r))$. During this period the switch voltage is given by,

\[ v_{s2} = R_{on} I_{dc} (1 - a_r \sin(\omega_s t + \varphi_r)). \] (3.9a)

When $t = T_s$ then from the above equation

\[ v_{s2} T_s = R_{on} I_{dc} (1 - a_r \sin \varphi_r) = v_{s1}(0). \] (3.9b)

Applying condition (2) when $t = T_s/2$, $V_{s2}(T_s/2) = R_{on} I_{dc}(1 + a_r \sin \varphi_r) = 0$ and hence

\[ a_r \sin \varphi_r = -1 \] (3.10)

Using (3.10) $v_{s1} 0 = v_{s2} T_s = 2R_{on} I_{dc}$. 

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For the ‘off’ state (0 ≤ t ≤ \( \frac{T_s}{2} \)) the switch is open and the current in the capacitor \( C_s \) is

\[
i_s(t) = I_{dc}(1 - a_r \sin \omega_s t + \phi_r).
\]  

(3.11)

The voltage across the capacitor \( v_{s1}(t) \) is given by

\[
\frac{dv_{s1}(t)}{dt} = \frac{I_{dc}}{C_s} (1 - a_r \sin \omega_s t + \phi_r).
\]  

(3.12)

Integrating the above equation it can be shown that

\[
v_{s1} = \frac{I_{dc}}{\omega_s C_s} \omega_s t + a_r \cos \omega_s t + \phi_r - \cos \phi_r + 2R_{on}I_{dc}
\]  

(3.13)

It is interesting to note that substituting (3.10) into (3.12) when \( t = T_s/2 \) the derivative \( dv_{s1}(t)/dt \) is also equal to zero. This is the same results as shown in the previous section when \( R_{on} = 0 \) which ensures that transients in the voltage and current waveforms are eliminated.

Using the condition (1) in (3.13), it can be shown that

\[
a_r \cos \phi_r = \frac{\pi}{2} + R_{on} \omega_s C_s.
\]  

(3.14)

From (3.10) and (3.14) the equations for the two parameters ‘\( a_r \)’ and ‘\( \phi_r \)’ are shown below,

\[
a_r = 1 + \frac{\pi}{2} + \omega_s C_s R_{on} \frac{1}{2} \left( \frac{1}{2} \right);
\]  

(3.15)

\[
\tan \phi_r = \frac{-1}{\frac{\pi}{2} + \omega_s C_s R_{on}}.
\]  

(3.16)
The equations for the switch voltage and current waveforms over a complete period are given in (3.17) and (3.18),

\[
\begin{align*}
    v_s(t) &= \frac{I_{dc}}{\omega_s C_s} \omega_s t + a_r \cos \omega_s t + \phi_r - \cos \phi_r - 2R_{on}I_{dc} \quad 0 \leq t \leq \frac{T_s}{2} ; \\
    R_{on}I_{dc} \left(1 - a_r \sin \omega_s t + \phi_r\right) &\quad \frac{T_s}{2} \leq t \leq T_s.
\end{align*}
\] (3.17)

\[
\begin{align*}
    i_s(t) &= I_{dc} \left(1 - a_r \sin \omega_s t + \phi_r\right) \quad 0 \leq t \leq \frac{T_s}{2} ; \\
    &\quad \frac{T_s}{2} \leq t \leq T_s.
\end{align*}
\] (3.18)

To plot the above equations it is necessary to obtain \( I_{dc} \). In terms of a specified value of \( V_{dc} \), this is obtained by integrating (3.19),

\[
V_{dc} = \frac{1}{T_s} \int_0^{T_s} v_{s1} \, t \, dt + \frac{1}{T_s} \int_{\frac{T_s}{2}}^{T_s} v_{s2} \, t \, dt .
\] (3.19)

In appendix B2 a simplified equation for \( I_{dc} \) (see (3.20)) can be derived,

\[
I_{dc} = \frac{V_{dc}}{\pi \omega_s C_s + \frac{3}{2} R_{on} + \frac{\omega_s C_s R_{on}}{\pi}^2}.
\] (3.20)

It is interesting to note that there is an error in the above equation for \( I_{dc} \) in [20] as expressed as

\[
I_{dc} = \frac{V_{dc}}{\pi \omega_s C_s + 2R_{on} + \pi \omega_s C_s R_{on}^2}.
\]
The effect of $R_{on}$ (0 to 5Ω) on $a_r$, $\phi_r$, and $I_{dc}$ is summarised in Table 3.1.

<table>
<thead>
<tr>
<th>$R_{on}$</th>
<th>$a_r$</th>
<th>$\phi_r$ (°)</th>
<th>$I_{dc}$ (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1.862</td>
<td>-32.482</td>
<td>0.197</td>
</tr>
<tr>
<td>1</td>
<td>1.873</td>
<td>-32.275</td>
<td>0.186</td>
</tr>
<tr>
<td>2</td>
<td>1.883</td>
<td>-32.071</td>
<td>0.176</td>
</tr>
<tr>
<td>3</td>
<td>1.894</td>
<td>-31.869</td>
<td>0.167</td>
</tr>
<tr>
<td>4</td>
<td>1.905</td>
<td>-31.670</td>
<td>0.159</td>
</tr>
<tr>
<td>5</td>
<td>1.915</td>
<td>-31.472</td>
<td>0.152</td>
</tr>
</tbody>
</table>

Table 3.1: Effect of $R_{on}$ on the parameters $a_r$, $\phi_r$ and $I_{dc}$.

Figures below shows how $R_{on}$ (0 to 5 Ω) affects the voltage and current waveforms,

Figure 3.4: Switch waveforms: (a) voltage and (b) current with the variable resistances ($R_{on}$) (in Ω)
1) From Fig.3.4 the following conclusion can be made. In the period \( \frac{T_s}{2} \leq t \leq T_s \) as \( R_{on} \) increases the peak current decreases and the peak voltage increases. This causes the ac output power to decrease, the overlap between the switch voltage and current waveforms increases while the power dissipated in \( R_{on} \) increases;

2) As \( I_{dc} \) decreases as \( R_{on} \) increases the dc input power decreases;

Consequently the above two effects cause the efficiency of dc to ac conversion to decrease.

To investigate how \( R_{on} \) affects the optimum input impedance at the design frequency it is necessary to determine the magnitude and angle of ‘\( K_f \)’ in (3.21).

\[
v_s(t) = 2 \ k_f \ \cos(\omega_s t + \phi) = 2 \ \frac{v_s}{T_f} \ cos(\omega_s t + \frac{\pi}{2} + \phi).
\]

(3.21)

Where

\[
K_f = \frac{1}{T_f} \ \int_0^{\frac{T_s}{2}} v_s_1 \ \ t \ e^{-j\omega_s t} dt + \int_{\frac{T_s}{2}}^{T_s} v_s_2 \ \ t \ e^{-j\omega_s t} dt
\]

(3.22)

The optimum input impedance of the external load harmonic network is given in (3.23).

\[
Z_{opt} = \frac{v_s(\omega_s t)}{I_{R}(\omega_s t)} = \frac{2 \ k_f}{a_{R}I_{dc}} e^{j(\frac{\pi}{2} + \phi - \phi_r)}.
\]

(3.23)
Table 3.2 shows (see appendix B.2) how $R_{on}$ (0 to 5Ω) affects the optimum impedance at the
design frequency.

| $R_{on}$ (Ω) | $2|k_t|$ | $\theta_t$ (º) | Re($Z_{opt}$) (Ω) | Im($Z_{opt}$) (Ω) |
|-------------|----------|---------------|-----------------|-----------------|
| 0           | 8.194    | 16.571        | 14.611          | 16.839          |
| 1           | 7.650    | 18.222        | 13.945          | 16.913          |
| 2           | 7.165    | 19.917        | 13.283          | 16.995          |
| 3           | 6.732    | 21.653        | 12.622          | 17.073          |
| 4           | 6.344    | 23.433        | 11.964          | 17.152          |
| 5           | 5.994    | 25.253        | 11.309          | 17.230          |

Table 3.2: Effect of $R_{on}$ on the optimum load impedance

3.2.3 Derivations of New Equations for the Voltage/Current Waveforms and Optimum Impedance

In the previous section the parameters ‘$a_r$’ and ‘$\phi_r$’ were obtained to ensure that transients in
the voltage/current waveforms and losses $\frac{1}{2}L_i^2$, $\frac{1}{2}CV^2$ were eliminated. In this section these conditions are not imposed and new equations are derived for the voltage/current waveforms and for the load optimum impedance at the design frequency. This has been done to investigate if this approach can reduce the overlap of the voltage and current waveforms and hence improve efficiency. Details of how the efficiency is affected using the new equations are discussed in the next chapter.
As in the previous section, the voltage \( v_{s1}(t) \) is present in the period \( (0 \leq t \leq \frac{T_s}{2}) \) and voltage \( v_{s2}(t) \) is present during the period \( (\frac{T_s}{2} \leq t \leq T_s) \), which is given by

\[
v_s(t) = v_{s1}(t) \quad 0 \leq t \leq \frac{T_s}{2} + v_{s2}(t) \quad (\frac{T_s}{2} \leq t \leq T_s)
\]

(3.26)

Where

\[
v_{s1}(t) = \frac{I_{dc}}{\omega_s C_s} \omega_s t + a_r \cos \omega_s t + \phi_r - \cos \phi_r + R_{on} I_{dc} (1 - a_r \sin \phi_r). \quad 0 \leq t \leq \frac{T_s}{2};
\]

(3.27a)

\[
v_{s2}(t) = R_{on} I_{dc} (1 - a_r \sin (\omega_s t + \phi_r)). \quad 0 \leq t \leq \frac{T_s}{2};
\]

(3.27b)

To obtain the values of ‘\( a_r \)’ and ‘\( \phi_r \)’ the following two conditions are imposed.

1) To ensure that the voltage waveform is periodic \( v_{s1}(0) = v_{s2}(T_s) \)

2) To make the switch voltage waveforms continuous \( v_{s1}(\frac{T_s}{2}) = v_{s2}(\frac{T_s}{2}) \) but not equal to zero.

Applying the above conditions to (3.27a) and (3.27b) results in a quadratic equation for ‘\( a_r \)’ and ‘\( \phi_r \)’, (see Appendix B.3)

\[
1 + R_{on}^2 \omega_s^2 C_s^2 4a_r^2 \cos^2 \phi_r - 4\pi a_r \cos \phi_r + (\pi^2 - 4R_{on}^2 \omega_s^2 C_s^2 a_r^2) = 0
\]

(3.28)
It is difficult to obtain analytically the two roots \((a_r, \varphi_r)\) of (3.28). A three dimensional graph shown in Fig 3.7 was initially used to determine the range of the two parameters, \(a_r\) (1.7~2.3mm) and \(\varphi_r\) (-27°~ -34°). These ranges of values were then used in a MATLAB programme (see appendix B.4) to determine the two parameters.

![Graph](image)

Figure 3.5: Optimum solutions \(Y(a_r, \varphi_r)\) of (3.26) using variable \(a_r\) and \(\varphi_r\)

For the new equations Fig. 3.6 shows the voltage and current waveforms and as expected in both waveforms there are now sharp discontinuities.

![Waveforms](image)

Figure 3.6: Switch waveforms: (a) voltage and (b) current with the variable resistors \((R_{\text{on}})\) (in \(\Omega\))
The obtained parameters \(a_r\), \(\varphi_r\), \(I_{dc}\), \(2|k_1|\), \(\theta_r\), and \(Z_{opt}\) for \(R_{on}\) 0 to 5 \(\Omega\) are shown in Table 3.3.

| \(R_{on}\) (\(\Omega\)) | \(a_r\) | \(\varphi_r\) (\(^\circ\)) | \(I_{dc}\) (A) | \(2|k_1|\) | \(\theta_r\) (\(^\circ\)) | \(\text{Re}(Z_{opt})\) (\(\Omega\)) | \(\text{Im}(Z_{opt})\) (\(\Omega\)) |
|----------------|---------|----------------|-----------|----------|----------------|----------------|----------------|
| 0              | 2.407   | -49.270        | 0.108     | 7.957    | 9.256          | 15.946         | 26.057         |
| 1              | 2.389   | -48.185        | 0.107     | 7.655    | 10.989         | 15.302         | 25.654         |
| 2              | 2.414   | -47.973        | 0.103     | 7.371    | 12.484         | 14.592         | 25.736         |
| 3              | 2.375   | -50.788        | 0.088     | 6.973    | 8.633          | 16.899         | 28.596         |
| 4              | 2.470   | -47.696        | 0.095     | 6.867    | 15.426         | 13.168         | 25.985         |
| 5              | 2.309   | -50.847        | 0.081     | 6.481    | 8.510          | 17.627         | 29.767         |

Table 3.3: Input impedance of the external load harmonic network vs. turn ‘on’ resistor \((R_{on})\) using optimum values of \(a_r\), \(\varphi_r\), \(2|k_1|\), and \(\theta_r\)

Table 3.3 shows that for the new equation \(R_{opt}\) has now increased and this would suggest that ac output power would also increase. The effect on the efficiency by the sharp discontinuities in the two waveforms is investigated in the next chapter.

### 3.3 Summary

In this chapter it has been shown that for \(R_{on}\) equal to zero and applying the required conditions the transients in the voltage/current waveforms are eliminated and the two waveforms do not overlap. For \(R_{on}\) not equal to zero two approaches have been used to determine the parameters \(a_r\) and \(\varphi_r\) of the two waveforms. One approach was to eliminate
sharp changes in the voltage/current wave forms and the other was to allow sharp changes in both waveforms. In both cases as $R_{on}$ is not equal to zero there is now an overlap in the two waveforms which must lead to the reduction in the efficiency of dc to ac power conversion.

The effect of losses due to the harmonic currents in the load resistor, $R_{on}$, and losses in the load harmonic network will be investigated in the next chapter. This investigation will be carried out using the equation derived in this chapter. Then these results will then be compared with those obtained using Agilent ADS and AWR (Microwave Office) software where the nonlinear circuits are analysed using Harmonic Balance method.
Chapter 4 Overview the Effect of Amplifier Losses on the Efficiency of D.C. to A.C. Power Conversion

4.1 Introduction

In the previous chapter the ideal load harmonic network has optimum input impedance at the design frequency and an open circuit at all harmonics of the design frequency. Consequently no power is dissipated in the load resistor $R_{opt}$ by the harmonic currents and the only power loss is in the $R_{on}$ resistance. As it is not possible to realise such an ideal load harmonic network some power will always be dissipated in $R_{opt}$ by the harmonic currents. In the design of a load harmonics network it is important to investigate the power loss due to the harmonic currents and how this loss affects efficiency of power conversion. In this chapter the ideal harmonic load is replaced by a series resonant circuit, as it could operate as a simply patch antenna. The effect of the $Q$ factor on the losses caused by the harmonic currents in $R_{opt}$ and on the efficiency is investigated using GA. These losses and their effect on efficiency are then compared with losses that occur in the resistance $R_{on}$. Finally different load harmonic networks are designed and the effect of losses in these networks on efficiency is investigated.
4.2 Effect of the Load Harmonic Currents on Efficiency

Fig. 4.1(a) shows an ideal load harmonic network for a class E amplifier. A simple practical equivalent circuit of the ideal network is a series resonant circuit having a high ‘Q’ factor shown in Fig. 4.1(b) [85]. In the investigation carried out in this section it is assumed that $R_{on}$ is equal to zero so that the losses in the load circuit are only due to the harmonic currents flowing in the load resistance $R_{opt}$.

\[ Z_{in}(f_0) = Z_{opt} = R_{opt} + jX_{opt} \]
\[ Z_{in}(n f_0) = \infty \quad \text{for } n = 2, 3, ... \]

Figure 4.1: Simplified form of the load harmonic network

The efficiency of dc to ac power conversion is defined as $\eta = P_{out}/P_{dc} \times 100\%$ where $P_{out}$ is the output ac power developed in the resistor $R_{opt}$ and $P_{dc}$ is the dc input power obtained from the dc supply. From (3.6) it can be shown that $V_{dc} = I_{dc}/(\pi \omega_s C_s)$ and hence $P_{dc} = I_{dc}^2/(\pi \omega_s C_s)$ For the ideal load harmonic network only current at the design frequency can flow in the load resistance $R_{opt}$ and the output ac power $P_{out} = (a I_{dc})^2 R_{opt}$, $R_{opt}$ is given by (3.9), $a = 1.862$ (see chapter 3) and hence it can be shown that the efficiency $\eta$ is 100%.
To investigate the losses due to the harmonic currents flowing in the resistance $R_{\text{opt}}$ it is useful to replace the ideal harmonic network by the series resonant circuit where the ‘$Q$’ factor can be modified.

For a typical value of $C_s = 1$ pF and a design frequency $f_s = 2$ GHz the optimum input impedance from table 3.1, is $14.61 + \text{j}16.84\Omega$.

The input impedance of the above load network is given by

$$Z_{\text{in}} = R + jQ \frac{n\omega_s^2 - \omega_0^2}{\pi n\omega_s \omega_0}.$$  \hspace{1cm} (4.1)

Where $\omega_0$ is the resonant frequency of the load harmonic network and $\omega_s$ is the design frequency ($f_s = 2$ GHz).

The GA is used to investigate how the $Q$ factor of the series resonant circuit affects efficiency and the bandwidth of the efficiency. This is achieved by determining the lowest value of the $Q$ factor so that maximum efficiency is still obtained by restricting the maximum amplitudes of the currents of the second and third harmonics relative to the amplitude of the current flowing in the load circuit at the fundamental frequency.

The objective function used in GA in the optimisation is given below.

$$\text{Objective Function} = \eta = \frac{P_{dc} - P_2 - P_3}{P_{dc}}.$$  \hspace{1cm} (4.2)

The input dc power to the amplifier is

$$P_{dc} = V_{dc}I_{dc}.$$  \hspace{1cm} (4.3)
The power loss in the resistance of the series resonant circuit at the second and third harmonics is given below.

\[ P_2 = \frac{1}{2} i_2^2 (2f_s) R. \]  
\[ P_3 = \frac{1}{2} i_3^2 (3f_s) R. \]  

(4.4a)  
(4.4b)

The currents flowing in the load resistance at the second and third harmonics are shown below.

\[ i_2 \ 2f_s = \frac{\frac{V(2f_s)}{z_{tn}(2f_s)}}{2l_{de}} \] ;  
\[ i_3 \ 3f_s = \frac{\frac{V(3f_s)}{z_{tn}(3f_s)}}{2l_{de}}. \]  

(4.5a)  
(4.5b)

From the Fourier analysis carried out of the voltage waveform (see (3.6)) the coefficients of the second and third harmonics are given below.[20].

\[ V \ 2f_s = \frac{2l_{de}}{\pi \omega \ C_s} \frac{4 + i \pi}{12} \]  
\[ V \ 3f_s = \frac{2l_{de}}{\pi \omega \ C_s} \frac{1}{9}. \]  

(4.6)

The conditions to minimize the current flowing through the load network, which will for the second and third current harmonics, are given below.

\[ 20 \log \frac{i_l(f_s)}{i_2(2f_s)} \approx 20 ; \]  
\[ 20 \log \frac{i_1 \ f_s}{i_3 \ 3f_s} \approx 20. \]  

(4.7a)  
(4.7b)
Details of the implementation of the GA software are shown in appendix C.1. From the results obtained Fig. 4.2 shows how the efficiency depends on the $Q$ factor and the resonant frequency.

From the Fig. 4.2 (a) it can be seen that the efficiency of the ideal class E amplifier is nearly 100% for $Q \geq 3$ and is nearly independent of resonate frequency from 1.7 to 1.95 GHz.
The ideal harmonic switch voltage and load harmonic current \((R_{on} = 0)\) were also achieved below.

<table>
<thead>
<tr>
<th>(Q)</th>
<th>(f_0) (GHz)</th>
<th>(I_R) (2 GHz)</th>
<th>(I_R) (4 GHz)</th>
<th>(I_R) (6 GHz)</th>
<th>(P_{out}) (W)</th>
<th>(P_{diss}) (W)</th>
<th>(\eta) (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>1.505</td>
<td>0.367</td>
<td>0.062</td>
<td>0.010</td>
<td>1.016</td>
<td>0.029</td>
<td>97.07</td>
</tr>
<tr>
<td>5</td>
<td>1.783</td>
<td>0.368</td>
<td>0.032</td>
<td>0.005</td>
<td>0.995</td>
<td>0.008</td>
<td>99.22</td>
</tr>
<tr>
<td>10</td>
<td>1.888</td>
<td>0.367</td>
<td>0.018</td>
<td>0.003</td>
<td>0.989</td>
<td>0.002</td>
<td>99.77</td>
</tr>
<tr>
<td>20</td>
<td>1.943</td>
<td>0.367</td>
<td>0.009</td>
<td>0.001</td>
<td>0.988</td>
<td>0.001</td>
<td>99.94</td>
</tr>
</tbody>
</table>

Table 4.1: Load harmonic current and harmonic switch voltage Vs variable \(Q\) factor
\((a = 1.862, \varphi = -32.482^o\)and \(P_{dc} = 0.987\) W\)

The Harmonic-Balance Analysis (HB) option in the ‘ADS’ software was used to model the designed circuit. HB modelling can be used for strongly or weakly nonlinear networks having single or multi tone excitation. The nonlinear sub-circuit is analysed in the time domain while the linear circuit is analysed in the frequency domain. In this design the nonlinear element is the switch and the linear network is the series resonant circuit.

The solution is obtained by an iterative process by ensuring continuity of current flow between the two sub-circuits for all the frequency components.

The simulation schematic of the circuit by using Agilent ADS software is shown in Fig. 4.3 where the period for the nonlinear network was specified as 0.5 nsec (as \(T_s = 1/f_0\)) while for the linear network the design frequency \((f_s)\) was specified as 2 GHz. In the schematic circuit below \(R_{on}\) is equal to zero so that only the effect on efficiency by the loss caused the harmonic currents in resistance \(R_{opt}\), is investigated.
The obtained simulated results shown in Table 4.2 confirm the above theoretical prediction that the $Q$ factor and hence the losses due to the harmonic currents in the load resistance have very little effect on the efficiency of power conversion. The main effect of $Q$ factor is on the bandwidth of efficiency and hence a circuit with a low $Q$ factor can be used to obtain a wide efficiency bandwidth.

<table>
<thead>
<tr>
<th>$Q$</th>
<th>$f_0$ (GHz)</th>
<th>$\eta$ (%)</th>
<th>Bandwidth (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>1.46</td>
<td>99.08</td>
<td>47</td>
</tr>
<tr>
<td>5</td>
<td>1.74</td>
<td>99.89</td>
<td>26</td>
</tr>
<tr>
<td>10</td>
<td>1.75</td>
<td>99.48</td>
<td>15</td>
</tr>
<tr>
<td>20</td>
<td>1.885</td>
<td>99.42</td>
<td>7</td>
</tr>
</tbody>
</table>

Table 4.2: Effect of $Q$ on efficiency and efficiency bandwidth from ADS simulation
4.3 Effect of $R_{on}$ on the Efficiency of Power Conversion

4.3.1 For the Condition when the Voltage Waveform at Half Period is Zero

Using (3.15) and (3.16) it can be shown that (see appendix D) the input dc power and ac output powers are given by,

$$P_{dc} = V_{dc}I_{dc} = \frac{V_{dc}^2}{\frac{1}{\pi\omega_sC_s} + \frac{3}{2R_{on}} + \frac{\omega_sC_sR_{on}}{\pi}}; \quad (4.8)$$

$$P_{out} = I_{dc}\frac{\omega_sR_{opt}}{2} = 1 + \frac{\pi}{2} + \frac{\omega_sC_sR_{on}}{2} \frac{R_{opt}}{I_{dc}}. \quad (4.9)$$

The power dissipated in the active device can now be obtained by evaluating (3.24).

$$P_{diss} = \frac{1}{\tau_s} \int_0^{\tau_s} V_s t I_s t \, dt. \quad (4.10)$$

The efficiency of power conversion is given by (4.11),

$$\eta = \frac{P_{out}}{P_{in}}. \quad (4.11)$$

The effect of $R_{on}$ (1 to 5 $\Omega$) based on the above derived equations and those obtained from ADS simulation on the input, output and dissipated power and efficiency is shown in table 4.3.
The above table shows that there is a good agreement between the predicted and simulated results. As can be see the power dissipated in the turn on resistance $R_{on}$ has a major effect on the efficiency of power conversion. The conversion loss decreases from 100% when $R_{on}$ is zero to 63% when $R_{on} = 5$ Ω. Consequently to obtain maximum efficiency an active device with the smallest $R_{on}$ resistance should be used. The result of sweeping the design frequency ($f_s$), is shown in Fig. 4.4.
Due to the important effect of the $R_{on}$, it is necessary to further investigate another new methodology to improve the performance of the class E PA, when the active device FET has been selected. From above figure, it can be seen that after changing operating frequency of the PA, its efficiency will be increased. When the design frequency ($f_s$) was swept to 2.2 GHz, the maximum efficiency could be achieved to 79% (see Fig. 4.4), but the perfected waveforms were not valid, which are given in Fig. 4.6. The above figure implies that the smooth current and voltage waveforms can be obtained at 2 GHz (see Fig. 4.5), but not the maximum efficiency.

![Efficiency of the amplifier vs. design frequency using ADS ($Q = 10$)](image)

Figure 4.4: Efficiency of the amplifier vs. design frequency using ADS ($Q = 10$)

![Waveforms of the class E PA ($R_{on} = 5 \Omega$) at 2 GHz](image)

(a) Voltage (in V) and current (in A) waveforms of the class E PA ($R_{on} = 5 \Omega$) at 2 GHz

(b) Efficiency (%) vs. Frequency (GHz)
From the above discussion, it implies that the conventional methodology of class E amplifier is not critical especially when the $R_{on}$ not equal to zero. Hence, a better method is to use the quadratic equation (3.28) to obtain better efficiencies, which have been fully explained in Chapter 3, so only the predicted and the simulation results are given in section 4.3.2 and the current and voltage waveforms can be seen in Fig. 3.8 and in section 4.3.3 the Genetic Algorithms (GA) will be used to achieve the required maximum efficiency.
4.3.2 Effect on the Efficiency for the Condition when the Voltage Waveform at Half Period Are equal but not Zero

Using Table 3.2, the optimum efficiency of the class E amplifier could be obtained below,

<table>
<thead>
<tr>
<th>$R_{on}$ (Ω)</th>
<th>$P_{dc}$ (W)</th>
<th>$P_{out}$ (W)</th>
<th>$P_{diss}$ (W)</th>
<th>$\eta$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Predicted</td>
<td>ADS</td>
<td>Predicted</td>
<td>ADS</td>
</tr>
<tr>
<td>0</td>
<td>0.541</td>
<td>0.587</td>
<td>0.541</td>
<td>0.586</td>
</tr>
<tr>
<td>1</td>
<td>0.536</td>
<td>0.582</td>
<td>0.502</td>
<td>0.544</td>
</tr>
<tr>
<td>2</td>
<td>0.516</td>
<td>0.561</td>
<td>0.453</td>
<td>0.492</td>
</tr>
<tr>
<td>3</td>
<td>0.442</td>
<td>0.460</td>
<td>0.372</td>
<td>0.392</td>
</tr>
<tr>
<td>4</td>
<td>0.477</td>
<td>0.526</td>
<td>0.366</td>
<td>0.404</td>
</tr>
<tr>
<td>5</td>
<td>0.406</td>
<td>0.412</td>
<td>0.309</td>
<td>0.323</td>
</tr>
</tbody>
</table>

Table 4.4: Effect of $R_{on}$ on the predicted and simulated results ($Q = 5$)

4.3.3 Application of Genetic Algorithm to Obtain Maximum Efficiency

The maximum efficiency could be obtained by using GA, the objective function is $\eta_{max} = \frac{P_{out}}{P_{dc}} (\alpha_r, \phi_r)$. Show in the appendix derivation of the equations below,

Using (3.22), the dc current can be obtained as

$$I_{dc} = \frac{V_{dc}}{\frac{\pi}{4\omega SC_s} \frac{\alpha_r \sin \phi_r}{\pi \omega SC_s} + \frac{\alpha_r \cos \phi_r + 3R_{on} + \frac{R_{on}}{I_{dc}} \frac{\alpha_r \cos \phi_r}{\pi}}{2} + \frac{2}{\pi \omega SC_s}}$$  \hspace{1cm} (4.12)
\[ P_{dc} = \frac{V_{dc}^2}{\frac{\pi}{4\omega_L C_L} a_r \sin \phi_r + \frac{a_r \cos \phi_r}{\pi \omega_L C_L} \left( \frac{3R_{on} l_{dc}}{2} + R_{on} l_{dc} c \right) \frac{a_r \cos \phi_r}{\pi}} \] (4.13)

Using the input impedance of the external load harmonic network in (3.28) as given

\[ Z_{in opt} = \frac{v_2(\omega s)}{i_R(\omega s)} = \frac{2 \pi x_1}{a_r l_{dc}} e^{j(\frac{\pi}{2} + \theta_2 - \phi_r)} = R_{opt} + jX_{opt} \] (4.14)

The ac output powers are given by,

\[ P_{out} = I_{dc} \frac{a_r^2}{2} R_{opt}. \] (4.15)

The maximum power conversion efficiency \( \eta_{max} \) is given in (4.16) as a function of \( a_r \) and \( \phi_r \).

\[ \eta_{max} = \frac{P_{out}}{P_{dc}} (a_r, \phi_r) \] (4.16)

The three dimensions graph \( (a_r, \phi_r) \), maximum power conversion efficiency \( \eta_{max}(a_r, \phi_r) \) of (4.16) has been plotted as shown below.

Figure 4.7: Optimum solutions \( \eta_{max} \) of (4.16) using variable \( a_r \) and \( \phi_r \)
By applying the GA programmes, the novel optimum input impedance has been obtained for variable turn on impedance \( R_{on} \), which were shown below in Table 4.5 below,

<table>
<thead>
<tr>
<th>( R_{on} ) (Ω)</th>
<th>( a_r )</th>
<th>( \varphi_A(°) )</th>
<th>Re(( Z_{opt} )) (Ω)</th>
<th>Im(( Z_{opt} )) (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2.508</td>
<td>-57.260</td>
<td>19.338</td>
<td>32.509</td>
</tr>
<tr>
<td>1</td>
<td>2.521</td>
<td>-57.203</td>
<td>18.922</td>
<td>32.823</td>
</tr>
<tr>
<td>2</td>
<td>2.577</td>
<td>-55.206</td>
<td>16.867</td>
<td>31.049</td>
</tr>
<tr>
<td>3</td>
<td>2.561</td>
<td>-58.186</td>
<td>18.464</td>
<td>34.449</td>
</tr>
<tr>
<td>4</td>
<td>2.683</td>
<td>-59.165</td>
<td>17.235</td>
<td>35.162</td>
</tr>
<tr>
<td>5</td>
<td>2.647</td>
<td>-58.301</td>
<td>17.015</td>
<td>34.966</td>
</tr>
</tbody>
</table>

Table 4.5: Effect of \( R_{on} \) on the predicted and simulated results \( Q = 5 \)

The voltage and current waveforms obtained from the Table 4.5 are shown in Fig. 4.8 when \( R_{on} = 0.01 \) Ω which is the smallest value allowed in the software and in Fig 4.9 when \( R_{on} = 5 \) Ω.

![Figure 4.8: Voltage and current waveforms of the class E PA \( R_{on} = 0.01 \) Ω](image)

(a) (b)
After further investigation, the spikes in the current waveforms shown in Figs 4.8 and 4.9 are operating over 50 GHz. Depending on the size of the transistor and low pass filters are commonly used in Morden communalisation systems, these high frequency spikes will be easily absorbed and it hardly affects the efficiency of the class E PAs.
The optimum solutions of (4.16) will be obtained by using the Genetic Algorithms (GA) (see appendix C.2). Final optimum solutions of the \( a_r \) and \( \varphi_r \) are achieved below,

<table>
<thead>
<tr>
<th>( R_{on} (\Omega) )</th>
<th>( P_{dc} ) (W)</th>
<th>( P_{out} ) (W)</th>
<th>( P_{diss} ) (W)</th>
<th>( \eta ) (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 0 )</td>
<td>Predicted</td>
<td>ADS</td>
<td>Predicted</td>
<td>ADS</td>
</tr>
<tr>
<td></td>
<td>0.403</td>
<td>0.415</td>
<td>0.396</td>
<td>0.412</td>
</tr>
<tr>
<td>( 1 )</td>
<td>0.389</td>
<td>0.398</td>
<td>0.363</td>
<td>0.378</td>
</tr>
<tr>
<td>( 2 )</td>
<td>0.399</td>
<td>0.415</td>
<td>0.357</td>
<td>0.376</td>
</tr>
<tr>
<td>( 3 )</td>
<td>0.350</td>
<td>0.352</td>
<td>0.296</td>
<td>0.307</td>
</tr>
<tr>
<td>( 4 )</td>
<td>0.327</td>
<td>0.329</td>
<td>0.265</td>
<td>0.277</td>
</tr>
<tr>
<td>( 5 )</td>
<td>0.324</td>
<td>0.327</td>
<td>0.251</td>
<td>0.263</td>
</tr>
</tbody>
</table>

Table 4.6: Effect of \( R_{on} \) on the predicted and simulated results \((Q = 5)\)

To expand values of the \( R_{on} \), the application of these novel methodologies will be investigated next.

Figure 4.10: Optimum load impedance, \( R_{opt} \) vs. variable turn on resistance, \( R_{on} \)
From Figs 4.10 and 4.11, it could be seen that when the $R_{on}$ is less than 5 Ω, the optimum load impedance, $R_{opt}$, is nearly constant and excellent agreement between the predicted (using GAs) and simulation results (using ADS) is achieved. Due to the losses in power transistors, the $R_{on}$ is normally selected less than 5 Ω; when the $R_{on}$ was bigger than 5 Ω, the novel equations achieved would not be valid. These figures are only used for future investigation.

4.4 Effect of Losses of Different Load Harmonic Networks on the Efficiency

4.4.1 Modelling with Ideal R_L_C Parallel Circuits

To deal with ideal load harmonic networks of an ideal class E amplifier, R_L_C parallel circuits were used to achieve the required input impedance at 2 GHz, which is equal to
$17.015 + j\ 34.966$ ohms (see table 4.5). Hence, a new harmonic load network was designed and simulated using Agilent ADS in Fig. 4.12 below.

After applying the required complex impedances of the harmonic circuit, the anticipated results have been carried out and the current and voltage waveforms have been plotted in Fig.4.13. Furthermore, the respective load current and voltage spectrums have given in Fig.4.14.
From Figs. 4.13 and 4.14, it can be seen that even the distorted input switch voltage and current waveforms have been applied, the smooth output voltage and current waveforms still be obtained.
From the ADS simulation, the excellent results could be obtained, which is about when the $R_{on}$ is equal to 5 ohms, 78.13% of the power efficiency could be achieved, which matches the predicted results in table 4.5.

The above discussion also implies that a yield optimum input impedance of the load networks will be confirmed to be used in the next step of the circuits’ design, in which the transmission line will be involved in the research.

### 4.4.2 Modelling with Ideal Transmission Lines

The transmission line takes a significant part in high frequency microwave RF circuits design. The ideal lumped elements which have been used in the last chapters will be transformed to transmission lines using ideal transmission line theory. The design frequency of the amplifier is 2 GHz. The simulation circuits can be seen in Fig. 4.15.
From Figs.4.16 and 4.17, it can be seen that even the distorted input switch voltage and current waveforms pass through lossy Mlines load harmonic networks, have been applied, the ideal voltage and current waveforms still be obtained and the efficiency of the class E amplifier is equal to 99.9\%, When $R_{on} = 0$. 

Figure 4.16: Voltage and current waveforms of the class E amplifier ($R_{on} = 0.01 \, \Omega$)

Figure 4.17: Spectrum frequencies of the load current (in A) (a) and voltage (in V) (b) ($R_{on} = 0.01$)
4.5 Summary

In this chapter it has been shown that as the $R_{on}$ resistance of the active device increased the peak of the current waveform reduced and the overlap of the current and voltage waveforms increased. Both effects contributed to the decrease in the efficiency of power conversion.

GA and new quadratic equations were then used to produce a design graph for a series resonant circuit to show the relationship between the ‘$Q$’ factor, resonant frequency and the efficiency of power conversion. By modelling the amplifier, it was shown that the efficiency is largely dependent on $R_{on}$ and independent of losses due to harmonic balance. Consequently the efficiency is largely dependent on the $R_{on}$ while the efficiency bandwidth depends on the $Q$ factor. To obtain high efficiency and high efficiency bandwidth an active device should have a low turn on resistance and the series resonant circuit should have a low $Q$ factor ($Q \geq 2$, see table 4.2).

In next chapter, the complex mathematical analyses in this chapter will be reduced, which have been studied and investigated in this chapter. A novel method is proposed to determine this resistance as a function of the length of the Mline, which is realised using both inexpensive PCB FR4 and Duroid 5870 substrates.
Chapter 5 Effect of the Losses in the Load Harmonic Networks on Amplifier Efficiency

5.1 Introduction

To obtain a high efficiency of dc to ac power conversion in an amplifier, it is necessary to decrease the power dissipation in the active device by ensuring that the overlap of the voltage and current waveforms at the output terminals of the active device is minimized. This reduction of overlap is obtained by using load harmonic networks to shape the above waveforms at the active device output terminals. In the three common classes of high efficiency power amplifiers (PAs) (E, F and F-1), this shaping is obtained by attenuating different harmonics of the waveforms using load harmonic networks [36, 82, 86-88]. For the class E amplifier [1, 36] a capacitance is placed across at the output terminals of the active device. This is to ensure that the output voltage is delayed until the active device is turned ‘off’ and the output voltage reaches its minimum value with a slow turn ‘on’. If this device is driven hard ‘on’ and ‘off’ to obtain high efficiency as shown in [17, 85] that the input impedance must be very high at the harmonic frequencies. At the design frequency the required input impedance depends on the value of the above capacitance [28].
Ideal lossless transmission lines (Tlines) are used in the initial design of harmonic networks for high efficiency power amplifiers and then practically realised using microstrip lines (Mlines). As the metal and substrate losses in Mlines are normally expressed in terms of attenuation constants, these losses are difficult to determine as they require solutions of complex mathematical equations. In this chapter, to reduce such complex analysis, the losses in a Mline are modelled as a Tline in series with a resistance. A novel method is proposed to determine this resistance as a function of the length of the Mline, which is realised using both inexpensive PCB FR4 and Duroid 5870 substrates. Then for the above two line models, harmonic networks were designed up to the second and third harmonics and the losses obtained losses at the design frequency are compared. Finally, the effect of the losses with different harmonic networks on the class E PA was investigated.

5.2 Review of S Parameters of Two Port Networks Using Unequal Source and Load Impedance

Fig 5.1 shows for a two port network the incident, reflected voltages/currents at the source and the load ports. It also shows the total voltages and currents ($V_1, I_1, V_2, I_2$) at the two ports.

![Figure 5.1: Block diagram of two ports networks](image-url)
S parameters used in the design of filters, couplers and power splitters normally assume that $R_{01} = R_{02} = 50 \, \Omega$. However in the design of harmonic networks used for amplifiers $R_{01} \neq R_{02}$ so that maximum efficiency of power conversion can be obtained. In this section therefore, derivation of the S parameters for $R_{01} \neq R_{02}$ is reviewed and then they are used to investigate the power loss in different load harmonic networks.

In Fig. 5.1 if $E_2$ is made equal to zero it is shown in the appendix that the normalised reflected signal, $a_2$, at the load port is given by

\[ a_2 = \frac{V_2 + I_2 R_{02}}{2 R_{02}} \]  

(5.1)

As $V_2 = -I_2 R_{02}$ then $a_2 = 0$ as required.

The incident signal ‘$b_2$’ at the load port is

\[ b_2 = \frac{V_2 - I_2 R_{02}}{2 R_{02}} \]  

(5.2)

Similarly by making $E_1$ equal to zero the reflected signal at the source port ‘$a_1$’ is given by

\[ a_1 = \frac{V_1 + I_1 R_{01}}{2 R_{02}} = 0 \]  

(5.3)

The incident signal $b_1$ at the source port is
Using the above equations the following parameters $S_{11}$ and $S_{22}$ can be obtained.

\begin{equation}
S_{11} \ a_2 = 0 = \frac{Z_{in_1} - R_{01}}{Z_{in_1} + R_{01}}
\end{equation}

\begin{equation}
S_{22} \ a_1 = 0 = \frac{Z_{in_2} - R_{02}}{Z_{in_2} + R_{02}}
\end{equation}

$Z_{in1}$ and $Z_{in2}$ are the input impedances of the two port network looking from port 1 and port 2.

Similarly the other two $S$ parameters shown in the equations below can be obtained.

\begin{equation}
S_{21} \ a_2 = 0 = \frac{-2I_2}{E_1} \frac{R_{01}R_{02}}{R_{02}}
\end{equation}

\begin{equation}
S_{12} \ a_1 = 0 = \frac{-2I_1}{E_2} \frac{R_{01}R_{02}}{R_{01}}
\end{equation}

It is convenient to use signal flow graphs to analyse microwave networks consisting of transmission lines. For a simple two port network a signal flow graph is shown in Fig. 5.1 where the node $(a_1, b_2, a_2, b_2, b_3)$ are connected by branches defined by the ‘$S$’ parameters.
The transducer power gain $G_T$ defined is defined.

$$G_T = \frac{\text{Power Delivered in the Load } (P_L)}{\text{Available Power from the Source } (P_{AVS})}$$  \hspace{1cm} (5.9)

From the signal flow analysis using Mason ‘non touching rule’ it can be shown that

$$\frac{P_L}{P_{AVS}} = \frac{S_{21}^2}{1-S_{11}\Gamma_s} \cdot \frac{1-\Gamma_s^2}{1-S_{22}\Gamma_L} \cdot \frac{1-(1-\Gamma_L^2)}{-S_{12}S_{21}\Gamma_L\Gamma_s}$$  \hspace{1cm} (5.10)

$\Gamma_s$ is the source reflection coefficient and $\Gamma_L$ is the load reflection coefficient, which are defined by the two equations below.

$$\Gamma_s = \frac{Z_{in1}-R_01}{Z_{in1}+R_01}$$  \hspace{1cm} (5.11)

$$\Gamma_L = \frac{Z_{in2}-R_02}{Z_{in2}+R_02}$$  \hspace{1cm} (5.12)
For a matched two ports network, as $I_s = I_L = 0$, then from equations above, it can be obtained as $\frac{P_L}{P_{AVS}} = S_{21}^2$ and the power loss $P_{loss}$ in the network is $(1 - S_{21}^2)$. Hence, in the next few sections, $S_{21}$ will be used to investigate the losses of the harmonic networks.

5.3 Modelling Losses in Microstrip Transmission Lines and Harmonic Networks

Conductor and dielectric losses in uniform transmission lines have been derived in terms of attenuation constants. However in the investigation of losses in harmonic networks complex equations are required to be solved. To simplify the analysis the microstrip line is modelled as an ideal lossless transmission line (Tline) in series with a resistance ‘$R$’ as shown in Fig.5.3 (a) and for each length of the Mline (see Fig. 5.3(b)), the resistance ‘$R$’ is tuned so that the ‘$S_{21}$’ parameter in both circuits is the same.

To reduce mismatch errors, a Tline in series with a resistance and a Mline connected in series with Tline (see Fig. 5.3(b)) are connected in a shunt configuration. To reduce errors due to the imaginary part of the input impedance of the lines, the electrical length of Tline in Fig.5.3(a) and the total length of the two lines in Fig. 5.3(b) should be halve-wavelength long. As the length of Mline is increased the electrical length of the ideal line connected in series is reduced to maintain that the total length of both lines is equal to the half wavelength throughout the measurement of the resistance. AWR software was used for different lengths of microstrip lines where the resistance ‘$R$’ was tuned till $S_{21}$ was the same for the two models.
By using the above methodologies, the losses of the Mline (R) are linearly dependent on the length of the Mline, which is about 0.0376 Ohms/mm using PCB FR4 (because practical fabrication tolerance occurs mismatch oscillation, the least square fitting method is used to obtain linear response see Fig. 5.4) and 0.0035 Ohms/mm using Duroid 5870 substrates.

The width (W) of the microstrip line was chosen so that the characteristic impedance, $Z_0$, was 50Ω. The investigation was carried out at 2 GHz for two substrates, PCB FR4 where the loss angle of the substrate is 0.019 and RT Duroid 5870 where the loss angle is 0.002. The results obtained are shown in the two figures in next page.
Figure 5.4: Resistances, $R$, as a Function of Length for PCB FR4

Figure 5.5: Resistances, $R$, as a Function of Length for RT Duroid 5870
As can be seen the resistance ‘$R$’ is smaller for the ‘Duroid’ than it is for ‘PCB FR4’ substrate as the former substrate has a much lower dielectric loss tangent. Further the above graphs show that there is a linear relationship between $R$ and the length of the microstrip line. This property will be used in GA in later work to optimise harmonic networks to obtain minimum loss at the design frequency. In the next section these results are used to compare the losses obtained for different topologies of harmonic networks which are realised using the two substrates.

5.4 Design of the Load Harmonic Networks to the Second and Third Harmonic and the Effect of Losses on the Efficiency of Power Conversion

In this section different load harmonic networks are designed to meet the requirement for a class E PA at the second harmonic. Their designs is based on the assumption $R_{on} = 0$, the required $Z_{opt}$ (as shown in chapter 3) is $14.611 + j16.682$ (Ohms) and load impedance is $Z_0 (= 50 \Omega)$. The required input impedance at the second harmonic is ideally infinity. As $R_{on} = 0$ the only losses are in the harmonic network and due to the harmonic currents in $Z_0$.

In the design of networks in order to suppress harmonics, shunt transmission lines are used, which are either a half-wave or a quarter-wave length long. This ensures a short circuit or low impedance at junctions with the series transmission lines. This is to ensure that the required input impedance is obtained independently at each harmonic frequency. For different harmonic networks the losses are obtained from the $S_{21}$ parameter and are compared for the two models of transmission lines as shown in Fig 5.3.
5.4.1 Losses in a Suppressed Second Harmonic Network

In Fig. 5.6(a) the second harmonic of 4 GHz is suppressed by the Mline $M_1$ and $M_2$, which are a half wavelength and a quarter wavelength long, respectively. The short circuit at the line $M_2$ models the effect of placing a dc voltage supply for the amplifier. The lines $M_3$ and $M_4$ are used to obtain matching at two ports at the design frequency. As the input impedance of the network at 2 GHz is 14.6 +j 16.8 Ohms a conjugate value of this impedance is required by the source port to obtain a maximum power transfer. In the AWR software used to model the designed networks, the ports are required to have only real impedances. To cancel the reactance j16.8 a capacitor $C_1$ of 4.67 pF is placed as shown in Fig. 5.6(a). Impedance of Ports 1 and 2 are 14.6 $\Omega$ and 50 $\Omega$, respectively. $M_3$ and $M_4$ are used to obtain matching at the design frequency. Fig. 5.6(b) models each Mline with a Tline in series with the appropriate resistance.

Figure 5.6: Harmonic Networks Using PCB and Duroid 5870 Substrates (a) MLines, (b) Modelled using TLines in Series with Resistance, $R$
The lengths and the values of the resistances for both substrates are summarised in the two tables below.

<table>
<thead>
<tr>
<th></th>
<th>Length of the Microstrip Lines (mm)</th>
<th>Equivalent Resistance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$</td>
<td>9.4</td>
<td>$R_1 = 0.67$</td>
</tr>
<tr>
<td>$M_2$</td>
<td>21.7</td>
<td>$R_2 = 1.54$</td>
</tr>
<tr>
<td>$M_3$</td>
<td>3.8</td>
<td>$R_3 = 0.27$</td>
</tr>
<tr>
<td>$M_4$</td>
<td>12</td>
<td>$R_4 = 0.85$</td>
</tr>
</tbody>
</table>

Table 5.1: Equivalent resistances of variable microstrip lines using PCB FR4 substrate ($Z_0 = 50 \, \Omega$)

<table>
<thead>
<tr>
<th></th>
<th>Length of the Microstrip Lines (mm)</th>
<th>Equivalent Resistance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$</td>
<td>9.4</td>
<td>$R_1 = 0.07$</td>
</tr>
<tr>
<td>$M_2$</td>
<td>21.7</td>
<td>$R_2 = 0.15$</td>
</tr>
<tr>
<td>$M_3$</td>
<td>3.8</td>
<td>$R_3 = 0.03$</td>
</tr>
<tr>
<td>$M_4$</td>
<td>12</td>
<td>$R_4 = 0.08$</td>
</tr>
</tbody>
</table>

Table 5.2: Equivalent resistances of variable microstrip lines using Duroid 5870 substrate ($Z_0 = 50 \, \Omega$)

The frequency response of the S-parameters is shown in Fig. 5.7 using PCB FR4 substrate (using Duroid 5870 substrate can be seen in Appendix D) and from $S_{12}$ determines the loss in both networks.
Figure 5.7: The obtained S-parameters (a) $S_{11}$, (b) $S_{22}$ using FR4 substrate and (c) $S_{21}$ using both substrates.

The switch voltage and current waveforms for the above harmonic networks are shown in Fig. 5.8. As it can be seen that the effect of losses is to considerably reduce the oscillations during the ‘on’ state and the oscillations are reduced to a lesser extent in the ‘off’ state for the current waveforms.
The efficiency obtained for the harmonic network for both substrates and their models are compared in the Table 5.3 below.

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB FR4</td>
<td>92.53</td>
</tr>
<tr>
<td>Duroid 5870</td>
<td>98.01</td>
</tr>
</tbody>
</table>

Table 5.3: Comparison of the efficiency using difference substrate

Due to using the lossy substrate (PCB FR4), the efficiency of the amplifier will reduce to 92%; less effect of the load harmonic voltage/current has less effect, which will only reduce the efficiency of the amplifier by about 2%.

Finally, T junctions were included and the lengths of the microstrip lines were tuned to obtain optimum S parameters. Fig. 5.9 shows the parameters $S_{11}$ and $S_{22}$ and as can be seen matching has been obtained at each port.
Figure 5.9: Obtain optimum S parameters: $S_{11}$ and $S_{22}$

The obtained $S_{12}$ parameter is shown in Fig. 5.10.
For PCB FR4 substrate \( S_{21} = 0.975 \) and the efficiency is 92.5%. For Duroid 5870 substrate \( S_{21} = 0.997 \) and the efficiency is 98%.

The voltage and current waveforms obtained for each substrate using microstrip line are shown in Fig. 5.11 and Fig. 5.12.
The expected voltage waveform was obtained but again the current waveform was distorted showing a big spike and oscillations. From previous discussions in chapter 4, it can be seen that the big spikes will not affect the performance of the PAs.

The efficiency obtained for the harmonic network with junctions is 92.3% for PCB FR4 substrate and 96.2% for the Duroid 5870 substrate. It is interesting to note the adverse effect on the losses of the efficiency.

In this section two different harmonic networks were designed using ideal lossless transmission lines and microstrip lines which were realised using high loss PCB FR4 substrate and a low loss Duroid 5870 substrate. It was found that the expected voltage waveform was obtained but the current was distorted. However this distortion only had a small effect on the efficiency of power conversion which is largely dependent on the losses in the substrate and the effect of junctions.

The obtained power conversion efficiencies are shown in Table 5.4, showing a good agreement for the two models shown in Fig. 5.7 and for the two substrates. The higher loss in
the PCB FR4 substrate as compared with the losses in the Duroid 5870 substrate causes the efficiency to reduce by about 6%.

<table>
<thead>
<tr>
<th></th>
<th>Power Conversion Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLines with R (PCB FR4)</td>
<td>90.52</td>
</tr>
<tr>
<td>TLines with R (Duroid 5870)</td>
<td>97.51</td>
</tr>
<tr>
<td>MLines (PCB FR4)</td>
<td>90.76</td>
</tr>
<tr>
<td>MLines (Duroid 5870)</td>
<td>95.63</td>
</tr>
</tbody>
</table>

Table 5.4: Power conversion efficiencies for the Two Models of the Harmonic Networks for PCB FR4 and Duroid 5870 Substrates

5.4.2 Losses in a Suppressed Second and Third Harmonics Network

Four topologies of a harmonic network up to third harmonic are shown in Fig. 5.13 where in each case the short circuit shows the position where a dc voltage for the amplifier would be connected.
In Fig. 5.13(a) the $T_2$ is made half-wavelength at the second harmonic while $T_4$ is made quarter-wavelength to ensure short circuit conditions at the junctions of $T_1/T_3$ and $T_3/T_4$. $T_1$ is made quarter wavelength at the second harmonic to ensure that the input impedance is infinity at this frequency. To obtain the required input impedance at the third harmonic the length of $T_3$ is obtained. A similar process is applied to the network in Fig. 5.13(b) except
now the length of $T_3$ is obtained to obtain the required impedance at the second harmonic. A similar design is applied for the two networks shown in Fig. 5.13(c) and Fig. 5.13(d). In Figs. 5.13(a) to 5.13(d) the lines $T_5$ and $T_6$ are used to obtain matching at the source and load ports.

The real and imaginary parts of the input impedance of the above four networks is shown in Figs. 5.14 and 5.15 where it can be seen that the required impedances at the design frequency and at the two harmonics have been obtained.
Figure 5.14: Real part of Input Impedance of the Four Networks operating at 2, 4 and 6 GHz
Figure 5.15: Imaginary part of Input Impedance of the Four Networks operating at 2, 4 and 6 GHz.

The frequency response of the ‘S’ parameters at the design frequency are shown in Fig. 5.16.
Figure 5.16: Obtain optimum S parameters: $S_{11}$ and $S_{22}$

From $S_{21}$ there is no loss in the network as expected below

Figure 5.17: Obtain optimum S parameters: $S_{21}$
The switch voltage/current waveforms obtained are shown in Fig. 5.17.

(a)

(b)

(c)
The switch voltage (in V) (A) / current (in A) (B) waveforms

Figure 5.18: The switch voltage (in V) (A) / current (in A) (B) waveforms

The efficiency obtained for four kinds of load harmonic networks are compared in the Table 5.5 below.

<table>
<thead>
<tr>
<th>Four kinds of load harmonic networks</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>99.44</td>
</tr>
<tr>
<td>(b)</td>
<td>99.90</td>
</tr>
<tr>
<td>(c)</td>
<td>99.72</td>
</tr>
<tr>
<td>(d)</td>
<td>99.78</td>
</tr>
</tbody>
</table>

Table 5.5: Comparison of the efficiency using difference substrate
From the switch voltage/current in Fig. 5.17 and the efficiency from Table 5.5, it can be determined that the best performing load harmonic network is (b) and it will be used to design the circuitry.

The above lossless transmission lines were replaced by microstrip lines and by lossless transmission lines in series with the appropriate resistance.

Figure 5.19: Two port networks: (a) Microstrip Line Model, and (b) Equivalent Transmission Line with $R$ Model for PCB FR4 and Duroid 5870 Substrates

The lengths and the values of the resistances for both PCB FR4 (and more details of using Duroid 5870 substrates can be see in Appendix D) are summarised in the two tables below,
### (a)

<table>
<thead>
<tr>
<th>Length of the Microstrip Lines (mm)</th>
<th>Equivalent Resistance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1 10.2</td>
<td>R₁ = 0.73</td>
</tr>
<tr>
<td>M2 20.5</td>
<td>R₂ = 1.46</td>
</tr>
<tr>
<td>M3 10</td>
<td>R₃ = 0.71</td>
</tr>
<tr>
<td>M4 6.8</td>
<td>R₄ = 0.48</td>
</tr>
<tr>
<td>M5 24.4</td>
<td>R₅ = 1.73</td>
</tr>
<tr>
<td>M6 12.2</td>
<td>R₆ = 0.87</td>
</tr>
</tbody>
</table>

(Total length = 44.7 mm)

### (b)

<table>
<thead>
<tr>
<th>Length of the Microstrip Lines (mm)</th>
<th>Equivalent Resistance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1 6.8</td>
<td>R₁ = 0.48</td>
</tr>
<tr>
<td>M2 13.5</td>
<td>R₂ = 0.96</td>
</tr>
<tr>
<td>M3 2.8</td>
<td>R₃ = 0.20</td>
</tr>
<tr>
<td>M4 10.2</td>
<td>R₄ = 0.73</td>
</tr>
<tr>
<td>M5 3.6</td>
<td>R₅ = 0.26</td>
</tr>
<tr>
<td>M6 7.8</td>
<td>R₆ = 0.55</td>
</tr>
</tbody>
</table>

(Total length = 44.7 mm)
Table 5.6: Equivalent resistances of variable microstrip lines using PCB FR4 substrate ($Z_0 = 50 \, \Omega$) (Total length = 52.9 mm).
The frequency response of the input impedance for the two models using PCB FR4 substrate (using Duroid 5870 substrate are given in Appendix D) is shown in Fig. 5.19.

Figure 5.20: Input Impedance (in Ω) of the load harmonic networks using (a) PCB FR4 substrate and (b) Equivalent circuits with R.
The frequency response of the ‘S’ parameters using load harmonic (b) using PCB FR4 substrate (results using Duroid 5870 could be found in Appendix D) in Fig. 5.18 is shown in Fig. 5.20.
Design of each of the above networks is very similar to that of the previous section and the frequency response of $S_{21}$ for the four circuits and the two substrates shows that a very good agreement is obtained in Fig. 5.21 using PCB FR4 and Fig. 5.22 using Duroid 5870.
Figure 5.22: The frequency response of $S_{21}$ using PCB FR4 for the four topologies circuits using (a) Tlines with $R$ and (b) Mlines
The obtained power conversion efficiencies are compared in Table 5.7.

<table>
<thead>
<tr>
<th></th>
<th>Power Conversion Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load harmonic networks</td>
<td>(a)</td>
</tr>
<tr>
<td></td>
<td>(b)</td>
</tr>
<tr>
<td></td>
<td>(c)</td>
</tr>
<tr>
<td></td>
<td>(d)</td>
</tr>
<tr>
<td>Tlines with R using PCB FR4</td>
<td>86.27</td>
</tr>
<tr>
<td></td>
<td>95.96</td>
</tr>
<tr>
<td></td>
<td>87.60</td>
</tr>
<tr>
<td></td>
<td>93.35</td>
</tr>
<tr>
<td>MLines using PCB FR4</td>
<td>82.91</td>
</tr>
<tr>
<td></td>
<td>93.65</td>
</tr>
<tr>
<td></td>
<td>84.28</td>
</tr>
<tr>
<td></td>
<td>92.42</td>
</tr>
<tr>
<td>MLines using Duroid 5870</td>
<td>96.85</td>
</tr>
<tr>
<td></td>
<td>96.21</td>
</tr>
<tr>
<td></td>
<td>98.69</td>
</tr>
<tr>
<td></td>
<td>99.24</td>
</tr>
<tr>
<td>Total Lengths of Mlines using</td>
<td>84.1</td>
</tr>
<tr>
<td>PCB FR4 substrate (mm)</td>
<td>43.2</td>
</tr>
<tr>
<td></td>
<td>93.7</td>
</tr>
<tr>
<td></td>
<td>50.9</td>
</tr>
<tr>
<td>Total Lengths of Mlines using</td>
<td>108.4</td>
</tr>
<tr>
<td>Duroid 5870 substrate (mm)</td>
<td>56.1</td>
</tr>
<tr>
<td></td>
<td>120.7</td>
</tr>
<tr>
<td></td>
<td>65.6</td>
</tr>
</tbody>
</table>

Table 5.7: Efficiency of Power Conversion for Mlines and Equivalent Tlines with Resistance R, and, Total Lengths of Mlines

From Table 5.7 there is a good agreement for efficiency obtained by the two models of transmission lines. From Tables 5.4 and 5.7, it can be seen that the efficiency is only slightly lower with the suppression of only the second harmonic networks shown in Fig. 5.10 than the suppression of the second and third harmonics shown in Fig. 5.22.

Table 5.8 also shows that the power conversion efficiency increases as the total lengths of the microstrip lines decreases, especially for lossy PCB FR4 substrate.
5.5 Summary

In this chapter the losses in Mlines are modelled as resistance in series with a Tline and a novel method has been used to determine how the resistance depends on the length of a Mline realised using PCB FR4 and Duroid 5870 substrate. The losses were compared the second suppressed harmonic networks with the second and third suppressed harmonics networks using the $S_{21}$ parameter. A good agreement was obtained for the two models. A harmonic network was designed for optimum input impedance at the design frequency and at second harmonic. The obtained losses for the two models were in good agreement and the efficiency of power conversion for both networks was nearly 91%.

Four different topologies were designed up to the third harmonic and it was shown again that there was a good agreement in the frequency response of the $S_{21}$ parameter for the two models. Then using the networks the effect of losses on the power conversion efficiency was investigated. A good agreement was obtained for the two models and it was also shown that as the total length of the Mlines increased the efficiency of power conversion decreased. The efficiencies for the suppressed second harmonic networks were nearly the same as those for the harmonic networks designed up to the third harmonic. From this result it can be assumed that it is sufficient to design harmonic networks only up to the second and third harmonic, especially using the lossy PCB FR4 substrate to design a class E amplifier using a nonlinear active device_ATF34143 transistor in next chapter.
Chapter 6 Design of High Efficiency Stabilized Class E Amplifiers Using a Nonlinear Active Device

6.1 Introduction

As investigated in the last few chapters, the large input signal is applied to drive the active devices hard ‘on’ and ‘off’ in order to obtain the high dc to ac power conversion. To reduce the power losses in the active device, a shunt capacitance \( C_s \) across the FET is required to minimise the overlap between the switch voltage and current waveforms. Consequently, it is necessary to investigate the nonlinear model of the given active device.

In this chapter, the active device models will be reviewed in section 6.2. In section 6.3 the most popular and efficient method to measure the input and output impedance of the nonlinear active devices (device-under-test (DUT)) has been introduced using passive or active load/source-pull measurement methods has be introduced and the stability analysis equations for class E PAs are studied in section 6.4. The selected MESFET ATF34143 has been described in section 6.5. A novel procedure of design of a high efficiency class E amplifier will be introduced, which is using the data sheet of the given active device (ATF34143) to obtain the turn-on resistance \( R_{on} \) and then the shunt capacitance \( C_s \) will be
determined by using the obtained $R_{on}$ in section 6.6 and 6.7. In section 6.8, design of matching networks using lumped elements for the class E amplifier will be introduced and design of matching networks using microstrip lines and the simulation results will be given in section 6.9 and 6.10. Finally, the implementation and practical measurement will be shown in section 6.11.

### 6.2 Literature Review of Active Device Models

It is well known that accurate device modelling is extremely important to develop monolithic integrated circuits [16, 89], consequently, it is necessary to review the relevant active device models first and it can give better approximations of the final design of the class E amplifiers if the performance of the nonlinear active model is described accurately.

To produce a commercial compact size of integrated circuits, the Field Effect Transistor (FET) is used. The most commonly used FETs are the MOSFET (Metal-oxide-semiconductor field-effect transistor) and MESFET (Metal semiconductor field effect transistor), which are used for amplifying or switching electronic signals. The nonlinear MOSFET and MESFET models with extrinsic elements are given in Fig. 6.1.
The nonlinear models of MOSFET and MESFET in Fig.6.1 are very similar. In the intrinsic models, the channel charging resistance $R_{ags}$ is the resistive path for the charging of the gate-source capacitance $C_{gs}$, the feedback gate-drain capacitance $C_{gd}$, the drain-source capacitance $C_{ds}$, the gate-source diode to model the forward conduction current $i_{gs}(v_{gs})$, and the gate-drain diode to account for the gate-drain avalanche current $i_{gd}(v_{gs}, v_{ds})$, which can occur and can be used for large signal operation conditions.

Because numerous MESFET fabrication possibilities have been explored of semiconductor systems, its main application areas are front end low noise amplifiers of microwave transmitters, power amplifiers for output stages of microwave links, satellite communication, and commercial optoelectronics and so on and so forth.

In this thesis the ATF34143 MESFET has been selected and its data sheet will be reviewed in the next section.
6.3 Review of the Nonlinear Analytical Methods for Class E Amplifiers

The most popular and efficient method to measure the input and output impedance of the DUT is to use passive or active load/source-pull measurement methods. The objective of the active load/source-pull measurement method is to find the best output/input impedance of the required optimum values of the load impedance $Z_L(nf_0)$/source impedance $Z_s(nf_0)$ in terms of the obtained optimized power gain and power-added efficiency (see Fig. 6.2), where $n = 1, 2, 3...$ When the transistor is operating in the nonlinear region, the measurements are required to produce large-signal operation as input and output impedance at required bias condition and certain frequency ranges.

![Figure 6.2: Topology of source/load-pull measurement systems](Image)

Fig. 6.2 shows at the input/output of the DUT, the measurements of the large-signal impedance are achieved at fundamental frequency ($f_0$), second harmonic ($2f_0$), third harmonic ($3f_0$) and so on.
6.4 Stability Analysis for Class E Amplifiers

Oscillation can occur in RF power amplifiers (PAs) due to positive feedback caused by the reciprocal properties of the active devices. It also could generate negative input impedance as shown in chapter 5. To simplify the test procedure, the Rollett $K$-factor [90] is normally used to determine if the testing device is unconditionally stable, see (6.1). Two conditions are required for unconditional stability as shown below

\[
K = \frac{1 - S_{11}^2 - S_{22}^2 + \Delta^2}{2 S_{12} S_{21}} > 1
\]

(6.1)

Where, $\Delta = S_{11} S_{22} - S_{12} S_{21}$. For additional conditions, any one of the following five conditions will ensure unconditional stability.

\[
1 + S_{11}^2 - S_{22}^2 - \Delta^2 > 0
\]

(6.2)

\[
1 - S_{11}^2 + S_{22}^2 - \Delta^2 > 0
\]

(6.3)

\[
\Delta < 1
\]

(6.4)

\[
1 - S_{11}^2 > S_{12} - S_{21}
\]

(6.5)

\[
1 - S_{22}^2 > S_{12} - S_{21}
\]

(6.6)

It is well known that the $K$ factor is normally used for stability analysis of linear amplifiers; hence, it has several limitations when used in stability analysis of nonlinear amplifiers. The linear analysis does not account for the instability caused by nonlinear components in PAs. Although the $K$ factor is not accurate, it is simple to obtain. Hence, this analysis still available in used most commercial microwave circuits design.
6.5 Review of High Frequency Nonlinear Model of a Given FET

When active devices (FETs) have been selected, its data sheet could be easily obtained. In this section, the active device models MESFET ATF34143 has been selected and from the data sheet, the maximum drain and source voltage ($V_{ds}$) is equal to 5.5 V and the maximum drain current ($I_{ds}$) is equal to 145 mA when the $V_{ds}$ is equal to 1.5 V. The Statz nonlinear model of the ATF34143 can be seen from Figs. 6.3 to 6.5, the evaluated internal capacitance ($C_I = C_{gs}$) is equal to 0.8 pF, which will be used to determine the $C_I$ in the next section.

6.6 Determine the Turn-on Resistance ($R_{on}$) and Turn-off Resistance ($R_{off}$) for the Given FET

From the data sheet as mentioned above, the IV curves could be obtained and modified in AWR (Microwave Office) software.

Figure 6.3 Typical I-V curves ($V_{GS} = -0.2$ V per step) [14]
Because to the drain voltage ($V_{dd}$) is about equal to the one third of the maximum drain voltage, hence the $V_{dd}$ is used as 3 V in this design for the off condition (when the $V_{GS}$ is equal to -0.6 V) and 0.8 V is used in the on condition.

![IV curves](image)

**Figure 6.4** From the I/V curves to determine the DC resistances

From the figure above, the dc resistance of the device, $R_{on}$, and $R_{off}$ have been calculated, which are equal to 5.3 and 714 $\Omega$. The AC load line of the load resistance ($R_L$) could be determined. In Fig.1, it is can be seen that the $R_L$ is from 11 to 22 $\Omega$ (see Fig. 6.4, \(R_L = \frac{3-0.8 \text{ V}}{100 \text{ mA to 200 mA}}\)), the average optimum impedance ($R_{opt}$) is about equal to 17 $\Omega$. Using the obtained $R_{on}$ (which is about 5 $\Omega = \frac{0.8 \text{ V}}{160 \text{ mA}}$), the shunt capacitance across the FET will be determined in the next section.
6.7 Determine the Shunt Capacitance ($C_s$) Across the Active Device of the Class E PA

Using the ideal waveforms of the class E amplifier, the ideal optimum impedance $R_{opt} = R_L$, which is from 15 to 17 Ω at 2 GHz when $R_{on}$ is equal to 5 Ohms [13], the equation is shown below,

$$C_s = \frac{1}{5.4466R_{opt} \omega_s} \tag{6.7}$$

Where $\omega_s$ is the angular velocity.

When the load of this transistor was fixed (from 15 to 17 Ω), the value of $C_s$ can be calculated, which value is from 0.9 to 1.07 pF.

![Diagram showing the relationship between shunt capacitance, inherent capacitance, external capacitance, and load resistance.]

It is well known, the shunt capacitance is equal to the total value of the inherent and external capacitance, see Fig. 6.5. From the data sheet, it has been given that the inherent capacitance
\(C_l\) is equal 0.8 pF. Hence the external capacitance \(C_{E_l}\) should be from 0.1 pF to 0.27 pF at 2 GHz.

From the empirical experience, it is hard to find the value of the capacitance is lower than 1 pF. Hence the 1 pF external capacitance and 17 \(\Omega\) optimum load \(R_L\) will be used in next section.

### 6.8 Design Matching Networks for the Class E Amplifier

Using the obtained load resistance \(R_L\), the class E PAs will be designed by using lump-elements and then microstrip lines \(M\text{lines}\) will be used to obtain the final results.

As discussed, a 17 \(\Omega\) load resistance will be used in this section. Using the schematic shown in Fig.6.6 and then the value of the inductance will be justified to obtain ideal smooth current and voltage waveforms (see Figs. 6.8 and 6.9). The final value of the inductance has been obtained, which is equal to 1.78 nH. An additional two parallel LC circuits were used to suppress higher harmonics such as at both 2\(^{nd}\) Harmonic (4 GHz) and 3\(^{rd}\) Harmonic (6 GHz) as required.
For the nonlinear model of the amplifier, the optimum impedance $R_{opt}$ is about equal to 17 Ohms. To obtain the input impedance of the given transistor, the schematic will be used in Fig. 6.6.

Figure 6.6: Ideal load harmonic networks for the class E amplifier
The input impedance of the load harmonic network is given below,

From the above figure, it can be observed that the input impedance of the load harmonic networks ($Z_L$) is equal to $17 + j37$ Ohms at 2 GHz and open circuits at 4 and 6 GHz as required (see Chapter 4).
The switch voltage/current waveforms are shown below,

![Current Waveforms](image)

Figure 6.8: Switch current waveform ($I_{ds}$) of the load harmonic network

![Voltage Waveforms](image)

Figure 6.9: Switch voltage waveform ($V_{ds}$) of the load harmonic network

To design the matching networks for the class E amplifier, the first step is to obtain the input impedance looking into the transistor ($Z_{in}$), which is given in Fig. 6.10,
Figure 6.10: Input impedance of the class E amplifier with a 1 pF shunt capacitor.

Figure 6.11: Input impedance of the class E amplifier with a stabilized resistor ($R_s$)
To obtain the high efficiency stabilized class E amplifier, it is necessary to investigate the relationship between the stabilized resistors \( R_s \) and the power added efficiency, which will be given below,

<table>
<thead>
<tr>
<th>( R_s ) (Ω)</th>
<th>( Z_{in} ) (Ω)</th>
<th>Power Added Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-3.168 – j19.24</td>
<td>76.39</td>
</tr>
<tr>
<td>5</td>
<td>1.905 – j19.24</td>
<td>73.28</td>
</tr>
<tr>
<td>12</td>
<td>9.008 – j19.21</td>
<td>69.2</td>
</tr>
<tr>
<td>22</td>
<td>19.15 – j19.09</td>
<td>63.7</td>
</tr>
</tbody>
</table>

Table 6.1: the relationship between the stabilized resistors \( R_s \) and the power added efficiency

### 6.9 Design of a High Efficiency Stabilized Class E Amplifier using Microstrip Lines

From previous section, it can be discovered that to obtain the stabilized class E amplifier, the stabilized resistors, \( R_s \), have to be used, as the real part of \( Z_{in} \) can become negative (see Fig. 6.10). This will reduce the efficiency of the amplifier.

The electrical and physical parameters of the substrate PCB FR4 used are: dielectric constant is 4.3, the height of substrate is 1.575 mm, the loss tangent is 0.019 and the thickness of the copper patch is 0.035mm.

By using one of the topologies in Fig.6 (the dimensions of the class E amplifier are shown in Table 6.2) will be used to obtain the final results, which will be given in Table 6.3.
In the above schematic, M1 and M2 are the source matching networks at the fundamental frequency \(f_0 = 2\ \text{GHz}\), M4 and M5 are used to create high impedance at 6 GHz (3\(^{rd}\) Harmonic), M6 and M7 are to generate high impedance at 4 GHz (2\(^{nd}\) Harmonic), M8 and M9 are the matching networks at 2 GHz. The gate voltage \(V_{gg}\) is equal to -0.7 V and the drain voltage \(V_{dd}\) is equal to 3V.
<table>
<thead>
<tr>
<th>Width (mm)</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>M5</th>
<th>M6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length (mm)</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Width (mm)</th>
<th>M7</th>
<th>M8</th>
<th>M9</th>
<th>C</th>
<th>C1</th>
<th>C2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length (mm)</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>1000 pF</td>
<td>2.2 nF</td>
<td>15 nF</td>
</tr>
</tbody>
</table>

Table 6.2: The dimensions of the class E amplifier with dc block capacitance (C=100 pF)

<table>
<thead>
<tr>
<th>$R_o$ (Ω)</th>
<th>$Z_{in}$ (Ω)</th>
<th>Power Added Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1.191 + j10.93</td>
<td>76.39</td>
</tr>
<tr>
<td>5</td>
<td>6.359 + j10.59</td>
<td>73.28</td>
</tr>
<tr>
<td>12</td>
<td>13.42 + j9.378</td>
<td>69.2</td>
</tr>
<tr>
<td>22</td>
<td>22.89 + j6.274</td>
<td>63.7</td>
</tr>
</tbody>
</table>

Table 6.3: the relationship between the stabilized resistors, $R_o$, and the power added efficiency, PAE

From table 6.2 above, it can be seen that the potential efficiency of the class E amplifier is about 77% which is matched to the research in chapter 4, which is using a novel quadratic equation (3.28) (76.268 %) and Genetic Algorithms (77.369 %) when $R_o$ is equal to 5 Ohms and the $R_s$ is equal to 0 Ohms (See table 4.4 and 4.6). But unfortunately, to stabilise the class E amplifier and to ease design of the source matching networks, the $R_s = 22$ Ohms will be used to design the high efficiency stabilized power amplifier.
6.10 Simulation Results of the Class E Amplifier using PCB-FR4

In this section, simulation is carried out for the stability $K$ factor; switch waveforms, $S$ parameters and the power added efficiency of the class E amplifier from the last section.

First of all, using AWR (Microwave Office) simulation tools, the designed class E amplifier has been simulated as shown below,

![Simulation block diagram using AWR software](image)

**Figure 6.13: Simulation block diagram using AWR software**

Using voltage and ampere meters, the switch current flowing through the transistor and the switch voltage across the transistor could be obtained when the input power is equal to 12 dBm as shown,
The frequency response of the stability factor $K$ is over 1.4 showing in Fig. 6.15, it can be obtain that the designed PA is unconditionally stable over the frequency range 1.9 to 2.1 GHz.
The frequency response of the $S_{11}$, $S_{22}$ and $S_{12}$ are shown in Figs. 6.16, 6.17 and 6.18 where the input power is 12 dBm.

Figure 6.16: Simulated $S_{11}$ at $P_{in} = 12$ dBm

Figure 6.17: Simulated $S_{22}$ at $P_{in} = 12$ dBm
Figure 6.18: Simulated $S_{12}$ at $P_{in} = 12$ dBm

Frequency response of the gain is shown below

Figure 6.19: Simulated Gain when $P_{in} = 12$ dBm
From above figures, the gain of the designed amplifier in simulation results is over 7 dB at 2 GHz and the simulated PAE will be equal to 59.6% at 2 GHz and input power is 12 dBm as shown in Fig. 6.20.

![Swept PAE](Image)

**Figure 6.20: The simulated PAE of the designed class E PA**

From above figures, it shows the balance between the matching and efficiency. When complexity input and output harmonic networks are used, excellent reflect coefficient parameters, $S_{11}$ and $S_{22}$ will be obtained. But when more and more Mlines are used for matching, more and more losses will be occurred and the efficiency will be reduced.

In this project, high efficiency class E PAs are required and the efficiency will be the main objective to be concentrated. Because the load harmonic networks are more complex than input harmonic network, the load performance $S_{22}$ is better than input performance $S_{11}$. 
6.11 Implementation and Measurement

A photograph of the fabricated class E PA is shown in Fig. 6.21, which has the equivalent circuit model discussed in last sections. The model is verified using the electromagnetic simulator, Microwave Office (AWR). The amplifier is designed using PCB-FR4 substrate with a dielectric constant of 4.3.

![Photograph of the fabricated class E PA](image)

Figure 6.21 Photograph of the fabricated class E PA

The measurement block diagram is shown in Fig. 6.22, and a photograph of the measurement is shown in Fig. 6.23. The power added efficiency and the gain are measured and shown in Table 6.3. An Agilent PSW signal generator was used to generate 2 GHz and up to 14 dBm.
input signal, an Agilent Oscilloscope DSO9254A was used to measure the output power. At 12.56 dBm input level, 4.3 dB Gain and 71.66% PAE are achieved.

Figure 6.22: The block diagram of the measurement setup

Figure 6.23: A typical measurement setup for the power amplifier
The input and output voltage waveforms operates at 2 GHz will be plotted below,

(a) Class E Amplifier Performance at 0 dBm

(b) Class E Amplifier Performance at 4 dBm
Figure 6.24: Input and output voltage waveforms operate at 2 GHz using Agilent Oscilloscope DSO9254A

<table>
<thead>
<tr>
<th>$P_{in}$ (dBm)</th>
<th>Real $P_{in}$ (dBm)</th>
<th>$P_{out}$ (dBm)</th>
<th>$P_{dc}$ (dBm)</th>
<th>$I_{dc}$ (mA)</th>
<th>PAE (%)</th>
<th>Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-0.87</td>
<td>0.6</td>
<td>7.08</td>
<td>1.7</td>
<td>6.43</td>
<td>1.46</td>
</tr>
<tr>
<td>2</td>
<td>0.59</td>
<td>1.95</td>
<td>8.57</td>
<td>2.4</td>
<td>5.87</td>
<td>1.37</td>
</tr>
<tr>
<td>4</td>
<td>2.44</td>
<td>4.52</td>
<td>9.82</td>
<td>3.2</td>
<td>11.25</td>
<td>2.09</td>
</tr>
<tr>
<td>6</td>
<td>4.46</td>
<td>6.42</td>
<td>11.21</td>
<td>4.4</td>
<td>12.02</td>
<td>1.95</td>
</tr>
<tr>
<td>8</td>
<td>6.53</td>
<td>9.95</td>
<td>12.55</td>
<td>6</td>
<td>29.98</td>
<td>3.42</td>
</tr>
<tr>
<td>10</td>
<td>8.67</td>
<td>12.54</td>
<td>13.91</td>
<td>8.2</td>
<td>42.95</td>
<td>3.86</td>
</tr>
<tr>
<td>12</td>
<td>10.74</td>
<td>14.6</td>
<td>15.11</td>
<td>10.8</td>
<td>52.44</td>
<td>3.86</td>
</tr>
<tr>
<td>14</td>
<td>12.56</td>
<td>16.86</td>
<td>16.29</td>
<td>14.2</td>
<td>71.66</td>
<td>4.30</td>
</tr>
</tbody>
</table>

Table 6.4: Gain and PAE vs. input power at 2 GHz
After counting the losses of the coaxial cables, the PAE of the designed class E amplifier has achieved over 71% at $P_{in} = 12.56$ dBm at 2 GHz, which is in agreement with the simulation results in the last sections and the predicted results in Chapter 4 by using new quadratic equations and GA. Even the resulting measured PAE is slightly higher than the simulation, because the nonlinear transistor is from the produced data sheet by vendor, which is not accurate. After sweeping the operating frequency of the class E PA, the response of Gain are given below,

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>$P_{in} = 10$ dBm</th>
<th>$P_{in} = 12$ dBm</th>
<th>$P_{in} = 14$ dBm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>7.27</td>
<td>6.97</td>
<td>6.51</td>
</tr>
<tr>
<td>1.2</td>
<td>6.51</td>
<td>6.31</td>
<td>5.19</td>
</tr>
<tr>
<td>1.4</td>
<td>5.33</td>
<td>5.27</td>
<td>5.15</td>
</tr>
<tr>
<td>1.6</td>
<td>4.67</td>
<td>4.60</td>
<td>4.48</td>
</tr>
<tr>
<td>1.8</td>
<td>4.15</td>
<td>4.05</td>
<td>4.40</td>
</tr>
<tr>
<td>2</td>
<td>3.86</td>
<td>3.86</td>
<td>4.30</td>
</tr>
<tr>
<td>2.2</td>
<td>3.33</td>
<td>3.25</td>
<td>3.22</td>
</tr>
<tr>
<td>2.4</td>
<td>2.74</td>
<td>2.69</td>
<td>2.75</td>
</tr>
<tr>
<td>2.6</td>
<td>1.61</td>
<td>1.69</td>
<td>1.67</td>
</tr>
<tr>
<td>2.8</td>
<td>-0.28</td>
<td>-0.40</td>
<td>-0.36</td>
</tr>
<tr>
<td>3</td>
<td>-3.33</td>
<td>-3.18</td>
<td>-3.25</td>
</tr>
</tbody>
</table>

Table 6.5: Response of Gain by sweeping frequency from 1 to 3 GHz at various input power ($P_{in}$)
From Table 6.5, it can be seen that the bandwidth of the class E PA is really broad, which matches the results in chapter 4. And it proves that even the small ‘Q’ factor networks have only a minor effect on efficiency, allowing a wide bandwidth to be obtained.

The Gain of the class E PA is over 7 dB at low frequency (e.g. 1 GHz), which is matched the previous simulation result (see Fig. 6.19); due to the lossy material (PCB FR4) has been used, lower Gain (around 4dB) is obtained at high frequency (e.g. 2 GHz). After 2.4 GHz, the Gain drops down dramatically, which matches the results in Fig. 6.19.

6.12 Summary

In this chapter, a novel procedure of design of a high efficiency class E amplifier has been introduced, which is using the data sheet of the given active device (ATF 34143) to obtain the turn-on resistance, \( R_{on} \), and then the shunt capacitance, \( C_s \), will be determined by using the obtained \( R_{on} \). Finally how to design of a high efficiency stabilized class E amplifier has been investigated, in which the stabilized resistors (\( R_s \)) is equal to 12 Ohms will used in the practical fabrication procedure.

In this chapter, the active device models have been reviewed. The most popular and efficiency method to measure the input and output impedance of the nonlinear active devices is to use passive or active load/source-pull measurement methods has be introduced.

A novel procedure of designing high efficiency class E PAs has been introduced to reduce the research cost, shorten the design period and save the energy of the wireless communication systems. The new method will increase the PAE of the conventional power to over 71%. From the achievement, it can be seen that if a new method could be investigated without stabilized resistance; the PAs could achieved over 76% or even more.
Finally the designed class E PAs have been fabricated and measured, the Gain of the class E PAs over 3.8 dB and the PAE of the class E PA has achieved over 52.44% at $P_{in} = 12$ dBm and 71.66% at $P_{in} = 14$ dBm at 2 GHz.
Chapter 7 Conclusions and Future Work

7.1 Conclusions

This section presents a brief summary of the important outcome of this research carried out on using mitigation technologies to increase the efficiency, reduce cost, broad bandwidth and simplify the procedure of circuitries design.

Chapter 2 initially reviewed the basic concepts and the implementation of GA. In the case of a dual frequency antenna had two objectives, as matching was required to be obtained at the two design frequencies. These objective functions were combined into three possible single global functions. They were then used in the GA, to determine the optimum dimensions of the patch and the position of the probe feed, to satisfy the requirements for the return loss at each frequency. For two of the objective functions although good results were obtained the return losses at each frequency were not similar. The third global function produced excellent and similar results for the return loss. Using the optimised design parameters the dual frequency patch was manufactured and tested. An excellent agreement was obtained between the predicted, modelled and practical results and based on this work a paper was published [54].
In chapter 3 which investigated the basic concepts of class E power amplifiers, the active device was modelled as a switch in series with the $R_{on}$ resistance and an ideal harmonic load was assumed. For the ideal case when $R_{on}$ was equal to zero, 100% efficiency of power conversion was obtained. It was found that if $R_{on}$ was finite the effect was to reduce input dc power, ac output power and caused the current/voltage waveforms to overlap.

In chapter 4, the performance of the output stage for the class E amplifier was investigated, where the active device was modelled as a switch in series with $R_{on}$. However the ideal harmonic load had been replaced by a series resonant circuit. Consequently there were additional losses due the harmonic currents flowing in the load resistance. In [57] to reduce this loss caused by the harmonic currents, a high $Q$ factor of the circuit was used. However when a high $Q$ factor was used the efficiency bandwidth was reduced.

In Chapter 5 ideal lossless transmission lines (Tlines) have been used in the initial design of harmonic networks for high efficiency power amplifiers, and then practically realised using microstrip lines (Mlines). As the metal and substrate losses in Mlines are normally expressed in terms of attenuation constants, these losses are difficult to determine as they required solutions of complex mathematical equations. To reduce such complex analysis, losses in a Mline have been modelled as Tlines in series with a resistance. A novel method was proposed to determine this resistance as a function of the length of the Mline, which was realised using both inexpensive PCB FR4 and expensive Duroid 5870 substrates (see Appendix D). Then for the above two line models, harmonic networks were designed up to the second and third harmonics and the obtained losses at the design frequency compared. Finally, the effect of the losses with different harmonic networks on class E PAs was investigated.
In chapter 6 active device models were reviewed. The most popular and efficiency method for measuring the input and output impedance of nonlinear active devices, the load/source-pull measurement method, was introduced.

A novel procedure for designing high efficiency class E PAs was introduced to reduce the research cost, shorten the design period and save energy in wireless communication systems. The new method increases the PAE of the conventional power to over 71%. However is limited in practice by the use of a stabilising resistor. If this can be removed the PAs could achieve over 76% efficiency.

This project also proved that the power loss due to the harmonic currents in the load resistor is very small and hence the efficiency largely depends on $R_{on}$. Therefore low $Q$ factor harmonic networks can be applied and achieve both high efficiency and a wide bandwidth which has been proved from practical measurement.

Finally the designed class E PAs have been fabricated and measured, the Gain of the class E PAs over 3.8 dB and the PAE of the class E PA has achieved over 52.44% at $P_{in} = 12$ dBm and 71.66% at $P_{in} = 14$ dBm at 2 GHz. Showing good agreement with theory.

7.2 Future Work

In this section, two areas of future work are proposed. The first proposal is to investigate how to further increase the efficiency of the class E PAs without sacrificing stability. The second suggestion is to improve the bandwidth of the AIAs, by using GAs to design a coupled slot antenna, which will be used in the load networks of the PAs.
7.2.1 Investigating on Increasing the PAE of the designed Class E PAs

From the achievement in chapter 4, it can be seen that the potential efficiency of the class E PAs could achieve over 80% without stabilized resistance; hence the first proposal of the future work will be to investigate the class E PAs to achieve the PAE over 76%.

7.2.2 Investigating on Increasing the Bandwidth of the Load Patch Antennas

By applying Genetic Algorithms optimization methods (see chapter 2), a probe fed patch antenna has been designed for replacing the load harmonic networks of the class E power amplifier, which could generate the input impedance, which is equal to 50 Ohms at 2 GHz and high input impedance (over 100 Ohms) at 4 GHz as shown below,

![Figure 7.1 Input impedance of the dual frequency patch antenna](image)

From the above figures, it can be seen that by using the GA and relevant equations in chapter 2, a dual frequency antenna could be fabricated, which could generate an input impedance $Z_{in}$
equal to 50 Ohms at 2 GHz and high impedance (100 Ohms) at the $2^{nd}$ harmonic (4 GHz) as class E PAs require. After replace the load harmonic class E PAs by using this dual frequency patch antenna, the size will be reduced.

But this narrow band patch will reduce the bandwidth of the designed class E PAs; hence, it is necessary to investigate the slot antenna in the future work.[15, 58, 91-97]

The main advantages of a microstrip patch antenna that it is light weight, inexpensive to manufacture, has a low profile and can be fed by a variety of method [14, 54, 58, 77, 79, 98-104]. However the main disadvantage is that it has a narrow bandwidth which can be increased by using a thick substrate or stacking the patches however these antennas exhibit poor radiation [80].

As a part of the future work of this project, a new PhD student Lei Liu in University of Northumbria at Newcastle upon Tyne has already worked on it and his PhD project is using GA to design slot antennas and some of our collaboration research will be shown below,

Figure 7.2 The top view (a), side view (b), after fabricated of the circular polarised broadband slot patch antenna
After designing, fabrication and testing the broad band slot antenna, it will be necessary to use the GA to simplify the procedure for the design of a slot antenna in the future work.
References


Appendix A Design of a Probe Fed Dual Frequency Patch Antenna

Matlab programme code of design of a probe fed dual frequency patch antenna:

```matlab
function [err,Z]=objval2(x0)
range 30-45 25-35 5-20 5-15
x0=x0*diag([15 19])*1e-3;
x0=x0+ones(size(x0))*diag([5 5])*1e-3;
f=[2.38e9 1.83e9];
Z=zeros(size(x0,1),2);
Z(:,1)=feed_p2(39.4e-3,30.4e-3,x0(:,1),x0(:,2),f(1));
Z(:,2)=feed_p2(39.4e-3,30.4e-3,x0(:,1),x0(:,2),f(2));
err=real(Z'.50).^2;\nerr=imag(Z').^2;\nerr=1./err;
%Function to be maximised
%objval=@(x) prod(sin(x*pi),2);
nc=2;
ng=20; %number of genes per chromosome
maxit=50; % Number of iterations
np=1e4; %Population Size
Ch=rand(np,ng*nc)>.5; %Throw forst population with random genes (50% ones 50% zeros)
bits=2.^(ng:-1:1)-ng; % Number corresponding to each bit 0-4 in our case.
inds=1:ng;
for it=1:maxit
    Phen=zeros(np,nc);
    for k=0:nc-1;
        Phen(:,k+1)= Ch(:,k*ng+(1:ng))*bits; \n    end
    [fitness,Z]= objval2(Phen);
    [dum,i]=sort(fitness,'descend'); %sorts each column of a matrix in descending order
    Ch=Ch(i,:); fitness=fitness(i,:); Phen=Phen(i,:);Z=Z(i,:);
    fitness=fitness.^6; % Accelerator to
    [dum,inds]=histc(rand(1,np),[0 ;cumsum(fitness/sum(fitness))]);
    sel=Ch(inds,:); %Select 1 bit per chromosome to swap over for the new population and
    sel=sel';Ch=Ch';
    bit=ceil(ng*rand(1,np))+(0:ng:((np*ng)-1)); sel(bit)=Ch(bit);
    sel=sel';Ch=Ch';
    %Add mutation with probability pm. Mutation rate decreases with time
    pm=0.001.^(it/20); rm=find(rand(size(sel))<pm); %Find indices and values of nonzero elements
    sel(rm)=-sel(rm); % not
    Ch=sel;
    disp([Phen(1,:)*diag([15 19])+ones(size(Phen(1,:)))*diag([5 5])])
    disp(Z(1,:));
    plot(fitness,Z),pause
end
```

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for k=0:nc-1; Phen(:,k+1)= Ch(:,k*ng+(1:ng))*bits; end

[fitness,Z]= objval(Phen);
[dum,i]=sort(fitness,'descend');
Ch=Ch(i,:); fitness=fitness(i,:); Phen=Phen(i,:);
Phen(1,:)*diag([15 19])+ones(size(Phen(1,:)))*diag([5 5]);
f=[2.38e9 1.83e9];
Appendix B  Concepts of Class E Power Amplifiers

B.1 Derivation of the Equations for the Voltage and Current Waveforms for \( R_{on} \neq 0 \)

The approximate equivalent circuits of the active device for the two conditions are shown below,

I. ON STATE: \((\frac{T_s}{2} \leq t \leq T_s)\)

\[
C_s \quad \rightarrow \quad R_{ON} \quad \rightarrow \quad C_s
\]

II. OFF STATE: \((0 \leq t \leq \frac{T_s}{2})\)

\[
C_s \quad \rightarrow \quad R_{OFF} \quad \rightarrow \quad C_s
\]

For the off state the current in the capacitor given by equation (B.1),

\[
c_s \frac{dV_{s1}(t)}{dt} = I_{dc}(1 - a_r \sin \omega_s t + \phi_r) ; \quad (B.1)
\]

The switch voltage \( v_{s1}(t) \) in (B.2) is obtained by integrating (B.1) where the constant \(2R_{on}I_{dc} \) is obtained when \( t = 0 \),
\[ v_{s1}(t) = \frac{I_{dc}}{\omega_s C_s} \omega_s t + a_r \cos \omega_s t + \varphi_r - \cos \varphi_r + 2R_{on} I_{dc}; \]  \hspace{1cm} \text{(B.2)}

Substituting the condition 2 in section 3.2.2, \((v_{s1}(\frac{T_s}{2}) = v_{s2}(\frac{T_s}{2}) = 0)\) (B.2) results in

\[ \frac{I_{dc}}{\omega_s C_s} \omega_s \left(\frac{T_s}{2}\right) + a_r \cos \omega_s \left(\frac{T_s}{2}\right) + \varphi_r - \cos \varphi_r + 2R_{on} I_{dc} = 0 \]  \hspace{1cm} \text{(B.3)}

and hence

\[ \pi - 2a_r \cos \varphi_r + 2R_{on} I_{dc} = 0. \]  \hspace{1cm} \text{(B.4)}

The above equation can be simplified as

\[ \cos \varphi_r = \frac{\pi}{2} + R_{on} \omega_s C_s. \]  \hspace{1cm} \text{(B.5)}

For the on state when the switch is closed the current now flows in the \(R_{on}\) resistance and

\[ v_{s2}(t) = R_{on} I_{dc} (a_r \sin \omega_s t + \varphi_r). \]  \hspace{1cm} \text{(B.6)}

Applying the condition 1 in section 3.2.2 \((v_{s2}(T_s/2) = 0)\) in (B.6)

\[ 1 + a_r \sin \varphi_r = 0 \]  \hspace{1cm} \text{(B.7)}

Using (B.5) and (B.6) it can be shown that the two constants are given by (B.7) and (B.8).
\[
a_r = 1 + \frac{\pi}{2} + \omega_s C_s R_{on}^2 z^{1/2}; \quad (B.7)
\]

\[
tan\varphi_r = \frac{-1}{\frac{\pi}{4} + \omega_s C_s R_{on}}. \quad (B.8)
\]

**B.2 Derivation of the \(I_{dc}\) and the Optimum Impedance at the Design Frequency where \(R_{on} = 0\)**

\[
V_{dc} = \frac{1}{\tau_s} \int_0^\tau_s v_{st} t \, dt + \frac{\gamma_t}{2} v_{sz} t \, dt
\]

\[
= \frac{1}{\tau_s} \int_0^\tau_s \frac{I_{dc}}{\omega_s C_s} \omega_s t + a_r \cos \omega_s t + \varphi_r - \cos \varphi_r + R_{on} I_{dc} (1 - a_r \sin \varphi_r) \, dt + \frac{\gamma_t}{2} R_{on} I_{dc} 1 - a_r \sin \omega_s t + \varphi_r \, dt
\]

\[
= \frac{I_{dc}}{\omega_s C_s} \frac{\tau_s^2}{8} + a_r \frac{\tau_s}{\omega_s} - \frac{2\sin \varphi_r}{\omega_s} - a_r \cos \varphi_r \frac{\tau_s}{2} + \frac{R_{on} I_{dc}}{2} (1 - a_r \sin \varphi_r) + \frac{R_{on} I_{dc}}{2} + \frac{2R_{on} I_{dc} a_r \cos \varphi_r}{\tau_s}
\]

\[
= \frac{I_{dc}}{\omega_s C_s} \pi \frac{a_r \sin \varphi_r}{\pi} - \frac{a_r \cos \varphi_r}{\pi} + \frac{R_{on} I_{dc}}{2} - \frac{R_{on} I_{dc}}{2} a_r \sin \varphi_r + \frac{R_{on} I_{dc}}{2} + \frac{R_{on} I_{dc} a_r \cos \varphi_r}{\pi} \quad (B.9)
\]

Applying (B.5) and (B.7), (B.9) can be simplified as

\[
I_{dc} = \frac{V_{dc}}{1 + \frac{1}{2} R_{on} + \frac{\omega_s C_s R_{on}^2}{\pi}} \quad (B.10)
\]

Fourier series is defined as

\[
v_s = \sum_{n=-\infty}^{\infty} K_n e^{j\omega_s t} \quad (B.11)
\]
The integration is performed over the whole period to obtain the switch voltage at the design frequency is shown in (B.14).

\[
K_n = \frac{1}{T_0} \int_0^{T_0} v_{s1} t e^{-jn\omega_s t} dt + \frac{T_0}{\tau_2} v_{s2} t e^{-jn\omega_s t} dt \tag{B.12}
\]

\[
K_1 = \frac{1}{T_0} \int_0^{T_0} v_{s1} t e^{-jn\omega_s t} dt + \frac{T_0}{\tau_2} v_{s2} t e^{-jn\omega_s t} dt \tag{B.13}
\]

The optimum input impedance of the external load harmonic network is obtained from B.15.

\[
v_s(\omega_s t) = 2K_1 \cos(\omega_s t + \theta_r) = 2K_1 \sin(\omega_s t + \frac{\pi}{2} + \theta_r) \tag{B.14}
\]

The optimum input impedance of the external load harmonic network is obtained from B.15.

\[
Z_{inopt} = \frac{v_s(\omega_s t)}{i_R(\omega_s t)} = \frac{2K_1}{a_r I_{dc}} e^{j(\omega_s t + \theta_r - \phi_r)} \tag{B.15}
\]

**B.3 Derivations of New Equations for the Voltage/Current Waveforms and Optimum Impedance**

When \( t = T_s/2 \) (3.9) and (3.13) are evaluated as shown below.

\[
v_{s1} \frac{T_s}{2} = R_{on} I_{dc} \left( 1 - a_r \sin \left( \frac{2\pi T_s}{T_s} + \phi_r \right) \right)
\]
For the condition \( v_{s1}\left(\frac{T_s}{2}\right) = v_{s2}\left(\frac{T_s}{2}\right) \neq 0 \) (see section 3.2.3), the required equation is shown below (B.16).

\[
\frac{I_{dc}}{\omega_s c_s} \frac{2\pi T_s}{T_s} + a_r + \cos \frac{2\pi T_s}{T_s} + \varphi_r - \cos \varphi_r + R_{on} l_{dc} (1 - a_r \sin \varphi_r)
\]

\[
= \frac{I_{dc}}{\omega_s c_s} \pi + a_r + \cos \varphi_r - \cos \varphi_r + R_{on} l_{dc} (1 - a_r \sin \varphi_r)
\]

\[
= \frac{I_{dc}}{\omega_s c_s} \pi - 2a_r \cos \varphi_r + R_{on} l_{dc} (1 - a_r \sin \varphi_r)
\]

For the condition \( v_{s1}\left(\frac{T_s}{2}\right) = v_{s2}\left(\frac{T_s}{2}\right) \neq 0 \) (see section 3.2.3), the required equation is shown below (B.16)

\[
R_{on} l_{dc} 1 + a_r \sin \varphi_r = \frac{I_{dc}}{\omega_s c_s} (\pi - 2a_r \cos \varphi_r) + R_{on} l_{dc} (1 - a_r \sin \varphi_r)
\]

\[
R_{on} 1 + a_r \sin \varphi_r = \frac{1}{\omega_s c_s} (\pi - 2a_r \cos \varphi_r) + R_{on} (1 - a_r \sin \varphi_r)
\]

\[
\frac{1}{\omega_s c_s} \pi - 2a_r \cos \varphi_r = 2R_{on} l_{dc} \sin \varphi_r.
\]  

(B.16)

(B.9) can now be expressed as the objective function in the form shown in B.17.

\[
\frac{1}{\omega_s c_s} \pi - 2a_r \cos \varphi_r = 2R_{on} l_{dc} \sin \varphi_r
\]

\[
\frac{1}{\omega_s c_s} \pi - 2a_r \cos \varphi_r = 2R_{on} l_{dc} \left(1 - \cos^2 \varphi_r\right)
\]
Objective Function could be achieved as shown below,

\[
\frac{1}{\omega_y C_s} \pi - 2a_r \cos \varphi_r = 4R_{on}^2 I_{dc}^2 (1 - \cos^2 \varphi_r)
\]

B.4 Matlab Program to Determine ‘\(a_r\)’ and ‘\(\varphi_r\)’ in (B.17)

```matlab
Cs=1e-12;
f=2e9;
omega=2*pi*f;
Ron=5;
Vdc=5;
[ar,phir]=meshgrid(1.7:0.05:2.3, -34:0.5:-27);
phir=phir.*pi./180;
Y=(1+(Ron*Cs*omega).^2.*((4*pi.*ar.*cos(phir).^2)-(4*pi.*ar.*cos(phir)+pi.^2-4*Ron^2*(omega.^2)*Cs.*ar.^2));
surf(ar,phir,min(0,Y))
```
Appendix C Using GA to Investigate the Class E Amplifier

C.1 GA is used to investigate the Ideal Load Harmonic Networks for Class E Amplifiers ($R_{on} = 0$)

function goal=Load_Net_fn(f0,Q)
cs=1e-12; Ron=0.01; fs=2e9; c=3e8; Vdc=5; omegas=2*pi*fs; omega0=2*pi*f0; T0=1/fs;
phi=-32.48/180*pi;
dt=0.005.*T0;t=[0:dt:T0/2];f=[1e9:1e9:9e9]; Idc=pi*omegas*cs*Vdc;
av=0.522./(omegas*cs); Idc/(omegas*cs*T0);
ar=sqrt(1+(pi/2+omegas*cs*Ron).^2); RL=14.68;
i=sqrt(-1);

% Switch Voltage
% First Harmonic
V1st=2*Idc./(omegas*cs*pi)*abs(pi^2/8-1-i*pi/4);

% Second Harmonic
V2nd=2*Idc./(omegas*cs*pi)*abs((4+i*pi)/12);

% Third Harmonic
V3rd=2*Idc./(omegas*cs*pi)*1/9;

Zopt1=abs(RL*(1+i*Q.*(omegas^2-omega0.^2)./(omega0*omegas)));
Zopt2=abs(RL*(1+i*Q.*(4*omegas^2-omega0.^2)./(2*omega0*omegas)));
Zopt3=abs(RL*(1+i*Q.*(9*omegas^2-omega0.^2)./(3*omega0*omegas)));

I1=ar*Idc;
I2=V2nd./Zopt2;
I3=V3rd./Zopt3;

P1=1/2.*(abs(I1.^2))*RL;
P2=1/2.*(abs(I2.^2))*RL;
P3=1/2.*(abs(I3.^2))*RL;
Pdc=Idc.*Vdc;
goal=100.*(Pdc-P2-P3)./Pdc; 

Plotting the Three Dimensions Figures:
[f0,Q]=meshgrid(1.7:.002:1.95,1:.05:5);
goal=Load_Net_fn(1e9*f0,Q);
figure(1)
[C,h]=contour(f0,goal,Q);
[C,h]=contour(f0,Q,goal);
set(h,'ShowText','on','TextStep',get(h,'LevelStep')*2)
xlabel('Frequency (GHz)'),ylabel('Q value'),title('Efficiency (%)')

%xlabel('Frequency (GHz)'),ylabel('Efficiency (%)'),zlabel('Q value'),title('Efficiency Vs Q value Vs Frequency')
%xlabel('Frequency'),ylabel('Efficiency'),title('Q value')
colormap cool
figure(2)
%surf(f0,Q,10*log10(goal)),shading('interp')
surf(f0,Q,goal),shading('interp')
%xlabel('Frequency'),ylabel('Q value'),title('Losses in dB')
xlabel('Frequency (GHz)'),ylabel('Q value'),zlabel('Efficiency (%)'),title('Efficiency Vs Q value Vs Frequency')

C.2 GA is used to investigate the Optimum Load Harmonic Networks for Class E Amplifiers ($R_{\text{on}} \neq 0$)

nc=2;
ng=20; %number of genes per chromosome
maxit=50; % Number of iterations
np=1e2; %Population Size
Ch=rand(np,ng*nc)>.5; %Throw first population with random genes (50% ones 50% zeros)
bits=2.^(ng:-1:1)-ng-1); % Number corresponding to each bit 0-4 in our case.
inds=1:ng;

for i=1:maxit
    Phen=zeros(np,nc);
    for k=0:nc-1; Phen(:,k+1)=Ch(:,k*ng+(1:ng))*bits; end
    fitness= amplifier_e_GA(Phen);
    [dum,i]=sort(fitness,'descend');
    Ch=Ch(i,:); fitness=fitness(i,:); Phen=Phen(i,:);
    fitness=max(0,fitness)+1e-10;
    %fitness=fitness.^6; % Accelerator to
    [dum,inds]=histc(rand(1,np),[0 :cumsum(fitness/sum(fitness))]);
    sel=Ch(inds,:); %Select 1 bit per chromosome to swap over for the new population and
    %swap
    sel=sel\';Ch=Ch;
    bit=ceil((ng*rnd(1,np))+((0:ng:(np*ng)-1));
    sel(bit)=Ch(bit);
    sel=sel\';Ch=Ch;
    %Add mutation with probability pm. Mutation rate decreases with time

150
pm=0.0001.^(it/20);  rm=find(rand(size(sel))<pm);  sel(rm)=~sel(rm);
Ch=sel;
disp([Phen(:,1).*diag([1.7 30])+ones(size(Phen(:,1)))*diag([1.3 -60])]);

% plot(fitness,Z),pause
end

function Efficiency=amplifier_e_GA(phen);
ar=phen(:,1)*1.7+1.3;
phir=phen(:,2)*30-60;
Efficiency=amplifier_e(ar,phir);

function Efficiency=amplifier_e(ar,phir)
Cs=1e-12;
f=2e9;
omega=2*pi*f;
Ron=30;
Vdc=5;

phir=phir.*pi./180;

Y=(1+(Ron*Cs*omega).^2)*4.*ar.^2.*cos(phir).^2-4*pi.*ar.*cos(phir)+pi.^2-
4*Ron^2*(omega.^2)*(Cs.^2).*ar.^2;

Idc=Vdc/(1/(omega.*Cs)*(pi/4-
ar.*sin(phir)./pi-
ar.*cos(phir)./2)+Ron-
Ron/2.*ar.*cos(phir)/pi);
Pdc=Vdc^2./(1/(omega.*Cs)*(pi/4-
ar.*sin(phir)/pi-
ar.*cos(phir)/2)+Ron-
Ron/2.*ar.*cos(phir)/pi);

ks1=Idc./(2*pi.*omega.*Cs).*((2-ar.*cos(phir).*pi/2+j.*(pi-2.*ar.*cos(phir)-ar./2.*pi.*sin(phir))));
ks1dc=-j*(Ron.*Idc/pi.*(1-ar.*sin(phir)));
ks2=Ron.*Idc./(2*pi).*(-1.*ar.*sin(phir).*((pi/2)+j*(2+ar.*cos(phir).*((pi/2))));
k1=ks1+ks1dc+ks2;

Re=Idc./(2*pi.*omega.*Cs).*(-2-ar.*cos(phir).*pi/2)-Ron.*Idc/4.*ar.*sin(phir);
Im=Ron.*Idc/(2*pi).*(-2+ar.*cos(phir).*pi/2)-Ron.*Idc/pi.*(1-ar.*sin(phir)-Idc/(2*pi.*omega.*Cs).*((pi-
2.*ar.*cos(phir)-ar./2.*sin(phir)));
V1=Re+j*Im;

thetav=atan2(imag(V1),real(V1));
K1=abs(V1);
Zopt=2.*K1./(ar.*Idc).*((exp(j.*(thetav+pi./2-phir))));
RL=real(Zopt);
Pout=(ar.*Idc).^2.*RL/2;
Efficiency = \frac{P_{out}}{P_{dc}} \times 100;
Appendix D Investigate the Losses of the Harmonic Networks of Class E PAs

D.1 Losses in a Suppressed Second Harmonic Network using Duroid 5870
Figure d.1: The obtained S-parameters using Duroid 5870 substrate (a) $S_{11}$, (b) $S_{22}$ and (c) $S_{21}$

**D.2 Losses in a Suppressed Second and Third Harmonics Network using Duroid 5870**

The lengths and the values of the resistances for Duroid 5870 substrates are summarised in the two tables below.

\[(c)\]

<table>
<thead>
<tr>
<th></th>
<th>Length of the Microstrip Lines (mm)</th>
<th>Equivalent Resistance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M1$</td>
<td>10.2</td>
<td>$R_1 = 0.071$</td>
</tr>
<tr>
<td>$M2$</td>
<td>20.5</td>
<td>$R_2 = 0.143$</td>
</tr>
<tr>
<td>$M3$</td>
<td>10</td>
<td>$R_3 = 0.070$</td>
</tr>
<tr>
<td>$M4$</td>
<td>6.8</td>
<td>$R_4 = 0.047$</td>
</tr>
<tr>
<td>$M5$</td>
<td>24.4</td>
<td>$R_5 = 0.170$</td>
</tr>
<tr>
<td>$M6$</td>
<td>12.2</td>
<td>$R_6 = 0.085$</td>
</tr>
</tbody>
</table>
### (b)

<table>
<thead>
<tr>
<th></th>
<th>Length of the Microstrip Lines (mm)</th>
<th>Equivalent Resistance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M1$</td>
<td>6.8</td>
<td>$R_1 = 0.047$</td>
</tr>
<tr>
<td>$M2$</td>
<td>13.5</td>
<td>$R_2 = 0.094$</td>
</tr>
<tr>
<td>$M3$</td>
<td>2.8</td>
<td>$R_3 = 0.020$</td>
</tr>
<tr>
<td>$M4$</td>
<td>10.2</td>
<td>$R_4 = 0.071$</td>
</tr>
<tr>
<td>$M5$</td>
<td>3.6</td>
<td>$R_5 = 0.025$</td>
</tr>
<tr>
<td>$M6$</td>
<td>7.8</td>
<td>$R_6 = 0.054$</td>
</tr>
</tbody>
</table>

(Total length = 44.7 mm)

### (c)

<table>
<thead>
<tr>
<th></th>
<th>Length of the Microstrip Lines (mm)</th>
<th>Equivalent Resistance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M1$</td>
<td>10.2</td>
<td>$R_1 = 0.071$</td>
</tr>
<tr>
<td>$M2$</td>
<td>10.2</td>
<td>$R_2 = 0.071$</td>
</tr>
<tr>
<td>$M3$</td>
<td>11.6</td>
<td>$R_3 = 0.081$</td>
</tr>
<tr>
<td>$M4$</td>
<td>13.5</td>
<td>$R_4 = 0.094$</td>
</tr>
<tr>
<td>$M5$</td>
<td>39.3</td>
<td>$R_5 = 0.279$</td>
</tr>
<tr>
<td>$M6$</td>
<td>9.5</td>
<td>$R_6 = 0.066$</td>
</tr>
<tr>
<td></td>
<td>Length of the Microstrip Lines (mm)</td>
<td>Equivalent Resistance (Ω)</td>
</tr>
<tr>
<td>-----</td>
<td>------------------------------------</td>
<td>---------------------------</td>
</tr>
<tr>
<td>M1</td>
<td>6.8</td>
<td>$R_1 = 0.047$</td>
</tr>
<tr>
<td>M2</td>
<td>6.8</td>
<td>$R_2 = 0.047$</td>
</tr>
<tr>
<td>M3</td>
<td>1.87</td>
<td>$R_3 = 0.013$</td>
</tr>
<tr>
<td>M4</td>
<td>20.5</td>
<td>$R_4 = 0.143$</td>
</tr>
<tr>
<td>M5</td>
<td>5.5</td>
<td>$R_5 = 0.038$</td>
</tr>
<tr>
<td>M6</td>
<td>11.4</td>
<td>$R_6 = 0.078$</td>
</tr>
</tbody>
</table>

Table D.1 Equivalent resistances of variable microstrip lines using Duroid 5870 substrate ($Z_0 = 50 \, \Omega$)
D.2: Input Impedance (in Ω) of the load harmonic networks using (a) Duroid 5870 substrate and (b) Equivalent circuits with R.
Figure d.3: The obtained S-parameters using Duroid 5870 substrate (a) $S_{11}$, (b) $S_{22}$ and (c) $S_{21}$
Figure D.4 The frequency response of $S_{21}$ using Duroid 5870 for the four topologies circuits using (a) Tlines with $R$ and (b) Mlines