Polynomial Curve Slope Compensation for Peak Current Mode Controlled Power Converters

Haimeng Wu, *Member*, *IEEE,* Volker Pickert, *Member*, *IEEE,* Xu Deng, *Damian Giaouris, Member*, *IEEE,* Wuhua Li, *Member*, *IEEE* and Xiangning He *Fellow*, *IEEE*

***Abstract*— Linear Ramp Slope Compensation (LRC) and Quadratic Slope Compensation (QSC) are commonly implemented in peak current mode controlled DC-DC converters in order to minimize subharmonic and chaotic oscillations. Both compensating schemes rely on the linearized state-space averaged model (LSSA) of the converter. LSSA ignores the impact that switching actions have on the stability of converters. In order to include switching events, the nonlinear analysis method based on Monodromy matrix was introduced to describe a complete-cycle stability. Analyses on analogue controlled DC-DC converters applying this method show that system stability is strongly dependent on the change of the derivative of the slope at the time of switching instant. However, in a mixed-signal controlled system, the digitalization effect contributes differently to system stability. This paper shows a full complete-cycle stability analysis using this nonlinear analysis method, which is applied to a mixed-signal controlled converter. Through this analysis, a generalized equation is derived that reveals for the first time the real boundary stability limits, for LRC and QSC. Furthermore, this generalized equation allows the design of a new compensating scheme which is able to increases system stability. The proposed scheme is called Polynomial Curve Slope Compensation (PCSC) and it is demonstrated that PCSC increases the stable margin by 30% compared to LRC and 20% to QSC. This outcome is proved experimentally by using an interleaved DC-DC converter that is built for this work.**

***Index Terms*— Linear Ramp Slope Compensation (LRC), Quadratic Slope Compensation (QSC), Stability analysis, Subharmonic oscillation, Polynomial Curve Slope Compensation (PCSC), Power converters**

I. INTRODUCTION

Peak current mode (PCM) control is a widely used current mode control (CMC) method for switching power DC-DC converters, offering a number of benefits such as inherent cycle-by-cycle current limiting, good current sharing of paralleled converters, and better transient response compared to voltage mode control [1]. It is well recognized that PCM controlled DC-DC converters suffer from subharmonic oscillations in continuous current mode operation when the duty cycle exceeds 50%. At this point, system stability is lost, resulting in an increase of inductor current and output voltage ripple. Subsequently, converter efficiency goes down [2] and the risk of higher electromagnetic interference (EMI) goes up [3]. In order to eliminate these undesired nonlinear phenomena, PCM with linear ramp compensation (LRC) has been introduced. Today, LRC is the most well-known and the most widely applied technique in industrial applications [4, 5] with a large number of commercial analog controllers available on the market. LRC products are available either with internal or external ramp compensation [6, 7]. In recent years, a few digital LRC controllers using a built-in analog comparator have also emerged on the market [8]. It is expected that more digital controllers with built-in analog comparators will become available on the market. That is because these so called mixed-signal controllers show high reliability, design flexibility and low cost [9, 10].

It is common to derive the magnitude and the grade of the slope of LRC from the state-space averaging method [11]. The disadvantage of state-space averaging is that the analysis ignores information on stability during switching instants (fast timescale) [12] and consequently nonlinear behaviors of power DC-DC converters are not considered in LRC.

In order to compensate for the lag of information, predictive digital LRC methods have been proposed. One predictive LRC method has been presented in [13] in which the inductor current is pre-calculated using knowledge of the inductance value. Inductor current and output voltage are sampled once per cycle and used to predict the desired comparator switch-off threshold. Another digital LRC technique introduces the calculation of the duty cycle of the next switching period by solving the instant at which the sampled current becomes equal to the compensated current reference from the outer voltage loop [14]. A technique of cycle-by-cycle duty ratio computation in real time has also been presented [15] where a time-to-digital converter translates information of the last duty ratio into digital code and then reconstructs the next duty ratio by using a moving average filter. All of these predicted digital LRC methods have in common that they predict future values of the duty cycle by employing a mathematical model. However, predicting future events cannot be regarded as true LRC control since inherent characteristics of real-time cycle-by-cycle current limiting abilities are lost [16].

Another attempt to improve stability is to change the slope from LRC to Quadratic Slope Compensation (QSC). The frequency bandwidth of the converter using QSC is

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H. Wu, V. Pickert, X.Deng and D. Giaouris are with the School of Engineering, Newcastle University, Newcastle upon Tyne, United Kingdom. (corresponding author: Xu Deng, Xu.deng@ncl.ac.uk).

Wuhua Li and Xiangning He are with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China.

independent from input and output voltages and therefore the typical overcompensation used in LRC to guarantee the stability for all load conditions becomes unnecessary in QSC [17]. QSCs with and without adaptive slope gradients have been reported in [18]. However, the underpinning method applied to all LRC and QSC techniques is state-space averaging and consequently exact knowledge on how stability is influenced during switching events is not available.

Due to the lag of fast timescale information, stability analysis methods have been developed to describe these switching events mathematically, in order to determine the complex phenomena of bifurcations, chaos, and subharmonics [19-21]. In addition, studies on the control of power converters from the perspective of switching events have attracted researchers' attentions [22, 23]. To address fast-scale nonlinearities, various stability analysis approaches have been applied on the piecewise linear dynamical systems, switched or hybrid systems, such as discrete map-based modeling [19], Floquet theory [24], Lyapunov-based methods [25], and trajectory sensitivity approach [26]. And different types of feedback and non-feedback control techniques have been suggested applying knowledge of the nonlinearity of the converter system [27-29]. However, all of the proposed techniques are highly dependent on complex mathematical models and therefore cannot be easily implemented in practical circuits.

In order to reflect the use of digital controllers, the complete-cycle analysis must also include digitalized variables. Therefore, the first part of this paper presents for a first time a theoretical complete-cycle analysis that combines continuous time and digitalized time, which is applied to a mixed-signal controlled converter. In this nonlinear analysis method, stability is not only determined by the ON and OFF state of the switches but also by the impact of the switching instants. The knowledge gained from the analysis has provided the derivation of a uniform equation that enables to describe a generalized slope compensation including LRC and QSC. This generalized equation allows the design of a new compensating slope that follows a polynomial function. Thus, the second part of this paper proposes a new slope compensation called Polynomial Curve Slope Compensation (PCSC). PCSC shows superior stability control to both LRC and QSC that increases the stable margin by about 30% compared to LRC and 20% compared to QSC.

The paper is structured as follows. Section II describes the theoretical fundamentals of a complete-cycle method by using the Monodromy matrix. Section III presents the analysis of applying the Monodromy matrix to an interleaved power DC-DC converter, which combines continuous and digital time domains to represent a mixed-signal controller. The section derives a generalized equation that describes the complete-system stability for LRC and QSC and allows the derivation of a new slope compensation method: PCSC. The practical implementation of PCSC using a purpose designed mixed-signal controller is described in Section IV. Section V demonstrates the experimental results of an interleaved boost converter employing LRC, QSC and PCSC for comparison. It is shown that PCSC extends significantly the stable margin of the converter. The final section, Section VI, summarizes the conclusions drawn from the investigation and analysis.

II. NONLINEAR ANALYSIS APPROACH BASED ON MONODROMY MATRIX

A. Methods for the calculation of ramp magnitude in the conventional slope compensation

Subharmonic oscillations associated with peak current control can be explained using a graphical approach as shown in Fig.1(a). To address this issue and regain stability, the approach of slope compensation is commonly applied as shown in Fig.1(b). For stable operation, the following relation must be satisfied:

$$\left|\frac{m_2 - m_{ca}}{m_1 + m_{ca}}\right| < 1 \tag{1}$$

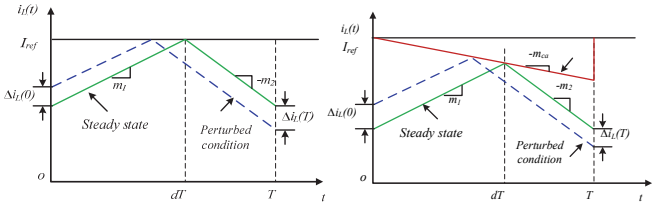
Here, m_1 and m_2 represent the slopes of inductor current when switch is on and off respectively and m_{ca} is the slope of the compensation ramp. Thus, the required slope of this ramp can be obtained as:

$$m_{ca} > \frac{1}{2}(m_2 - m_1) \tag{2}$$

In boost converters, m_2 and m_1 can be calculated by the following expressions:

$$\begin{cases} m_1 = \dfrac{V_{in}}{L} \\ m_2 = \dfrac{V_{out} - V_{in}}{L} \end{cases} \tag{3}$$

where, L is the inductance of the power inductor, V_{in} is the input voltage and V_{out} represent the output voltage of the converter. Another approach to avoid the subharmonic oscillations observed during peak current mode control is by using information of the double pole at half the switching frequency [1, 30]. Both methods have been developed by using linearized state-space averaging (LSSA) models information on input and output voltages and other system parameters that affect the stable margin of a system are not included.



(a) (b)

Fig.1(a) Peak current control without slope compensation
(b) Peak current control with conventional linear ramp slope compensation

B. Principle of nonlinear analysis method by Monodromy matrix

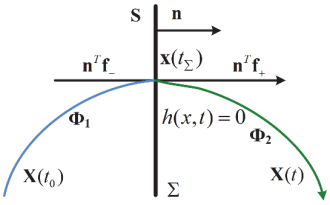


Fig. 2 Diagram of Filippov's method in stability analysis

A Monodromy matrix-based approach has been proven to provide a better insight of the stability. In this approach the

switching events are described analytically by the so called saltation matrix [24, 31]. Combining the saltation matrix with the state transition matrix which presents the information of the switches are in ON or OFF state, a full set of data is obtained that can be used for stability analysis. As the Monodromy matrix-based approach can be utilized to any converter and any controller, it is seen as an enabler tool to develop advanced control methods. The principle of the Monodromy matrix-based method is presented in this section.

For any power converter, the actions of various switches make the system evolve through different linear time-invariant (LTI) subsystems which can be described by a state equation as follows:

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{4}$$

where **A** and **B** are time-dependent matrices which relate to the system parameters, and **u** represents the external input of the system. Equation (4) describes power converters as piecewise smooth and the vector field is discontinuous at the switching instant. In order to describe the switching instant, the Filippov method is applied. The Filippov method uses the state transition matrices before and after each switching event and the saltation matrix that describes the behavior of the solution during the switching [32]. Fig. 2 illustrates the diagram of the Filippov method for stability analysis. The state transition matrices (STM) $\mathbf{\Phi}$ are easily computed based on the exponential matrix (5). The expression of the saltation matrix **S** [32, 33] is shown in (6):

$$\mathbf{\Phi} = e^{\mathbf{A}(t-t_0)} \tag{5}$$

$$\mathbf{S} = \mathbf{I} + \frac{(\mathbf{f}_+ - \mathbf{f}_-)\mathbf{n}^T}{\mathbf{n}^T\mathbf{f}_- + \dfrac{\partial h}{\partial t}} \tag{6}$$

where **I** presents the identity matrix of the same order of state variables, h defines the switching condition which relates to the control algorithm, **n** is the normal vector to the switching surface $\sum$ which separates the regions of state vectors fields, and $\mathbf{f}_-$ and $\mathbf{f}_+$ denote the vector fields before and after the switching instants. **S** is applied to study the discontinuous vector field, by investigating the evolution of vectors crossing the switching surface $\sum$ as shown in Fig.2. The expression of the saltation matrix introduces the influence of switching events for the system, which is ignored when using LSSA. More theoretical description can be found in [2, 32, 33].

III. Monodromy Matrix Applied to a Mixed-Signal (Analogue/Digital) Controlled Interleaved DC-DC Converter

In an interleaved DC-DC converter, there are four subsystems depending on the state of the switches and for each subsystem, a STM can be derived as $\mathbf{\Phi_1}$~$\mathbf{\Phi_4}$. The control diagram and key operational waveforms of interleaved boost converter with slope compensation are illustrated in Fig.3(a) and Fig.3(b) respectively. The output voltage v_c and inductor currents i_{L1} and i_{L2} are chosen as state vectors. The corresponding phase portrait orbit of the output voltage and inductor currents is shown in Fig.3(c). It demonstrates that the state vectors are not smooth in the switching instants and can therefore be described with the help of the saltation matrices $\mathbf{S_{12}}$~$\mathbf{S_{41}}$. Fig.3(d) presents the derivation of the Monodromy matrix **M** which contains the comprehensive information of the system including the slope compensation. The stability of a periodic solution is subject to the eigenvalues of this matrix. If all the eigenvalues calculated are located in the unit cycle of the complex plane, the system can be confirmed as stable; otherwise, the system is considered as unstable exhibiting various bifurcations determined by the movement trajectory of crossing the unit circle. Assuming that there is an initial perturbation $\Delta\mathbf{X}(t_0)$, it evolves in one complete period through four different STM and four saltation matrices S in sequence. For a given system at t_0, the system can be proved to be stable when this perturbation tends to become zero when $t\to\infty$. For a periodic orbit with a period of T, the following equation can be written [32]:

$$\Delta\mathbf{X}(t_0+T) = \mathbf{M}\Delta\mathbf{X}(t_0) \tag{7}$$

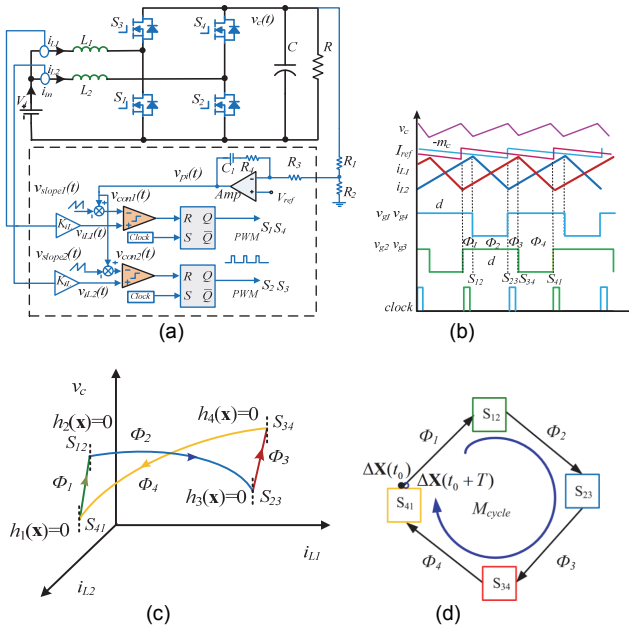


Fig.3 Interleaved boost converter with slope compensation: (a) topology and control diagram (b) key operational waveforms (c) portrait curve of input voltage and inductor currents (d) derivation of the Monodromy matrix

A. Derivation of the Monodromy matrix applied to a mixed-signal controller

Previous literature studies only the Monodromy matrix on the continuous-time analysis [24, 31]. Due to expected growth of mixed-signal controllers in the future, studies must extend digital and analog signals within the Monodromy matrix which is here reported for the first time. According to equation (6), the normal vector **n** and the term of $\partial h/\partial t$ are the key to derive the saltation matrix S.

The interleaved converter has four system states and each applies at different subintervals starting from time t=0 and ending at t=T. Thus the following right-hand side state equations and relevant matrices can be obtained:

$[0,(d-0.5)T]$	$[(d-0.5)T,0.5T]$	$[0.5T,dT]$	$[dT,T]$
$f_1=\begin{bmatrix}-\frac{v_c}{RC}\\ \frac{V_i}{L_1}\\ \frac{V_i}{L_2}\end{bmatrix}$ (8)	$f_2=\begin{bmatrix}\frac{i_{L1}R-v_c}{RC}\\ \frac{V_i-v_c}{L_1}\\ \frac{V_i}{L_2}\end{bmatrix}$ (9)	$f_3=\begin{bmatrix}-\frac{v_c}{RC}\\ \frac{V_i}{L_1}\\ \frac{V_i}{L_2}\end{bmatrix}$ (10)	$f_4=\begin{bmatrix}\frac{i_{L2}R-v_c}{RC}\\ \frac{V_i}{L_1}\\ \frac{V_i-v_c}{L_2}\end{bmatrix}$ (11)

$$\mathbf{A}_1=\begin{bmatrix}-\frac{1}{RC} & 0 & 0\\ 0 & 0 & 0\\ 0 & 0 & 0\end{bmatrix} \quad (12) \qquad \mathbf{A}_2=\begin{bmatrix}-\frac{1}{RC} & \frac{1}{C} & 0\\ -\frac{1}{L_1} & 0 & 0\\ 0 & 0 & 0\end{bmatrix} \quad (13)$$

$$\mathbf{A}_3=\begin{bmatrix}-\frac{1}{RC} & 0 & 0\\ 0 & 0 & 0\\ 0 & 0 & 0\end{bmatrix} \quad (14) \qquad \mathbf{A}_4=\begin{bmatrix}-\frac{1}{RC} & 0 & \frac{1}{C}\\ 0 & 0 & 0\\ -\frac{1}{L_2} & 0 & 0\end{bmatrix} \quad (15)$$

$$\mathbf{B}_1=\mathbf{B}_2=\mathbf{B}_3=\mathbf{B}_4=\begin{bmatrix}0 & 0 & 0\\ 0 & 0 & \frac{1}{L_1}\\ 0 & 0 & \frac{1}{L_2}\end{bmatrix} \quad (16) \qquad \mathbf{u}=\begin{bmatrix}0\\ 0\\ V_i\end{bmatrix} \quad (17)$$

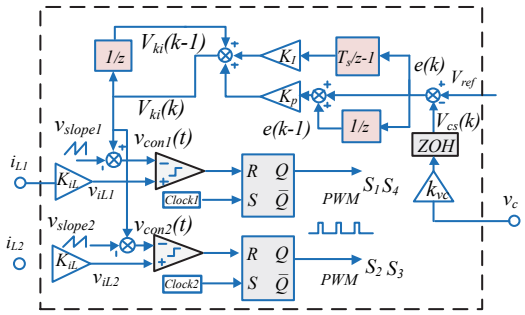


Fig.4 Mixed-signal controller for interleaved DC-DC converter

In digitalized control, the effect of sampling and zero-order hold (ZOH) makes fundamental changes in the derivation of the saltation matrix. It is common to digitalize the slower outer loop whereas the faster inner loop is kept in the time domain in order to avoid the implementation of high-speed analogue-to-digital converter (ADC) [34]. In Fig.4, the output voltage v_c is therefore sampled and one constant value $V_{cs}(k)$ is send to the controller for one switching period. The relationship between the variable v_c and sampled value $V_{cs}(k)$ is:

$$v_c = V_{cs}(k)\cdot e^{At} = V_{cs}(k)\cdot e^{\frac{t}{RC}} \qquad t\in[0,(d-0.5)T] \quad (18)$$

An output of the digital PI controller $V_{ki}(k)$ controls the error e(k) that occurs between $V_{cs}(k)$ and V_{ref} , and $V_{ki}(k)$ can be represented as:

$$V_{ki}(k)=V_{ki}(k\text{-}1)+\Delta V_{ki}(k)=V_{ki}(k-1)+(K_p+K_IT_s)e(k)-K_pe(k-1) \quad (19)$$

and

$$e(k)=(V_{ref}-K_{vc}V_{cs}(k)) \quad (20)$$

where K_I and K_p represent the gains of the PI controller; K_{vc} is the gain from the sampled output voltage v_c; T_s is the switching period, m_c represents the slope of the compensation ramp, $V_{ki}(k\text{-}1)$ is the output of the integral from the last period and $e(k\text{-}1)$ is the last error signal between sampled output voltage and reference V_{ref}. Thus the control signal $v_{con}(t)$ can be obtained as follows:

$$v_{con}(t)=V_{ki}(k)+m_ct \quad (21)$$

Assuming that a_c represents the amplitude of this compensation ramp at the end of each switching period, the following expression must be obtained:

$$a_c=|m_cT_s| \quad (22)$$

In the peak current control algorithm, the switches of the DC-DC converter will turn off when the generated control signal $v_{con}(t)$ equals the values of the inductor current i_{L1} and i_{L2} which is illustrated in Fig.3. Therefore, when the duty cycle d is bigger than 0.5, the switching functions can be defined as $h(x,t,k)$, which are shown as follows:

$$h_{12}(x,t,k)=(K_p+K_IT_s)(V_{ref}-K_{vc}V_{cs}(k))+V_{ki}(k-1)$$
$$-K_pe(k-1)+m_ct-K_{iL}i_{L2} \quad (23)$$

$$h_{34}(x,t,k)=(K_p+K_IT_s)(V_{ref}-K_{vc}V_{cs}(k))+V_{ki}(k-1)$$
$$-K_pe(k-1)+m_c(t-\frac{T_s}{2})-K_{iL}i_{L1} \quad (24)$$

with K_{iL} is the gain of the analogue inductor current. The derivative of the switching condition can be obtained as:

$$\frac{\partial h_{34}}{\partial t}=\frac{\partial h_{12}}{\partial t}=m_c=-\frac{a_c}{T_s}=s_a \quad (25)$$

From equation (18), $V_{cs}(k)$ can be represented by v_c at the time of switching instant, thus

$$V_{cs}(k)=v_c\cdot e^{\frac{t}{RC}}\Big|_{t=t_d=(d-0.5)\,\mathrm{T}} \quad (26)$$

Its normal vector to the switching manifold can be given by

$$\mathbf{n_{12}}=\begin{bmatrix}\partial h_{12}/\partial v_c\\ \partial h_{12}/\partial i_{L1}\\ \partial h_{12}/\partial i_{L2}\end{bmatrix}=\begin{bmatrix}s_c\\ -K_{iL}\\ 0\end{bmatrix} \quad (27)$$

$$\mathbf{n_{34}}=\begin{bmatrix}\partial h_{34}/\partial v_c\\ \partial h_{34}/\partial i_{L1}\\ \partial h_{34}/\partial i_{L2}\end{bmatrix}=\begin{bmatrix}s_c\\ 0\\ -K_{iL}\end{bmatrix} \quad (28)$$

where

$$s_c=-(K_p+K_iT_s)K_{vc}e^{\frac{t_d}{RC}} \quad (29)$$

As the value of t_d is relatively small to the value of RC, the term $e^{\frac{t_d}{RC}}$ becomes 1, thus, s_c can be simplified to:

$$s_c=-(K_p+K_iT_s)K_{vc} \quad (30)$$

Therefore, from the equation (6), the saltation matrices $\mathbf{S_{12}}$ and $\mathbf{S_{34}}$ can be obtained as:

$$\mathbf{S}_{12}=\begin{bmatrix} 1+\dfrac{s_c i_{L1}}{C(s_{pa}+s_a)} & -\dfrac{K_{iL} i_{L1}}{C(s_{pa}+s_a)} & 0 \\ -\dfrac{s_c v_c}{L_1(s_{pa}+s_a)} & 1+\dfrac{v_c K_{iL}}{L_1(s_{pa}+s_a)} & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{31}$$

$$\mathbf{S}_{34}=\begin{bmatrix} 1+\dfrac{s_c i_{L2}}{C(s_{pb}+s_a)} & 0 & -\dfrac{K_{iL} i_{L2}}{C(s_{pb}+s_a)} \\ 0 & 1 & 0 \\ -\dfrac{s_c v_c}{L_2(s_{pb}+s_a)} & 0 & 1+\dfrac{v_c K_{iL}}{L_2(s_{pb}+s_a)} \end{bmatrix} \tag{32}$$

where

$$s_{pa}=\mathbf{n}_{12}^T f_1=\begin{bmatrix} s_c & 0 & -K_{iL} \end{bmatrix}\begin{bmatrix} -\dfrac{v_c}{RC} \\ \dfrac{V_i}{L_1} \\ \dfrac{V_i}{L_2} \end{bmatrix}$$

$$=-\frac{s_c v_c}{RC}-\frac{K_{iL}V_i}{L_2}=\frac{(K_p+K_i T_s)K_{vc}V_{cs}(k)}{RC}-\frac{K_{iL}V_i}{L_2} \tag{33}$$

$$s_{pb}=\mathbf{n}_{34}^T f_3=\begin{bmatrix} s_c & -K_{iL} & 0 \end{bmatrix}\begin{bmatrix} -\dfrac{v_c}{RC} \\ \dfrac{V_i}{L_1} \\ \dfrac{V_i}{L_2} \end{bmatrix}$$

$$=-\frac{s_c v_c}{RC}-\frac{K_{iL}V_i}{L_1}=\frac{(K_p+K_i T_s)K_{vc}V_{cs}(k)}{RC}-\frac{K_{iL}V_i}{L_1} \tag{34}$$

The pulse of clock signal and the rising edge of the ramp occur at the same time, since it is a forced switching action and the value of ∂t is small enough to make the result of $\partial h/\partial t$ to be infinity. In other words, this switching action makes the saltation matrixes $\mathbf{S_{23}}$ and $\mathbf{S_{41}}$ to be the identity matrix.

$$\mathbf{S}_{23}=\mathbf{S}_{41}=\mathbf{I} \tag{35}$$

For the interleaved control algorithm, the time of each subinterval can be represented in terms of d and T. The state transition matrices are given by the matrix exponential, hence

$$\begin{cases} \mathbf{\Phi}_1=e^{\mathbf{A}_1(d-0.5)\mathrm{T}} \\ \mathbf{\Phi}_2=e^{\mathbf{A}_2(1-d)\mathrm{T}} \\ \mathbf{\Phi}_3=e^{\mathbf{A}_3(d-0.5)\mathrm{T}} \\ \mathbf{\Phi}_4=e^{\mathbf{A}_4(1-d)\mathrm{T}} \end{cases} \tag{36}$$

Thus, the Monodromy matrix $\mathbf{M}$ can be calculated by the following expression:

$$\mathbf{M}=\mathbf{\Phi}_{cycle}=\mathbf{\Phi}_1\times\mathbf{S}_{12}\times\mathbf{\Phi}_2\times\mathbf{S}_{23}\times\mathbf{\Phi}_3\times\mathbf{S}_{34}\times\mathbf{\Phi}_4\times\mathbf{S}_{41} \tag{37}$$

The stability of the system can be predicted by investigating the movement of eigenvalues of this matrix at different given parameters and input conditions.

B. Investigation on Quadratic Slope Compensation (QSC) by Monodromy matrix

The principle waveforms of LRC and QSC are illustrated in Fig.5. QSC has been introduced to achieve higher stable operation compared to LRC. Reference [35] presents the stability analysis of this compensation using classical averaging modelling method and concludes that the improvement of system stability is related to the increased amount of the equivalent slope compared with conventional compensation. In Fig. 5, a_c and a_m represent the amplitude of slope compensation for LRC and QSC respectively and their values are related to the compensation effect that determines stable operational regions. Using QSC the switching condition can be written to

$$h(x,t,k)=(K_p+K_I T_s)(V_{ref}-K_{vc}V_{cs}(k))+V_{ki}(k-1)$$
$$-K_p e(k-1)-a_m(t/T_s)^2-K_{iL}i_L \tag{38}$$

and its rate becomes

$$\frac{\partial h}{\partial t}=-2a_m d/T_s \tag{39}$$

Thus, the term of $\partial h/\partial t$ is not only related to the amplitude a_m of the ramp, but also relates to the duty cycle d. According to the outcomes of the stability analysis method, the bigger value of term $\partial h/\partial t$ makes the eigenvalues of the Monodromy matrix moving towards the center of the unit cycle which results in an extended stable margin. Thus, equation (39) shows new knowledge in that if d is above 0.5, the absolute value of this term is bigger than its conventional linear counterpart assuming identical amplitudes of a_m and a_c. With the help of (39) two new statements can be made:

Statement 1: For d>0.5 and a_m=a_c QSC offers better stability control compared to LRC

Statement 2: For d<0.5 and a_m=a_c LRC offers better stability control compared to QSC

In principle, Statement 2 can be regarded as less relevant as no slope compensation is required for PCM controlled converter operating at d<0.5. However, many commercial controllers apply LRC with a fixed slope regardless the duty cycle d. Both findings on the stability limitations of LRC and QSC are new knowledge and are reported here for the first time. Experimental results will be presented in detail to verify these statements.

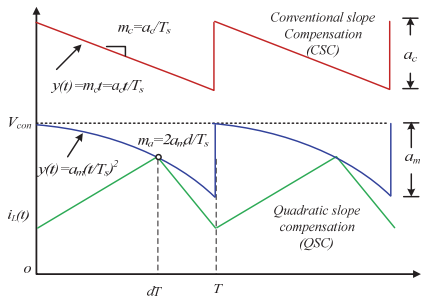


Fig.5 Principle waveform of QSC and LRC

C. Proposed Polynomial Curve Slope Compensation (PCSC) control

When applying the nonlinear analysis method using the Monodromy matrix, it can be shown that the system stability is strongly relevant with the change of the derivative of the ramp at the time of switching instant and not only to the absolute magnitude value of the slope instant. However, when and how to change the derivative of the slope to realize the best compensation performance is still challenging that have not been studied in the previous research. Thanks to the knowledge gained from the analytical work described above, it allows now to develop a generalized slope shape that achieves an optimized compensation. As system stability is a function of the derivative at the switching instant, a feasible concept is to increase the control freedom by introducing a new control variable. If the order of the generated curve is able to be varied against the time t, the information of order can be introduced in the saltation matrix that effectively affects the switching instance. This concept leads to a polynomial shape thus the new scheme is named Polynomial Curve Slope Compensation (PCSC) where the compensation slope is realized by producing a curve of an nth powered polynomial over time t. By applying this approach, the switching condition can be given as follows:

$$h(x,t,k)=(K_p+K_IT_s)(V_{ref}-K_{vc}V_c)+ V_{ki}(k-1)-a_m(t/T_s)^n-K_{iL}i_L \quad (40)$$

and its rate is:

$$\frac{\partial h}{\partial t}=-na_m t^{n-1}/T_s^n=-na_m d^{n-1}/T_s \quad (41)$$

The term $\partial h/\partial t$ relates to the duty cycle d, amplitude a_m and the number of order n (n=1,2,3,4…) which is different from the previous expressions that relates only to a_c (LRC) or to a_m and duty cycle d (QSC). Equation (41) can be termed as general equation as it describes (26) for n=1 (LRC) (replacing a_c *with* a_m) and it describes (39) for n=2 (QSC). Equation (41) can be nominalized against (25):

$$f(n,d)=[-na_m d^{n-1}/T_s]/(-a_m/T_s)=nd^{n-1} \quad (42)$$

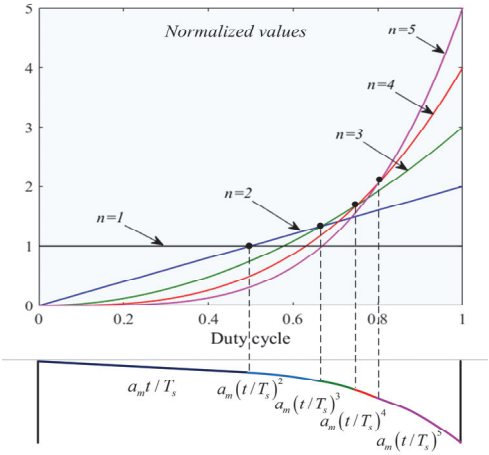


Fig.6 Proposed Polynomial Curve Slope Compensation (PCSC) scheme

The normalized curves for different duty cycle d and order n are presented in Fig.6. This figure allows to find the optimized order n at different duty cycles. For example, the figure shows that the curve for n=1 is above all others when d<0.5. This means that up to this point LRC produces the biggest value of the term $\partial h/\partial t$, enabling the largest stable operational region. In the subinterval of [1/2, 2/3] the curve of QSC demonstrates the best stability control. Similarly, by calculating the positions of the cross points, the best curves can be obtained when n equals 3, 4 and 5 in the subintervals of [2/3, 3/4], [3/4, 4/5] and [4/5, 1] respectively. According to this result, a PCSC control scheme for optimized stability control can be constructed as shown in Fig.6, which theoretically has the biggest stable operation margin at the whole range of the duty cycles. Like LRC or QSC, PCSC does not rely on a high fidelity model and therefore does not require long calculation times at each switching period. This is an advantage for DC/DC converters operating at high switching frequencies where processing time is crucial. The challenge with PCSC is the generation of the particular polynomial shape, which can only be achieved when using analogue-to-digital converter (DAC) with high resolutions as shown in the following Section IV.

IV. Experimental Setup

A. Developed mixed-signal controller

For a fully digital peak current controller, the main challenge is that the instantaneous waveform of the inductor current must be digitalized by a high-speed ADC converter. Given the rapid changes in the inductor current, ADCs with high sampling and conversion rates and high-performance processors are required.

To avoid the need to sample the inductor current constantly during the switching period, a feasible alternative to the fully digital peak current solution is to use mixed-signal microcontrollers where the voltage controller utilizes digital implementation and the current loop remains in the analogue domain. Thereby the discrete threshold value is converted into an analog voltage by an internal DAC, to represent the current threshold level for the on-chip comparator. However, all commercially available mixed-signal controllers have the limitations as follows:

- Only able to produce the common saw-tooth type compensation using some specialized peripheral circuit.
- A small number of slope compensation amplitude can be set as only a few bits (4 bits) of relevant registers are used for the configuration
- Up to 10 bits resolution DAC which is not able to generate sophisticated waveforms.

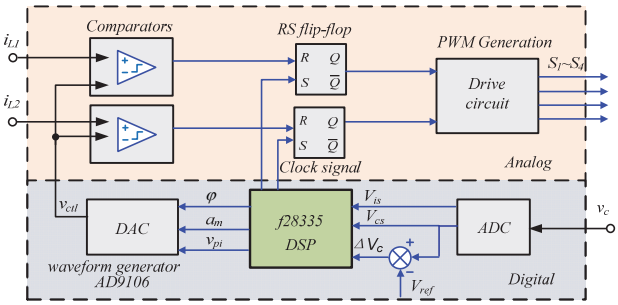


Fig.7 Diagram of the proposed mixed-signal controller

Therefore a new mixed-sigal controller was developed for this project. An external high-performance 12-bit DAC AD9106 is employed with a common DSP processor, which is to generate various types of the compensation slopes with high-resolution waveforms. Fig.7 shows the diagram of this mixed-signal controller. The DSP processor is used as a master unit to achieve the functions of voltage signal sampling, digital proportional-integral (DPI) calculating and sending commands to the independent on-chip waveform generator AD9106 to produce the control signals. This AD9106 is integrated with a on-chip pattern memory, which can be used to generate complex waveforms. Its internal static random-access memory (SRAM) provides the function of direct waveform generation based on stored data, with flexible gain and offset adjustments using 7-bit registers. Configuration can be achieved via SPI communication with the master processor.

B. *Interleaved DC/DC converter*

TABLE I
SPECIFICATIONS OF SYSTEM PARAMETERS

Parameters	Value	Parameters	Value
Input voltage (V)	5~18	Frequency (kHz)	50
Output voltage (V)	24	K_{iL}	1/8.5
Power rating (W)	60	K_{p1}	0.5
Inductance (μH)	75	K_{i1}	2000
Output capacitance (μF)	40	$a_c(a_m)$	0.05-0.2
K_{vc}	1/120		

An interleaved boost converter is built to verify the effectiveness of the theoretical analysis and the proposed control scheme. Table 1 shows the specification of this converter. It can be seen that the converter is designed to operate at wide range of the input voltage which enables to validate the different compensation techniques at various duty cycles.

All of the components were assembled into a power case and a photograph of the full prototype is given in Fig.8.

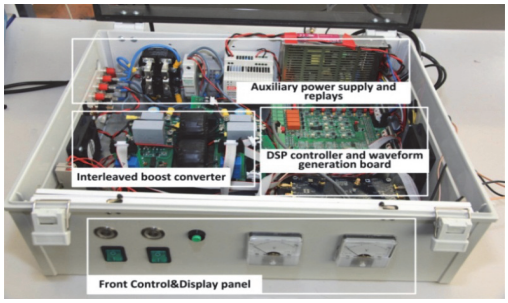
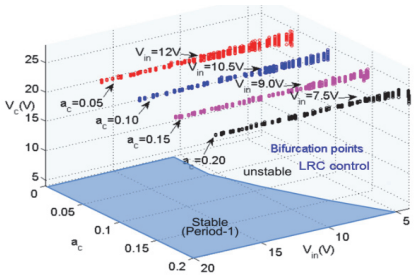


Fig.8 Photograph of prototype

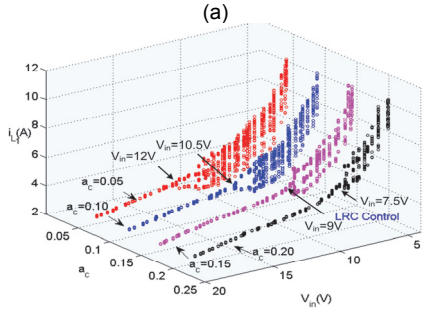
V. EXPERIMENTAL SETUP

A. *Linear Ramp Compensation (LRC)*

Fig.9 shows the experimental results from the power converter using LRC. The experimental graphs were generated based on the measured and stored data using Matlab. Fig.9(a) shows the output voltage v_c as a function of input voltage variation V_{in} and ramp variation a_c. The arrows marked V_{in} for 7.5V, 9V, 10.5V and 12V indicate the start of bifurcation. These points have been reflected onto the XY plane to show the area of stable operation. Fig 9(b) shows the inductor current i_{L1} as function of input voltage variation V_{in} and ramp variation a_c. This figure show more clearly the start of bifurcation.



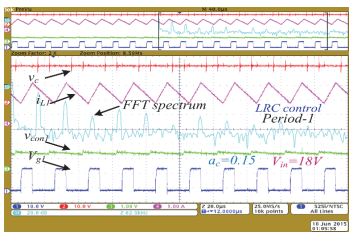
(a)



(b)

Fig.9 Experimental bifurcation diagram of output voltage v_c (a) and inductor current i_{L1} (b) at different input voltages vin and ac using LRC control

Fig.10 shows the operational waveforms of interleaved boost converter at different input voltages when a_c equals 0.15. When the input voltage V_{in} is set at 18V, the waveforms indicate that the system is in the stable operation of period-1 as illustrated in Fig.10 (a). If the input voltage is reduced to V_{in}=8V which is less than the bifurcation point, the converter exhibits the behavior of period doubling bifurcation in the operation of period-2, where the frequency of the inductor current becomes half of the switching frequency as shown in Fig.10(b). Thus the corresponding FFT spectrum curve indicates that the fundamental frequency of the inductor current to be 25kHz. Fig.10(c) presents the operational waveforms of the converter when V_{in}=6V, the PWM of drive signals become random and the continuous wide band frequency FFT spectrum curve indicates that the converter is operating in the chaotic state. The corresponding calculated locus of eigenvalues shown in Fig.10(d) provides the information of the margin of stable operation at different given parameters which can be used to indicate the system stability to facilitate the practical circuit design.



(a)

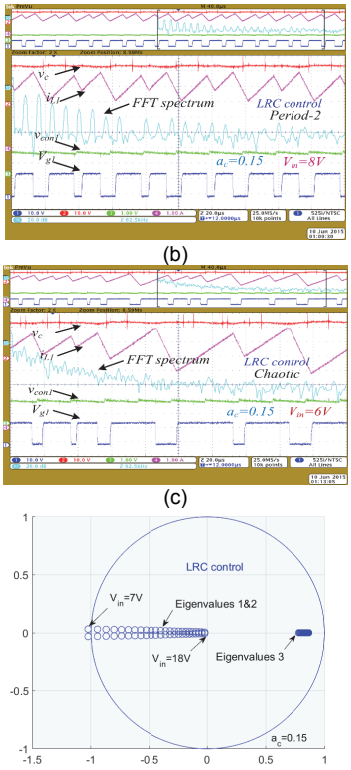


Fig.10 Key operational waveforms at different input voltages using LRC control (a_c =0.15): (a) V_{in}=18V (b) V_{in}=8V (c) V_{in}=6V (d) Locus of eigenvalues using LRC control (a_c =0.15)

B. *Quadratic slope compensation (QSC)*

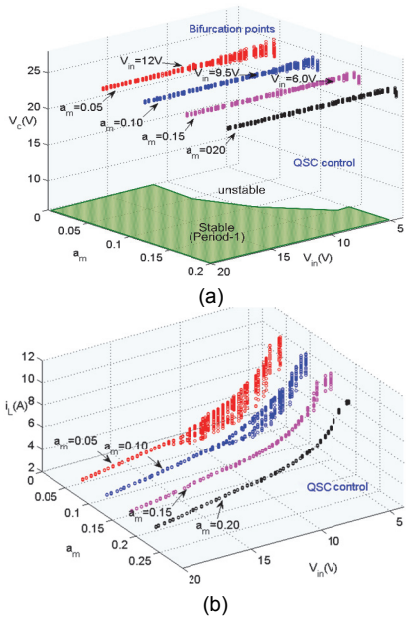


Fig.11 Experimental bifurcation diagram of output voltage v_c (a) and inductor current i_{L1} (b) at different input voltages vin and am using QSC control

As discussed in the Section II, QSC is able to extend the range of stable operation compared to LRC when using an identical amplitude of ramp and a duty cycle larger of 0.5. Fig.11 shows the bifurcation diagram of inductor current and output voltage at different input voltages and a_m when employing QSC control scheme. By observing the positions of the bifurcation points, the stable operational range is enlarged. For example, the bifurcation point changes from V_{in}=10.5V (LRC) to V_{in}=9.5V (QSC) at a_m=0.10. At a_m=0.15, the bifurcation point reduces from 9V to 6V and if a_m is further increased to 0.20, no bifurcation is observed and the converter becomes stable over the whole input voltage range from V_{in}=6V to V_{in}=18V.

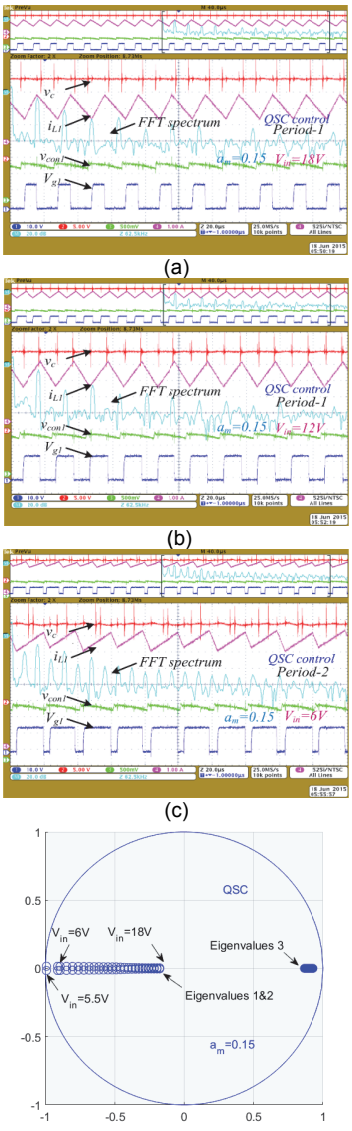


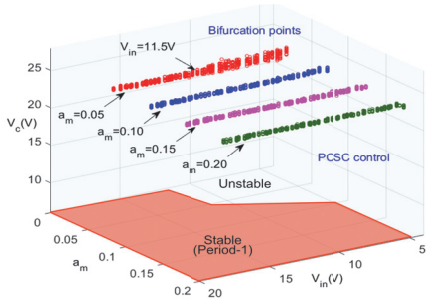
Fig.12 Key operational waveforms at different input voltages by using QSC control (a_m =0.15): (a) V_{in}=18V; (b) V_{in}=12V; (c) V_{in}=6V (d) Locus of eigenvalues using QSC control

Fig.12 shows the operational waveforms when the input voltage equals to 18V, 12V, and 6V respectively. The system is operated in period-1 both at 12V and 18V as illustrated in Fig.12(a) and Fig.12(b). When the input voltage is reduced to 6V, the system exhibits the double-period (period-2) phenomena as depicted by the operational waveforms and the FFT spectrum (Fig. 12(c)). The locus of eigenvalues provides an insight of the stability and is a numerical result. LRC control will lose stability when the input voltage is less than 7V

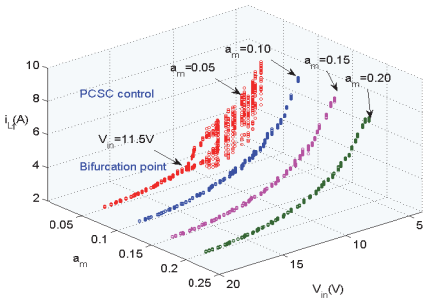
(Fig.10(d)) where the locus of QSC (Fig.12(d)) shows stability loss at approximately V_{in}=5.5V which is below the measured voltage of V_{in}=6.0V. The small difference between the numerical value of 5.5V and the measured value of 6.0V lies with parameter and measurement sensitivities which seems to be more influential at QSC than LRC.

C. *Proposed Polynomial Curve Slope Compensation (PCSC) control*

Fig.13 shows the bifurcation diagram of the converter when employing PCSC, where the bifurcation only takes place when a_m is 0.05. Compared with LRC and QSC, this bifurcation point varies from 12V to 11.5V. In addition, when a_m equals 0.10, 0.15 and 0.20 respectively, the converter shows period-1 stable operation at the entire input range. For instance, for a_m=0.15 the converter exhibits bifurcation for LRC and QSC as shown in Fig.9 and Fig.11 respectively. In contrast, there is no bifurcation employing PCSC and the key operational waveforms show the converter is stably operating at 18V, 12V and 6V input voltage as illustrated in Fig.14. The calculated eigenvalues of the system matrix clearly show the stable margin of the system at different given input voltages in Fig.14 (d), and it is evident that the interleaved power DC-DC converter employing PSCS has a bigger stable margin compared to LRC and QSC.

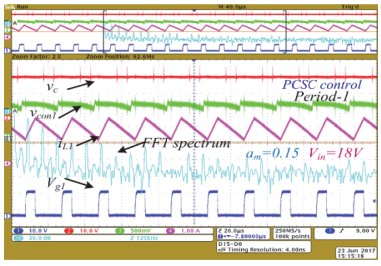


(a)

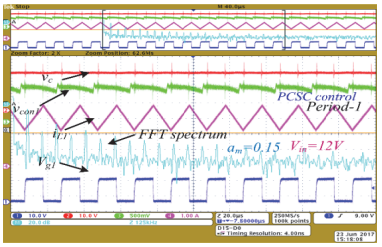


(b)

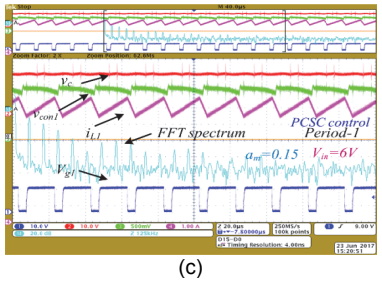
Fig.13 Experimental bifurcation diagram of output voltage v_c (a) and inductor current i_{L1} (b) at different input voltages v_{in} and a_m using PCSC control



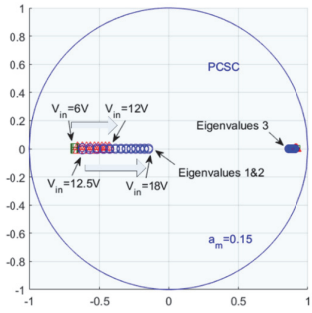
(a)



(b)

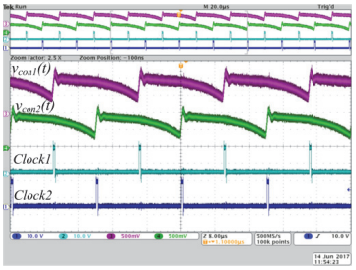


(c)

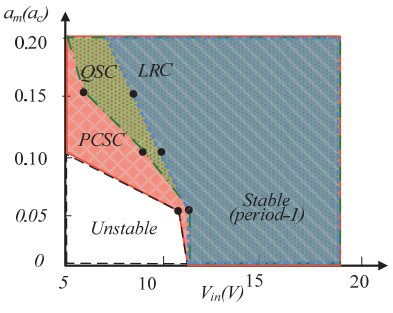


(d)

Fig.14 Key operational waveforms at different input voltages by using PCSC control (a_m =0.15): (a) V_{in}=18V; (b) V_{in}=12V; (c) V_{in}=6V (d) Locus of eigenvalues using PCSC control (a_m =0.15)



(a)



(b)

Fig.15 (a) Generated polynomial curve slope compensation (PCSC) and corresponding clock signals for the interleaved DC/DC converter (b) Comparison of the stable operational region employing LRC, QSC and PCSC

Fig.15(a) illustrates the generated PCSC curve including the corresponding clock signals in the controller. Fig.15(b) presents

the comparison of the stable operational region of all three control methods employing the three different compensation settings. LRC only provides stable operation in the blue area. The olive area shows the extended stable area produced by QSC and the red area presents the even further extended stable area generated by PCSC compared to QSC. Based on the areas, one can approximate that the extended area generated by QSC (olive) is 10% of the area generated by LRC (blue) and that the even further extended area by PCSC is 20% of the area produced by QSC. Thus, PSCS extends the stable region by approximately 30% compared to LRC and 20% compared to QSC.

VI. Conclusion

This paper uses a new investigation method to determine the effectiveness of mixed-signal controlled compensation circuits by applying a nonlinear stability analysis based on the Monodromy matrix. With this method it is possible to investigate the switching instance behavior which leads to a full set of information on system stability at various compensation parameters. A comparative study on LRC and QSC control schemes reveals why QSC has better compensation performances for duty cycles bigger 0.5 and why LRC has better compensation performances for duty cycles less than 0.5. Knowledge gained from this investigation has led to the development of a new compensation method called Polynomial Curve Slope Compensation (PCSC). Compared to other compensations techniques, PCSC provides best compensation effect with an extended stable operational region to boost the performance of converter operation, avoiding period-doubling bifurcation and chaos. Like LRC and QSC, PSCS is an universal method thus it is independent from power levels, switching frequencies and applications. Experimental results validate the effectiveness of this method on an interleaved boost converter utilizing a new mixed-signal controller.

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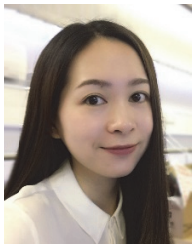
Haimeng Wu (M'10) was born in Zhejiang, China, in 1986. He received the B.Sc. degree from Chongqing University, Chongqing, China, in 2008. He was nominated as the postgraduate exempted from the national postgraduate entrance examination to Zhejiang University and then he got the M.Sc. degree from College of Electrical Engineering, Zhejiang University, Hangzhou, China, in 2011. He received the grants from Engineering and Physical Science Council (EPSRC) for his further education in UK. In 2016, he received his Ph.D. degree at the School of Engineering, Newcastle University, United Kingdom.

He joined in Electrical Power Research Group at Newcastle University as a Postdoctoral Researcher since 2015. His current research interests include power electronics for electric vehicles and advanced nonlinear control.

Volker Pickert (M'04) studied Electrical and Electronic Engineering at the Rheinisch-Westfaelische Technische Hochschule (RWTH), Aachen, Germany and Cambridge University, UK. He received his Dipl.-Ing. degree from RWTH in 1994 and the Ph.D. degree from Newcastle University, Newcastle upon Tyne, U.K. in 1997.

From 1998 to 1999, he was Application Engineer with Semikron GmbH, Nuremberg, Germany and from 1999 to 2003 he was Group Leader at Volkswagen AG, Wolfsburg, Germany, responsible for the development of electric drives for electric vehicles. In 2003 he was appointed as a Senior Lecturer in the Electrical Power Research Group at Newcastle University and in 2011 he became Full Professor of Power Electronics. In 2012 he has become the Head of the Electrical Power Research Group. He has published more than 120 book chapters, journal and conference papers in the area of power electronics and electric drives. His current research interests includes power electronics for automotive applications, thermal management, health monitoring techniques and advanced nonlinear control.

Prof. Pickert is the recipient of the IMarEST Denny Medal for the best article in the Journal of Marine Engineering in 2011. He was chairman of the biannual international IET conference on Power Electronics, Machines and Drives in 2010 in Brighton and he is the active Editor-in-Chief of the IET Power Electronics journal.



Xu Deng received the B.Eng. and M.Eng. degrees in Electrical Engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2010 and 2013, respectively. She received the PhD degree in Electrical Engineering from Newcastle University, Newcastle upon Tyne, U.K, in 2017. She is currently a Research Associate of Electrical Power Research Group in the School of Engineering, Newcastle University, Newcastle upon Tyne, U.K. Her main researches are integrated drives and advanced control methods for power electronics and electric machines.

Damian Giaouris – has received his PhD & MSc in the area of Control of Electrical Systems from Newcastle University (UK), Postgraduate Certificate & BSc in Mathematics from Open University (UK), and BEng in Automation Engineering from Technological Educational Institute of Thessaloniki (Greece).

He was a Lecturer in Control Systems at Newcastle University since 2004, before moving to the Centre for Research and Technology Hellas (Greece) in 2011. Since September 2015 he is a Senior Lecturer in Control of Electrical Systems at Newcastle University. His research interests include control of power converters, power systems, smart grids, electric vehicles, and nonlinear dynamics of electrical systems. He has more than 115 publications (with more than 1400 citations), currently he is an associate editor of IET Power Electronics and he has been a Guest Associate Editor of IEEE Journal on Emerging and Selected Topics in Circuits and Systems.

Wuhua Li (M'09) received the B.Sc. and Ph.D. degree in applied power electronics and electrical engineering from Zhejiang University, Hangzhou, China, in 2002 and 2008, respectively. From 2004 to 2005, he was a Research Intern, and from 2007 to 2008, a Research Assistant in GE Global Research Center, Shanghai, China. From 2008 to 2010, he joined the College of Electrical Engineering, Zhejiang University as a Post Doctor. In 2010, he was promoted as an Associate Professor. Since 2013, he has been a Full Professor at Zhejiang University, Hangzhou, China. From 2010 to 2011, he was a Ryerson University Postdoctoral Fellow in the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. He has published more than 100 peer-reviewed technical papers and holds more than 30 issued/pending patents. His research interests include high power devices, advanced power converters, and operation optimization for renewable energy based power systems.

Dr. Li, due to his excellent teaching and research contributions, received the 2011 TOP TEN Excellent Young Staff Award and the 2012 Distinguished Young Scholar from Zhejiang University, the 2012 Outstanding Young Researcher Award from Zhejiang Province, the 2012 Delta Young Scholar from Delta Environmental & Educational Foundation, and the 2012 National Outstanding Young Scholar. He received four Scientific and Technological Achievements Awards from Zhejiang Provincial Government and the State Educational Ministry of China in 2009, 2011, and 2014, respectively.

Xiangning He (M'95–SM'96–F'10) received the B.Sc. and M.Sc. degrees from Nanjing University of Aeronautical and Astronautical, Nanjing, China, in 1982 and 1985, respectively, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 1989, all in applied power electronics and electrical engineering.

From 1985 to 1986, he was an Assistant Engineer at the 608 Institute of Aeronautical Industrial General Company, Zhuzhou, China. From 1989 to 1991, he was a Lecturer at Zhejiang University. In 1991, he obtained a Fellowship from the Royal Society of U.K., and conducted research in the Department of Computing and Electrical Engineering, Heriot-Watt University, Edinburgh, U.K., as a Post-Doctoral Research Fellow for two years. In 1994, he joined Zhejiang University as an Associate Professor. Since 1996, he has been a Full Professor in the College of Electrical Engineering, Zhejiang University. He was the Director of the Power Electronics Research Institute and the Head of the Department of Applied Electronics, and he is currently the Vice Dean of the College of Electrical Engineering, Zhejiang University. His research interests include power electronics and their industrial applications. He is the author or co-author of more than 280 papers and one book Theory and Applications of Multi-level Converters (Beijing, China: China Machine Press, 2006). He holds 22 patents.