Thermal and Mechanical Analysis of Clamping Area on the Performance of Press Pack IGBT in Series-connection Stack Application

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***Abstract*—Press Pack Insulated Gate Bipolar Transistors (PP-IGBTs) are commonly connected in series and stacked together with heatsinks using an exterior clamping fixture in order to achieve high voltage dc-link levels. A suitable contact area between the clamping fixture and the device is essential to ensuring optimal PP IGBT thermo-mechanical performance, especially for the first and last devices in a stack. In this study, the effects of the clamping area on collector deformation, temperature, and stress distribution are investigated by means of the finite element method (FEM). Moreover, the paper analyzes the influence of heatsink thickness to maximize the stress evenness of the terminal PP IGBT and reduce the overall length of the stack system. The results indicate that the collector lid is prone to warpage due to thermal expansion, which results in a decrease in the effective contact area between component layers. As the contact resistance increases, the chips accumulate considerable heat. Increasing the clamping area at this point can adequately compensate for the warp deformation and can also improve the stress uniformity of the chips. Finally, an experiment making use of stress-sensitive film has been carried out to verify the developed FEM models.**

***Index Terms*—Press Pack Insulated Gate Bipolar Transistors (PP IGBTs), clamping area, thermo-mechanical performance, FEM model**

I. Introduction

Press Pack Insulated Gate Bipolar Transistor (PP IGBT) modules exhibit many advantages, such as explosion-proof package [1], stable short-circuit failure mode [2], and elimination of bonding wires [3]. Therefore, they are ideal solutions for high-power, high-reliability electronic systems, for example, for high voltage direct current (HVDC) transmission and flexible AC transmission systems (FACTS) [4]. The reliability of PP IGBTs is always the major topic in power electronic system design. A key potential failure originates from the uneven mechanical stress distribution within the package [5]. When a clamping force is applied to a device, stress occurs and may produce some deformation. Ideally, the stress should be uniformly distributed among the chips, to maximize the electrical, thermal and mechanical performances.

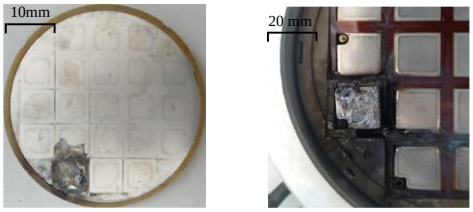

Fig. 1. Images of metal layers within a PP IGBT after failure. (a) Molybdenum plate. (b) Burnt metal surface.

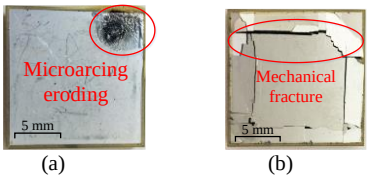

Fig. 2. Typical failures of PP IGBT chips. (a) Micro-arcing eroding. (b) Mechanical fracture.

Since PP IGBTs abandon wire bonding connections, both electrical connections and thermal dissipation use a press pack, and the connection state of each chip is linked to the current path and cooling capacity [6]. The failure test developed by Poller shows that micro-electrical discharge is a possible failure mode and is caused by lost contact between metal layers [7]. Moreover, once the current distribution among the IGBT chips becomes uneven, thermo-mechanical fatigue may occur at some locations that carry extreme thermal stress [8]. More concerningly, if the chips are not in sufficient contact with other components during the short-current moment, the total energy discharge reaches 16 kJ when a peak current of 357.8 kA [9]. Also, the Al metallization of silicon wafer increased heat aids in the formation of molten Al, which further accelerates the degeneration of the chip zone [10]. Fig. 1 presents pictures of burned PP IGBT metal layers following failure. Similar to

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failure patterns reported in the literature, the failure point here occurred on one of the parallel chips. The most plausible reason for this is that the contact condition of the chip is damaged, as after constant current shock and temperature fluctuation cycling, fatigue accumulation results in eventual electrical or thermal failure.

The pressed state of the chips and the stress withstood determine whether it is in sufficient contact, with Fig. 2(a) showing the chip failure caused by too little compressive stress. However, too much compressive stress leads to mechanical fracture, as is shown in Fig. 2(b). As different PP IGBT manufacturers present different chip manufacturing processes, the rated stress for contacts to remain sufficient is about 1.5–12 MPa [11] [12]. In the pre-stress stage, the stress should not be less than the recommended numerical range. However, in the heating stage, the thermal stress and higher temperature caused by power loss should also be considered. In the heating phase, chips with a temperature of 105℃ will withstand compressive stresses greater than 30 MPa [13]. The peak junction temperature should be less than 125℃ in operation [14], and therefore, the thermal stress it causes should be below the corresponding value.

In terms of quantifying the degree of unevenness for mechanical performance, the nonconstant standard deviation is a mature method. The random errors to the standard deviation are added to denote the wall shear stress in a turbulent boundary layer [15]. The standard deviation of the stress is used to describe the fatigue limiting parameter for certain steels and ceramics when quantifying the failure model [16]. Therefore, the standard deviation of the chip stress can be selected to indicate the margin of safety for PP IGBTs.

Normally, several PP IGBTs are placed in a connected series in order to achieve high voltage levels. Each device exhibits a pair of heatsinks mounted on the collector and emitter sides, respectively. In order to clamp the string of PP IGBTs and heatsinks together, a clamping fixture is used at both ends of the string. Reducing the thickness of heatsinks could be of interest because that would reduce the overall length of the stack system [17]. However, when applying a thinner heatsink, the stress distribution of PP IGBTs can be affected, especially in the case of heatsink set between the clamping fixture and terminal PP IGBT, where the clamping fixture geometry exhibits impacts on the performance of the device. Therefore, if an unsuitable heatsink and clamping fixture is used, both of the terminal PP IGBTs will become the weakest link in the whole string.

In the past, simple models based on the finite element method (FEM) were often used to investigate micro-changes in PP IGBTs [18]. Over the years, more complex models, such as those of multi-physical field (electrical-thermo-mechanical) FEM, have been developing to analyze the collector current, temperature and stress distribution [19]. A. Hasmasan found that the clamping conditions mainly influence the uneven stress distribution [20], which becomes much more complicated during the heating process due to its coupling with thermal and electrical performances [21]. As the clamping force increases, the on-state voltage and contact resistance of the PP IGBTs decreases [22]. In addition, the stress distribution is affected by the geometric structure of the fixture [6]. The clamping fixture with a cylindrical shape is a better choice for maintaining the internal stress and temperature distribution. Neglecting thermal expansion, to ensure the stress distribution, the height of the clamping fixture should be larger than the radius of the device [23].

Previous studies, however, usually neglected the heatsink element when building FEM models, and so the numerical results do not accurately reflect the performance distribution. Furthermore, the clamping fixture and device are assumed to exhibit the same diameter, and as according to engineering mechanics theory, the stress (force per unit area) of the chips corresponds to the clamping force and clamping area [24]. Therefore, the thermal parameters are also affected by the size of the clamping fixture.

This paper develops a thermal- and mechanical-based model in order to analyze the performance of PP IGBT. The effect of the heatsink and clamping area on the mechanical performance has been discussed in detail with reference to the uniform clamping pressure exerted on the device. Furthermore, the temperature influence of the stress distribution and deformation has also been investigated, including the conditions of uniform and non-uniform thermal contact resistance. The validated experiments were performed utilizing stress-sensitive films.

II. Modeling of PP IGBT

A. Setting of boundary conditions

The press pack semiconductors are composed of multilayer metal components. The typical structure of a PP IGBT is shown in Fig. 3. In this example, 15 parallel IGBT chips and six Fast

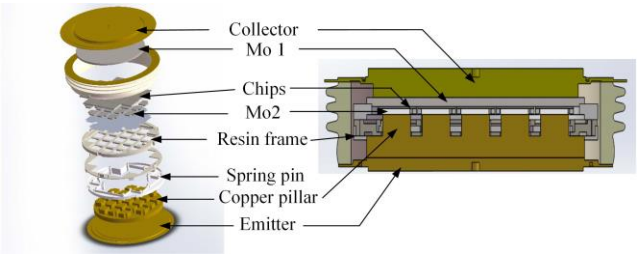


Fig. 3. Internal construction of typical PP IGBT.

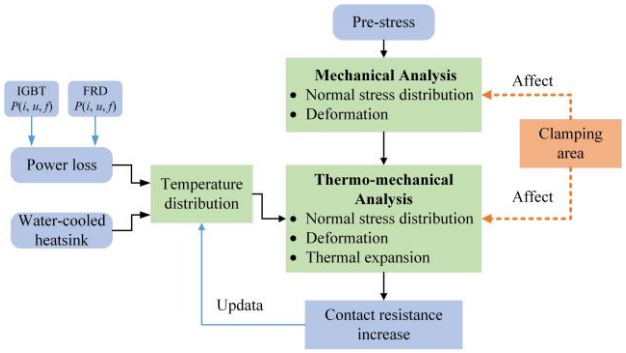


Fig. 4. Flow chart of relationship between clamping area and thermo-mechanical performance of PP IGBT.

TABLE I
DIMENSIONS AND CONSTITUTED MATERIAL OF PP IGBT.

Component	Area (mm^2)	Thickness (mm)	Material
Collector	5674 ($\pi \times 42.5 \times 42.5$)	7.6	Cu
Mo1	4301 ($\pi \times 37 \times 37$)	1.5	Mo
IGBT chip	203.5 ($14.6 \times 14.6 - 3 \times 3$)	0.25	Si
FRD chip	212.5 (14.6×14.6)	0.25	Si
Mo2	169 (13×13)	1.5	Mo
Pillar	169 (13×13)	5	Cu
Emitter	5674 ($\pi \times 42.5 \times 42.5$)	4.4	Cu

TABLE II
MATERIAL PROPERTIES OF STACK.

	k (W/m·k)		CTE(ppm/℃)		C_p	E	ν
	T	Value	T	Value	(J/kg·K)	(GPa)	
Si	50	130	50	2.8	505	190	0.27
	200	82	125	3.1			
Cu	100	391	25	16.4	385	155.1	0.35
	150	390	50	16.7			
Mo	138		5.1		250	312	0.3
Steel	36		1.2		520	210	0.3
Resin	0.75		1.85		1048	5.92	0.35
Gas	0.0173		3.8×10^{-3}		1030	—	—
Al	237		13.1		880	72	0.33

Recovery Diode (FRD) chips of the same size are arranged on the same plane and pressed between two Mo (molybdenum) plates that are used to protect the chips. The collector and emitter enter the package from two sides. Furthermore, the Cu (copper) pillars are laid above the emitter to balance the stress. The gate of every single IGBT chip is connected to the active drive circuit by a spring pin. The resin frame could prevent the chips from shifting, and the package is filled with protective gas. The dimensions and constituted material of each component within the PP IGBT is displayed in Table I. The gate corner of each PP IGBT chip is omitted for simplicity due to their minimal gate leakage currents, and its area is 9 mm^2.

In real application, all of the collector current, temperature and stress distribution are coupled together within the package. In terms of the electrical calculation, the power loss could be equivalent to the heat generation in FEM, therefore, the core issue of coupling simulation is the analysis of heat conduction and solid mechanical [13] [18]. The aim of this paper is to discuss the effect of clamping area on the collector deformation, temperature, and stress distribution without heating and after heating. A flow chart of the relationship between the clamping area and parameter distribution of the PP IGBT is presented in Fig. 4. First, in the pre-stress process (there is no heating), the rated clamping force is loaded onto the stack to ensure that all components within the device are in good contact. Subsequently, the clamping pressure is maintained, and the chips are heated up through power loss, the thermo-mechanical performance is then calculated under different clamping area. In terms of multilayer packaging device, the collector, as a lid of multilayer packaging device, will suffer thermal expansion and edge warpage after heating up. Therefore, the chips at the border of the package will lose their clamping loads, the whole frame within the package is lopsided. As the CTE and thermal time constant of each metal are different, the expansion amount of chips is smaller than that of other metal components, the resulting gap might be in the nm range up to a few μm [13]. Therefore, the chips at the border of the packaging have a degraded contact condition than that of middle. The insufficient contact area between the components increases the thermal contact resistance, which leads to greater heat accumulation. The higher temperature serves to further aggravate such thermal stress, expansion, and deformation. This paper is discussed in terms of the initial state of mechanical analysis without heating, the initial thermo-mechanical analysis with uniform thermal contact resistance, and an analysis with non-uniform thermal contact resistance.

The temperature calculation is set on the basis of the power loss generated by the heat sources of chips (e.g., IGBT and FRD) and the cooling capability of the water-cooled heatsink. This problem is fundamentally described by the diffusion-convection partial differential equation, below:

$$\frac{\partial}{\partial t}T(x,t)-\frac{k}{C_p\rho}\Delta T(x,t)=\frac{q_{loss}}{C_p\rho} \tag{1}$$

where, ρ is the density, C_p the specific heat capacity, k the coefficient of heat conduction, q the heat flux, and T the temperature function with position x and time t.

The power loss of the semiconductors includes conduction and switching loss, which can be calculated by the linear adaptation of the datasheet of a 3,300 V/1,500 A module. The average losses of the IGBT in each sine wave period are delineated as (2) [25]. The threshold voltage $U_{CE0}(T_{vj})$ and on-state slope resistance $r(T_{vj})$ are taken from the *I/U* diagram, i_C is the peak forward current of the collector, m the modulation factor in PWM algorithm, and $\cos\varphi$ the power factor. The switching loss P_{sw} consists of turn-on and turn-off losses. In this paper, the assumption exists that, during a switching period, the duty ratio of the IGBT power switch is 0.5. The power loss dissipation of each IGBT chip is 150W with the switching frequency f_{sw} of 150 Hz and the FRD chips are turned off to reduce the calculation complexity.

$$\begin{aligned} P_{\text{cond,I}} &= \frac{1}{2}\left(U_{CE0}(T_{vj})\cdot\frac{i_C}{\pi}+r(T_{vj})\cdot\frac{{i_C}^2}{4}\right) \\ &+m\cdot\cos\varphi\cdot\left(U_{CE0}(T_{vj})\cdot\frac{i_C}{8}+\frac{1}{3\pi}r(T_{vj})\cdot{i_C}^2\right) \end{aligned} \tag{2}$$

$$P_{sw,I} = P_{on,I} + P_{off,I} = \frac{1}{\pi} f_{sw} \cdot \frac{i}{I_{nom}} \cdot \frac{U_{DC}}{U_{nom}} \cdot \left(E_{on}\left(I_{nom}, U_{nom}, T_{vj}\right) + E_{off}\left(I_{nom}, U_{nom}, T_{vj}\right)\right) \quad (3)$$

The thermal resistance $R_{th\text{-}tot}$ is used to describe the characteristics of heat flow transmission in semiconductors and includes the body thermal resistance $R_{th\text{-}body}$ and thermal contact resistance $R_{th\text{-}cont}$. The $R_{th\text{-}body}$ is related to the element thickness d and section area A. The $R_{th\text{-}body}$ of the PP IGBT electrode is set to 0.002 K/W, the copper pillar is 0.2 K/W, the Mo plate 1 is 0.004 K/W, each Mo plate 2 is 0.09 K/W, and each chip is set to 0.02 K/W.

$$R_{th-body} = \frac{1}{k} \times \frac{d}{A} \quad (4)$$

For coarse contact, the real contact area is much smaller than the apparent contact area, such that the electrical current or thermal flow carried from one component to another is dependent on the roughness of surface l and contact force F_N [26]. From the experimental test, the l of the chip surfaces is 0.14 μm, both Mo plates are 0.22 μm, and the electrodes are 0.5 μm. G is the coefficient of resistance, and v the Poisson ratio. In general, if the thermal conductivity $\Lambda_{th\text{-}cont}$ no longer increases with F_N, it reaches saturation:

$$\Lambda_{th-cont} = \frac{1}{R_{th-cont}} = \frac{7.4k(1-v^2)}{Gl} F_N \quad (5)$$

Just as electrical resistance can be written as U/I, the $R_{th\text{-}tot}$ can also be written as (6), where ΔT is the temperature difference between the ends of the component, and Q is the amount of heat flowing through the element per second [27].

$$R_{th-tot} = \frac{\Delta T}{Q} \quad (6)$$

In terms of the material of components used in the FEM model, the collector, emitter, and pillar are set as Cu. The IGBT and FRD chips are silicon (Si) [28]. The clamping fixture is steel [29]. In particular, the temperature-dependence of metal material will affect the accuracy of the FEM model.

B. Model simplification

In accordance with the stack structure in a real application, the proposed geometry model in this paper consists of PP IGBTs, heatsinks, and a clamping fixture. A 3D view of the geometry model with four PP IGBTs of series-connection is shown in Fig. 5. To increase the heat dissipation, two heatsinks are presented between each of the two adjacent PP IGBTs. The radius of devices is R1–R4, respectively, with R1 being equal to 42.5 mm. The height of clamping fixture H should be larger than the radius of PP IGBT, which can remove the height effects on the stress difference among the chips [23]. Thus, H is designed as 50 mm. In this case, the radius of clamping fixture R in the simulation is changed along with the range from 15 to 70 mm. The contact setting between multilayer within the package is frictional, the friction coefficient of contact surface between Mo plates and chips is 0.5, the other contact layers are 0.75 [6]. The value between heatsink, PP IGBT and fixture is also set to 0.75. In this case, the Augmented Lagrange is selected for frictional contact. The simulation boundary condition is set according to the maximum limit of the datasheet, but in practice applications, the mechanical clamping force should be less than this value to avoid plastic deformation.

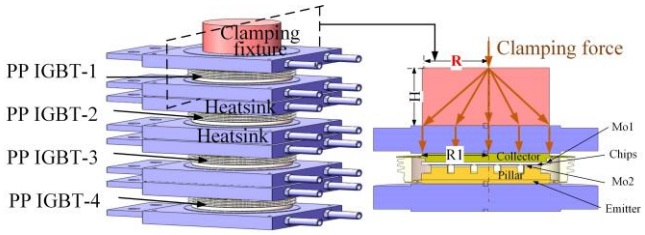


Fig. 5. FEM geometry model of a PP IGBT stack.

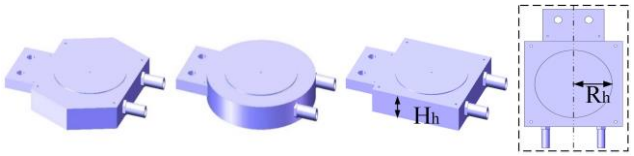


Fig. 6. Shapes for the heatsink.

Three different geometric structures for the heatsink are compared using the heatsink design recommendation [30], as is shown in Fig. 6, where R_h is the effective contact radius with PP IGBT, and H_h is the thickness of heatsink. In order to cool the whole PP IGBT, R_h must be greater than 42.5 mm, which is equal to 50 mm. The internal water pipe of the heatsink may influence thermal convection, but it is not considered in this paper.

In a high-power press pack stack, the assembly includes press pack semiconductors, heatsinks, and busbars. Reducing the thickness of heatsinks would reduce the overall length of the complete stack, which helps increase safety, especially in working conditions with vibrations or bumps. Moreover, as an electrical interface of the stack, according to the calculation formula of metal conductivity (7) [31], the heatsink thickness H_h is inversely proportional to the electrical conductivity Λ_{ele}:

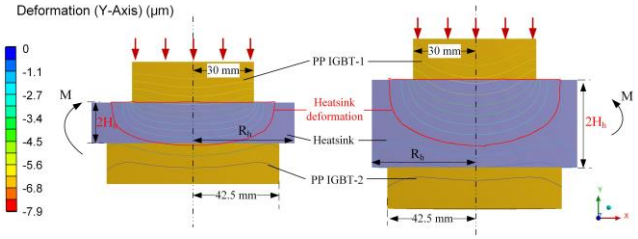
$$\frac{1}{\Lambda_{ele}} = R_{ele} = \frac{\rho_{ele} L}{S_h} = \frac{\rho_{ele} H_h}{\pi R_h^2} \quad (7)$$

where R_{ele} is the electric resistance, the ρ_{ele} of aluminum resistivity is $2.85 \times 10^{-8}\ \Omega \cdot m$, and S_h is the surface area of the heatsink.

A thinner heatsink could help enhance Λ_{ele}; however, as for the water-cooled radiators, formula (8) shows that reducing the thickness or the caliber of the internal water pipe r within the heatsink will sacrifice the fluid flow rate Q_v, by multiplying the cross-sectional area of the pipe A by the flow speed v' [32]. According to formulas (2) and (3), the power loss of PP IGBT q_{loss} is set to 2400W (150W*16), the specific heat capacity of

TABLE III
EFFECT OF HEATSINK PARAMETERS

	H_h<21.25mm (R_h=50mm)	H_h≥21.25mm (R_h=50mm)	Shape
			Square/Hexagon/ Circular
(1) $R_1=R_2=R_3=R_4$	PP IGBT 2-4 have the same results; the stress distribution is even	Stress distribution remains unchanged	Stress distribution remains unchanged
(2) $R_1>R_2>R_3>R_4$	The rim of the devices receives large stress		
(3) $R_1<R_2<R_3<R_4$	The rim of the devices receives small stress		



(a) (b)

Fig. 7 Effect of heatsink thickness on two adjacent IGBTs. (a) $2H_h$=20 mm, (b) $2H_h$=50 mm.

cooling water C_p is 4.186 kJ/(kg•°C), and the density ρ is 996 kg/m^3, assuming that the temperature difference between the inlet and outlet ΔT is 8°C. Therefore, the Q_v should be greater than 4.3 L/m^3 in order to ensure that the heat is effectively removed when designing the heatsink size.

$$Q_{v'} = \mathrm{A}\cdot v' = \left(\pi r^2\right)\cdot v' = \frac{q_{loss}}{C_p \rho \Delta T} \tag{8}$$

Moreover, the purpose of the heatsink is to transmit the clamping loads evenly from above one IGBT to the next and prevent their respective stress distribution from affecting each other [29]. The material of the heatsink is aluminum 6061 T6, the typical tensile strength is 310 MPa, and the yield strength is 275 MPa. The effect of the heatsink parameter on the stress distribution within the PP IGBT has been analyzed and is presented in Table III. In the stack, the clamping force is loaded onto the clamping fixture, and normal stress will occur when the heatsink is placed in compression. When R_h = 50mm, the rating clamping force is 30 ± 5 kN [33] in this case, so the maximum value of compressive stress σ of 4.45 MPa is safe, which less than the allowable stress for the material used.

$$\sigma = \frac{30000 \pm 5000N}{\pi \cdot \left(50mm\right)^2} = 3.18\sim 4.45\ MPa \tag{9}$$

Table III shows that the stress distribution is affected by the heatsink thickness. In the stack, the compressive stresses cause the shape of the heatsink to shorten, as is shown in Fig. 7, where the deformation of the Y-Axis is produced in the heatsink by the given loading. Taking situation (3) of Table III as an example, R1 is equal to 30 mm and R2 to 42.5 mm, and the simplified stack consists of two portions of different materials, Al and Cu, with different moduli of elasticity. Supposing the surface of the heatsink is subjected to pure bending, the moment-curvature equations for the X-Z plate illustrated in (10), where factor D is referred to as the plate stiffness, are used to describe the flexural rigidity *EI* [34]. *I*, the moment of the inertia equation of a rectangle around its centroid axis is shown in (11), *b* is the base or width of the rectangle and *h* its height:

$$\begin{cases} M_x = D\left(\dfrac{\partial^2 w}{\partial x^2} + v\dfrac{\partial^2 w}{\partial z^2}\right) \\ M_z = D\left(\dfrac{\partial^2 w}{\partial z^2} + v\dfrac{\partial^2 w}{\partial x^2}\right) \\ M_{xz} = -D\left(1-v\right)\dfrac{\partial^2 w}{\partial x \partial z} \end{cases} \tag{10}$$

$$D = \frac{Eh^3}{12\left(1-v^2\right)}$$

$$I = \frac{bh^3}{12} \tag{11}$$

Since *I* and h^3 are proportional, as for the heatsink, the flexural rigidity *EI* is proportional to H_h^3. When loading clamping force on the heatsink, the solid will suffer bending, however, with the thickness increase, the flexural rigidity become larger, and the bending deformation of the undersurface will disappear. Fig. 7 compares the effects of different heatsink thickness between two adjacent PP IGBTs. In Fig. 7(a), the undersurface of the heatsink bends when the thickness $2H_h$ is equal to 20 mm, which will transmit inhomogeneous clamping loads. Because the radius of the PP IGBT is R1 < R2, the rim of PP IGBT-2 receives a small amount of stress. In contrast, no deformation occurs on the heatsink undersurface in Fig. 7(b) due to the thickness $2H_h$ becoming larger, equal to 50 mm. By analogy to the short columns of structural member, the column is a lot thicker and can bear higher compressive stress [35].

In terms of the thickness of the clamping fixture, the stress of the chips is relatively uniform and will not change when the fixture height is larger than the radius of PP IGBT [23]. In this case, the stress value also decreases with the $2H_h$ increase, and it is almost constant when $2H_h$ reaches 42.5 mm. Thus, to simplify the analysis model of the PP IGBT string, the total thickness $2H_h$ of 50 mm between each two PP IGBTs is used in the next section.

C. *Mesh sensitivity study*

A three-dimensional geometry model is constructed in Solidworks, the static mechanical and thermo-mechanical finite element analysis are conducted by ANSYS. With the mesh becoming much refined, the stress intensity factor becomes larger [36]. The sharp re-entrant corners of the geometric model or corners of the metal layers induce the singularities that leading to the occurrence of stress concentrations. Therefore,

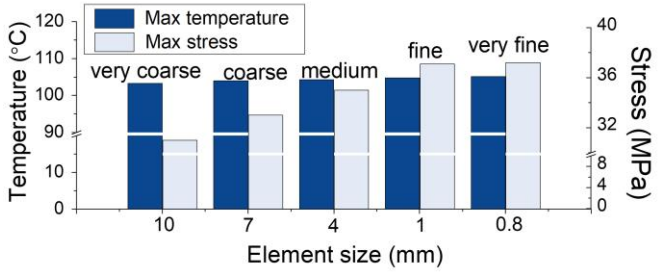


Fig. 8. Effect of mesh density on the simulation results of the chips.

the harder geometries of PP IGBT are modified by modeling the fillets. To verify the convergence of the stress results and determine the optimal configuration for accurate results, a mesh sensitivity study is carried out. The maximum chip temperature and maximum stress (in the heating process) with different element sizes are compared in Fig. 8. The temperature is nearly 105℃ at any element size, which illustrates that it is not obviously affected by the mesh density. In contrast, the stress is sensitive to the element size, the stress increasing with the decrease in element size. The stress difference between the 10 mm size and 0.8 mm size is 22 MPa. Until the size is less than 1 mm, the fine model exhibits a closer result compared to the very fine one, which means that the stress is changed slightly with a more accurate element size. However, the solving time difference between both models is about 500 min. Therefore, the element size of 1 mm for chips and two Mo plates would be the appropriate value to use for parametric studies, whereas the other components use 3 mm to reduce the consuming time. In terms of the mesh methods in Ansys workbench, there are various methods such as tetrahedron, hex-dominant, multizone and automatic. The hex-dominant method automatically generates hexahedron elements outside the solid and tetrahedron elements inside, which suitable for bulk geometry. The multizone sweep method does not need to slice the geometry and can automatically generate hexahedral mesh. The solid domains of the chips and Mo plates mesh with the hexahedral cells, and others are discretized with the multizone method, yielding a total of 226,442 elements and 883,387 nodes.

III. FEM Simulation

A. *Effect of clamping area without heating*

In the pre-stress stage, the clamping fixture applies to the stack to ensure that the components within the device remain in good contact, and no current occurs through the PP IGBT in this stage. Therefore, this section analyzes the effect of the clamping area on the collector and chips' mechanical performance without heating. According to PP IGBT manufacturer's recommended loading range, the loads applied on the stack is variable. The clamping pressure of 4.5 MPa is loaded onto the stack, so with the clamping area increase, the clamping force is also increased.

The collector lid deformation (PP IGBT-1) is shown in Fig. 9. The extracted path, along with the diameter of the collector surface, is marked with a red arrow. When R = 15 mm, the rim of the collector is in an upward warp, whereas the central

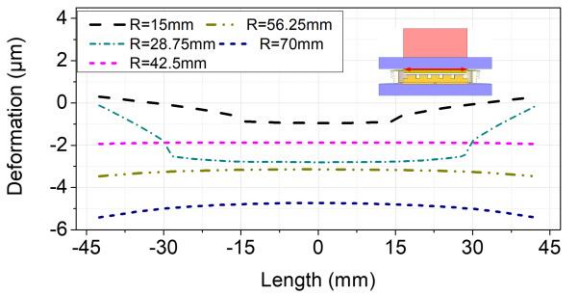


Fig. 9. Effect of clamping area on collector deformation without heating up, (Y-Axis).

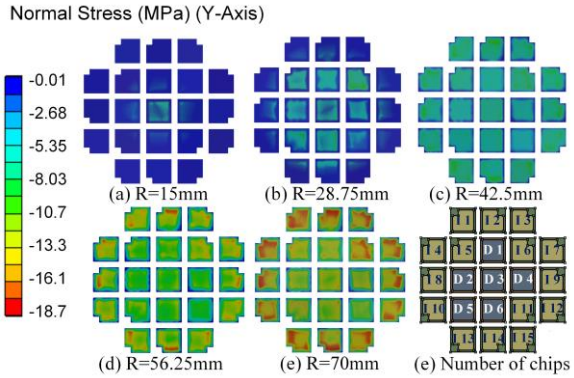


Fig. 10. Normal stress distribution amongst chips without heating up.

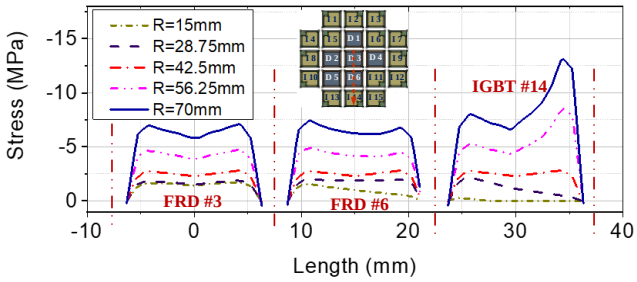


Fig. 11. Normal stress comparison of the extracted path without heating up.

position is slightly concave, and the deformation magnitude is 1.3 μm. Then, the concave range is extended with an increase of R to 28.75 mm, and the deformation magnitude increases by double. R = 42.5 mm, the radius of the PP IGBT, is the best value to select. No warping is produced, which means that the clamping force can be evenly transferred. However, the larger clamping area (R > 42.5 mm) causes the collector edge to bend downwards.

The stress is a physical quantity that expresses the internal forces of the continuous material, and the normal stress refers to that which is exacted on a loaded member by an axial force [24]. The tensile stress is considered positive normal stress and the compressive stress as negative. The absolute value of normal stress σ is equal to the axial force F divided by the compressive area A.

$$\sigma = \frac{F}{A} \tag{12}$$

In the rating clamping state [29], the σ of the PP IGBT does not exceed the proportional limit of the metal material, and so with Hooke's law it follows that:

$$\varepsilon = \frac{\sigma}{E} = \frac{F}{AE} \tag{13}$$

where E is the Young's Modulus, σ the stress, and ε the strain.

Considering that the thickness of collector H_C is 7.6 mm, the uniform compressive area A_C is equal to the clamping area of the clamping fixture. ε is the deformation per unit thickness of the collector under axial loading, with the deformation δ written as:

$$\delta = \varepsilon H_C = \int_0^{H_C} \frac{F}{A_C E} dx \tag{14}$$

According to the collector deformation of the Y-axis in Fig. 9, the deformation value differs with the change in the clamping area A_C. Moreover, the results show that bending in the collector also occurred when the loads are perpendicular to the collector's axis. The maximum normal stress σ_{max} is at the upper and lower edges of the maximum bending moment cross-section [24]. In (15), y_{max} is the distance from the solve point to the neutral surface, I_y the moment of inertia of the cross-section to the neutral axis, and M_{ymax} the bending moment of the cross-section, where I_y/y_{max} is only decided by the cross-section's shape and physical dimensions:

$$\sigma_{\max} = \frac{M_{y\max}}{I_y / y_{\max}} \tag{15}$$

The moment-curvature equations are shown as (10)–(11). The σ_{max} and bending degree of the collector surface are affected by the compressive area, and therefore the compressive range for multiple metal layers is also changed, which leads to the peak stress occurring at different chips. Each chip is numbered as shown in Fig. 10(f). The chips D1 to D6 are 6 FRD chips located at the center area of the module, and the others are 15 IGBT chips numbered 1 to 15. For example, higher stress is produced in the center chips in R that are less than 42.5 mm, as shown in Fig. 10(a) and (b). In this case, the surface area of PP IGBT is 56.7 cm^2; when R is 15 mm, the loading area is only 7.1 cm^2, and the peak stress occurs perpendicularly on FRD #3. As a result, a partial loss of contact occurs among the components within the rim of the package. With the clamping radius increase, the force load range becomes large. Fig. 10(d) and (e) indicate that the higher stress tends to the outer circle chips. Fig. 10(c) presents a much better distribution where R equals to the device, with the result being the same as in [13].

Meanwhile, due to the almost symmetrical distribution for each sample, the compressive stress of FRD #3, FRD #6, and IGBT #14 are extracted to present the exact change from the center to the edge within the package. The extracted path corresponds to the arrow, as is shown in Fig. 11. Because the minimum rating is 3.18 MPa in this case [33], R < 42.5 mm is an unreasonable choice, as the stress of IGBT #14 is nearly 0 MPa when R of 15 mm, the decrease in the contact area is a possible factor that can cause micro-arcing and ablation failure [7]. However, for R > 42.5 mm, the maximum stress point occurs at the edge of IGBT #14. In particular, the maximum value in R = 70 mm is 13 MPa. Every chip withstands the relatively close stress in R = 42.5 mm. In summary, the stress distribution is sensitive to the external clamping condition, and the even stress distribution can be obtained when R = 42.5 mm.

B. Effect of clamping area with uniform thermal contact resistance

The thermal simulation for the FEM model is based on a steady-state analysis. In the material library, the thermal conductivities of the components are created and assigned. In terms of constrain settings, all PP IGBT chips are subjected to an identical power loss and insulated from each other. The thermal convection of the heatsink surface is assumed to be 1,500 W/m·K and the water cooling temperature is set to 50℃ [22]. The outer surface of the ceramic is set to a thermal convection of 8.76 W/m·K. The solving environment for the whole PP IGBT is air with an ambient temperature of 20 ℃. The clamping load and connection setting are consistent with the previous section. For 21 chips, the thermal contact resistance between each pair of chip-Mo is set to 0.11 K•W [37]. Fig. 12 shows the temperature distribution among the chips in the heating process. No electrical current occurs through the FRD chips, but the FRDs still withstand the temperature due to the thermal coupling effect of their multichip structure. The temperature of each chip is calculated by averaging the temperature at the mesh nodes [27]; the temperature difference between IGBT #14 and FRD #3 is 14.3℃. Moreover, for the cross-view of PP IGBT, the thermal transmission paths spanned the chips to the electrodes. The role of the pillar is to protect the gate spring pin, and it also can make the emitter further from the chips layer, which leads to the temperature of the emitter being lower than that of the collector.

The thermal stress and expansion are caused by the mismatch of CTE between the adjacent metal layers and the temperature gradient acting on the interface. Compared with the original shape, each metal layer exhibits varying degrees of expansion and warping. In Fig. 13, the red curve shows the deformation caused by thermal expansion without clamping force, where a maximum of 37 μm occurs at the collector edge and a minimum

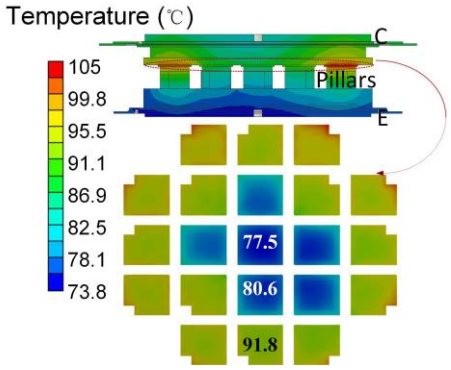


Fig. 12. Temperature distribution of PP IGBT.

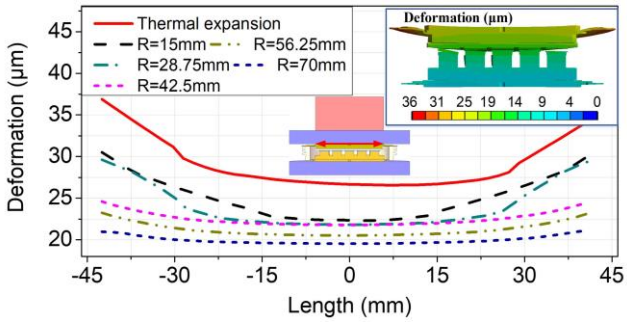


Fig.13. Effect of clamping area on collector deformation in the heating process (Y-Axis).

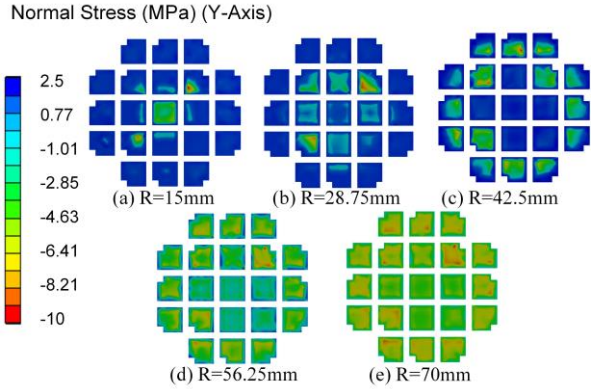


Fig. 14. Normal stress distribution amongst chips in the heating process (Y-Axis).

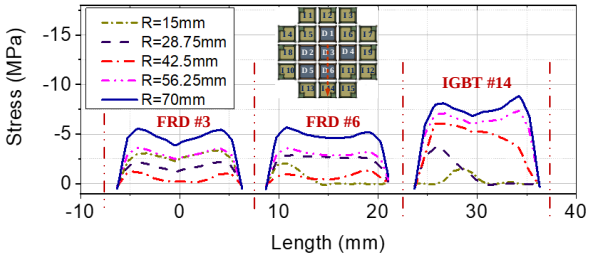


Fig. 15. Normal stress comparison of the extracted path in the heating process.

of 26.4 μm in the center position. The clamping fixture could effectively reduce the expansion and compensate for the deformation, especially for the collector edge. When R < 42.5 mm, only the expansion of the center position can be restricted, but the denting effect still cannot be addressed. In contrast, the smallest deformation magnitude is obtained when R is equal to 70 mm.

The normal stress distribution among the chips under different clamping areas is shown in Fig. 14, and the normal stress of the extracted path is illustrated in Fig. 15. The results show that the temperature is another important factor affecting the stress distribution and press state; (16) is the thermal stress equation.

$$\sigma = E \cdot \alpha \cdot \Delta T \tag{16}$$

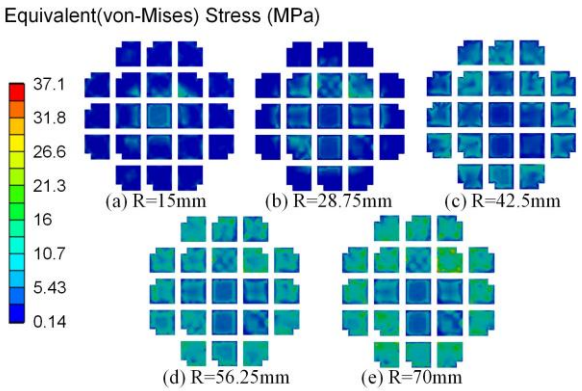


Fig. 16. Equivalent Stress distribution amongst chips in the heating process.

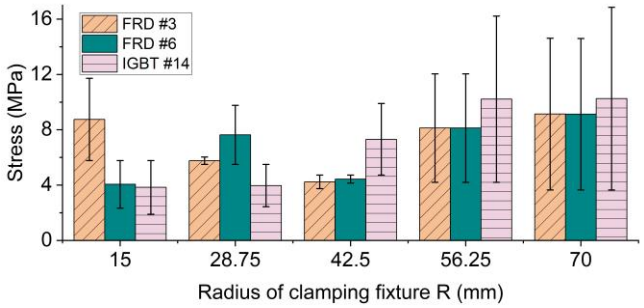


Fig.17. Chip stress comparison with uniform thermal contact resistance.

TABLE IV
COMPARISON OF STRESS EVENNESS WITH UNIFORM THERMAL CONTACT RESISTANCE

R(mm)	15.00	28.75	42.50	56.25	70.00
Minimum	#14	#14	#3	#3	#3
Maximum	#3	#3	#14	#14	#14
Standard deviation	2.77	2.49	1.72	1.21	0.98

Since the metal layers suffer serious thermal expansion due to the temperature increase, and the size of the chip becomes larger. All chips withstand the tensile stress caused by thermal expansion and compressive stress caused by clamping, both interfering with each other. Compared with the stage without heating, the absolute value of normal stress is relatively reduced due to the influence introduced by the thermal expansion. However, if the expansion is not effectively restricted, the chips mainly take tensile stress. Take R of 15 mm and 27.5 mm for example, the collector lid appears the deformation warpage of edge, the outer chips within the package lose their clamping loads, which leads their thermal expansion is unlimited. Partial chips withstand compressive stress, and the others take tensile stress, leading to unreliability of the entire device.

According to [38], [39], and [40], the von Mises stress is used to indicate the complex stress state and dangerous region of the chips. The equivalent stress is shown in Fig. 16, where R = 42.5 mm is not the best selection for maintaining the uniformity of stress distribution. The outer circle chips endure a larger degree of stress than the center chip because they

withstand higher temperatures. For example, the maximum stress of IGBT #14 is nearly 17.6 MPa; and FRD #3 is 6 MPa. The extreme differentiation (11.6 MPa) is a critical possible cause of chip failure. In the case of R > 42.5 mm, the stress distribution is relatively homogeneous, and the differentiation of the maximum stress between IGBT #14 and FRD #3 declines to 7.3 MPa when R = 70 mm.

For every single chip, the stress at all mesh nodes of the chip is averaged, and the average value is then taken as the chip's stress value; the stress values of FRD #3, FRD #6, and IGBT #14 are compared in Fig. 17. When R < 42.5 mm, IGBT #14 exhibits the smallest stress due to the insufficient contact resulting from collector warping. The stress difference between IGBT #14 and FRD #3 is 3.11 MPa when R = 42.5 mm, and it decreases to 2.25 MPa when R = 70 mm, where it reaches nearly a 38% reduction in the stress difference. In Table IV, the standard deviations between the three chips' stress values are compared to evaluate the evenness of the stress distribution. Compared with the R of 42.5 mm, the clamping radius of 70 mm is desirable for ensuring the evenness of stress in the heating stage.

C. Effect of clamping area with non-uniform thermal contact resistance

In section B, the initial thermal contact settings of 21 chips are the same; however, some metal layers are separated (as shown in Fig. 13) after heating up, and the thermal contact resistance within the IGBT package will increase. Moreover, the temperature distribution among the chips is uneven under the thermal coupling effect, so the deformations and warps of chips are various, which results in the different thermal contact resistances. Therefore, the thermal contact resistance settings of the 21 chips must be updated. As the increased thermal contact resistance will lead to the chips withstand greater heat accumulation, the mechanical performance must be calculated again with the changed temperature.

The gap between the chip and Mo plate can be understood as increasing the roughness of each other. Formula (5) shows that the thermal contact resistance $R_{th\text{-}cont}$ relates to the roughness and clamping condition, so that the increased $R_{th\text{-}cont}$ can be obtained through the calculation of the deformation differences between the chip surfaces and the Mo plate, as displayed in Table V. Δd1 is the deviation of contact pair chip-Mo plate 1 and Δd2 is that of contact pair chip-Mo plate 2. The results show that the deformation deviation is affected by not only the chips' position but also the clamping area, and that the chips at the edge of the package (IGBT #14) withstand a higher deformation difference than those at the center position (FRD #3). Moreover, since the warpage of the components being compensated with the increase of the clamping area, both Δd1 and Δd2 are decreased.

The thermal resistance $R_{th\text{-}tot}$ is increased due to a significant increase in $R_{th\text{-}cont}$, and thereby the relevant temperatures must be updated. According to (6), the updated temperature is obtained through the growth values of $R_{th\text{-}tot}$. Fig. 18 shows the three chips' temperatures, including that with initial uniform $R_{th\text{-}cont}$ and the update non-uniform $R_{th\text{-}cont}$. Compared to the former, the latter becomes greater because the $R_{th\text{-}cont}$ is

TABLE V
DEFORMATION DEVIATION AMONGST CHIPS

R(mm)		15.00	28.75	42.50	56.25	70.00
FRD #3	Δd_1 (μm)	1.4	1.4	1.3	1.2	1
	Δd_2 (μm)	1.2	1.16	1.1	0.8	0.25
FRD #6	Δd_1 (μm)	1.8	1.34	1.31	1.21	1.18
	Δd_2 (μm)	1.54	1.29	1.16	1	0.3
IGBT #14	Δd_1 (μm)	2.3	1.8	1.5	1.4	1.3
	Δd_2 (μm)	2.8	2.13	1.3	0.82	0.1

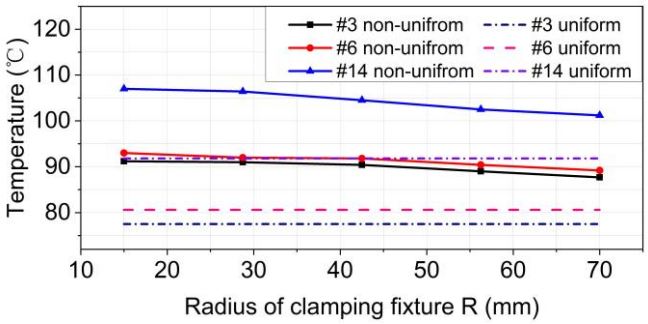


Fig.18. Chip temperature with different clamping areas.

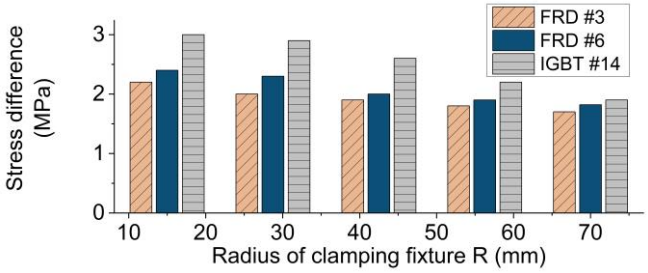


Fig. 19. Differences in chip stress between uniform and non-uniform thermal contact resistance.

increased, which is caused by the decrease in the contact area. Furthermore, a negative correlation is found between the temperature and clamping area.

According to formula (16), the strain and stress relate to the temperature, and increasing the temperature scale will directly lead to the level of mechanical stress changing. The average stress of each chip is calculated with the uniform and non-uniform $R_{th\text{-}cont}$, respectively. The results from the uniform $R_{th\text{-}cont}$ are displayed in Fig. 17. Fig. 19 shows a comparison of the stress difference between both conditions. For the five clamping areas, the stress deviation is reduced when the clamping area increases. One possible reason for this phenomenon is the temperature of R = 70 mm being less than that of R = 15 mm and the thermal stress being smaller. Moreover, a larger clamping area provides a better limit for the thermal expansion stress and the warpage deformation is recompensed. Therefore, in a real application, the effect of the temperature factor on the stress value is reduced by using the clamping fixture with a greater radius.

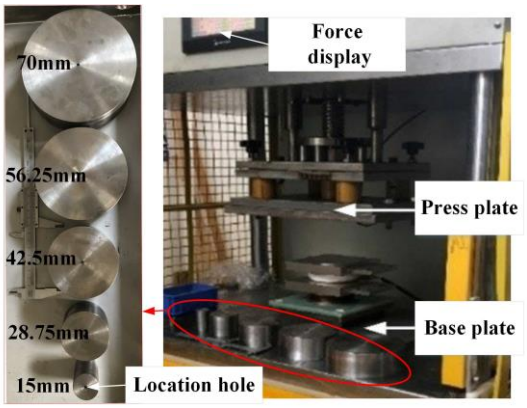


Fig. 20. The experimental set up.

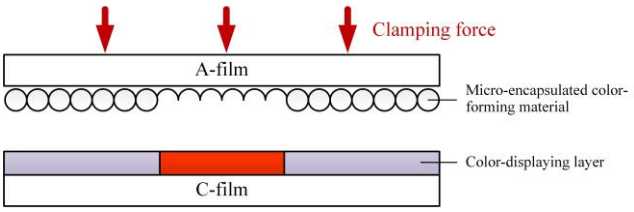


Fig. 21. Operating principle of stress-sensitive film.

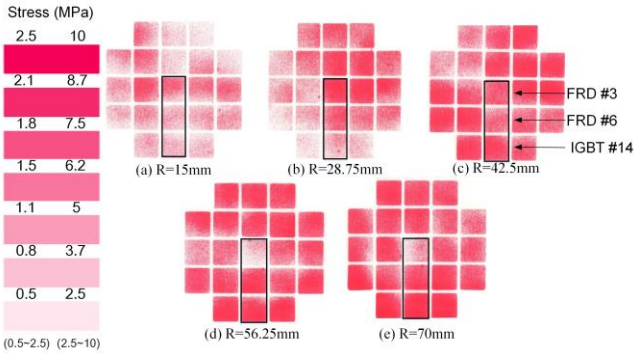


Fig. 22. Experimental results of stress distribution over the chips.

IV. Experimentation

The experimental tests are carried out using the setup shown in Fig. 20. Five steel cylinders with different radius are designed to clamp the heatsink and PP IGBT. All of cylinders exhibit an identical height of 50 mm with polished surfaces. The center of each surface has a location hole that helps to evenly load the vertical force. The test bench assembles the press plate, base plate, press machine, and clamping force display. The clamp plate and base plate are adjusted in parallel to one another, and the parallel distance between both plates is measured by a distomat. During the operation, the stack is placed over the base plate, and the press plate moves down slowly to load the clamping force. Meanwhile, the sizes of all of the internal components of the PP IGBT are measured, and then screened to ensure that the height tolerance is less than 2 μm. The configuration of the experimental conditions is the same as

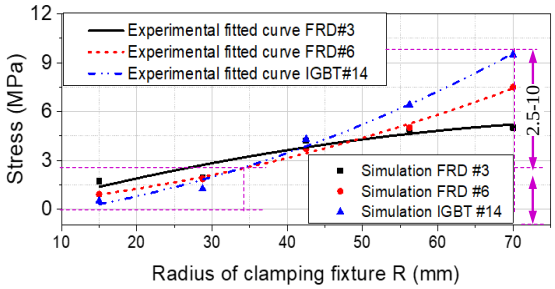


Fig. 23. Comparison of experimentation and simulation for chip stress.

TABLE VI
COMPARISON OF EXPERIMENTATION AND SIMULATION FOR EVENNESS AMONGST CHIPS

	R (mm)	FEM	Experiments	Error (%)
15.00	Minimum		IGBT #14	
	Maximum		FRD #3	
	Standard deviation	0.77	0.7	10.3
28.75	Minimum		IGBT #14	
	Maximum		FTD #6	
	Standard deviation	0.39	0.36	11
42.5	Minimum		FRD #6	
	Maximum		IGBT #14	
	Standard deviation	0.27	0.251	7.5
56.25	Minimum		FRD #3	
	Maximum		IGBT #14	
	Standard deviation	0.92	0.846	6.7
70.00	Minimum		FRD #3	
	Maximum		IGBT #14	
	Standard deviation	2.05	2.021	6.9

what is set out in the FEM simulation.

The compressive stress distribution over the chips is obtained using stress-sensitive films. Because the film is electrically- and thermally-insulated, the stress distribution is verified without heating. The films are placed between the Mo plates 1 and chips. The stress-sensitive film consists of two polyester bases, as shown in Fig. 21. The A-film coated with a layer of micro-encapsulated color-forming material and C-film with a layer of the color-displaying material. When the load is applied, the microcapsules are broken and the color-forming material reacts with the color-displaying one, with red patches appearing on the film [41]. After the measurement, the compressive stress can be approximately estimated depending on the intensity of red spots in the film. The pure red corresponds to the maximum stress value of the film measurable range, and the pure white is equal to the minimum value. Thus, the compressive stress value can be calculated according to the color saturation which can be obtained by the RGB normalization value of the image, shown as (17) [42]:

$$S = 1 - \frac{\min(R,G,B)}{\max(R,G,B)} \tag{17}$$

Fig. 22 shows the compressive stress distribution with different clamping areas, with the stress values calculated accordingly by the standard color sample density [43]. The films exhibit several types for different measurement ranges. In Fig. 22(a) and (b), the films can test the value between 0.5 MPa and 2.5 MPa. Thus, the stress magnitude of entire chips is less than 2.5 MPa. In Fig. 22 (c)–(e), another level film (2.5–10 MPa) is applied to record higher stress.

FRD #3, #6, and IGBT #14 are also chosen for quantitative comparison, with the color saturation of each chip being calculated by averaging the 256 × 256 pixel dots with the image-processing method in computer-aid software, and the stress value of the chip being obtained by means of the color saturation-stress conversion. The relationship between each chip stress and clamping radius is delineated in Fig. 23. The measurement results correspond to the trend that shown in the simulations. The curve-fitted mathematical model of experimentation is also given as (18)–(20):

$$\sigma_{D3} = -0.57+0.14R+0.0008R^2 \quad (18)$$

$$\sigma_{D6} = 0.18+0.03R+0.001R^2 \quad (19)$$

$$\sigma_{I14} = 0.53-0.01R+0.002R^2 \quad (20)$$

Again, the standard deviation between the chips is represented in Table VI. The agreement between the experimental data and simulation results is also compared. From the comparison, the simulated values are generally consistent with the measurement data, and the errors are kept within 11%. It is evident that among the three selected chips, the maximum stress changes from #3 to #14 with the increasing clamping area. The most uniform stress distribution is obtained when R = 42.5 mm. Therefore, the experimental results confirm the accuracy of the developed FEM model.

V. Conclusion

This paper presents a thermal and mechanical analysis of the clamping area influence in the PP IGBT module. The study investigated performance over chips with differently-sized clamping areas using analytical, numerical, and experimental methods. From this, the following conclusions can be drawn:

1) When the radius of the clamping fixture R is designed to be identical to that of the PP IGBTs (e.g., 42.5 mm in this paper), the best results were shown to maintain the evenness of the stress distribution among the chips in the process without heating power.

2) However, when the heating power is taken into account, the device suffers significant thermal expansion, warpage, and sees an inhomogeneous distribution of stress and temperature. An extreme case is the stress difference between chips, which can reach up to 11.6 MPa when the clamping radius R is equal to 42.5 mm. It is also found that increasing the clamping area could effectively reduce thermal expansion and achieve an even stress distribution. As the clamping radius R increased from 42.5 mm to 70 mm, the stress difference between the edge chip and center chip is nearly a 38% reduction.

3) For the four PP IGBTs series-connection stack, where the diameter of each device differed, the simulation results showed that the stress distribution within each PP IGBT was also affected by the heatsink thickness. When the total heatsink thickness between each of two adjacent PP IGBTs was greater than 42.5 mm, as in this case, the evenness of the stress distribution could remain.

The present work can be applied to mechanical design in high-power converter applications and can also be extended to combine with other methods to develop an optimal solution for enhancing thermo-mechanical reliability and optimizing heatsink size and clamping area.

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