A cost-efficient Current-Source Gate Driver for SiC MOSFET Module and its Comparison with Voltage-Source Gate Driver

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***Abstract*— A current-source gate driver (CSG) is considered as a candidate to improve the switching performance of Silicon Carbide (SiC) MOSFET compared with a SiC MOSFET powered by a voltage-source gate driver (VSG). Various CSG circuits have been proposed to promote the switching transients by generating a constant gate current. However, those circuits are normally designed with complicated structures and high costs due to extra components and control signals. This paper proposes a cost-efficient approach to adjust the gate current of the conventional VSG which can improve its dynamic performance of the devices. Following the comparison analysis of CSG and VSG, a simple-structure circuit is introduced to replace the gate resistor in the conventional VSG. This circuit transforms that the gate current shows constant levels during the switching transients, which exhibits current-source characteristics. Simulation and experimental studies have been undertaken to verify the effectiveness of the proposed circuit. The results show that the turn-on switching time and oscillation can be reduced using the proposed circuit compared with the conventional VSG and the proposed circuit is less hardware intensive compared to other CSGs.**

Keywords—current-source gate driver, switching performance, SiC MOSFET module, turn-on time

I. INTRODUCTION

SiC MOSFET is widely considered as one of the next generation power semiconductors due to its superior features for high voltage, high frequency, high power density and high temperature applications [1]–[7]. However, the fast switching speed and short switching time introduce sharp electrical overshoot and high electromagnetic interference (EMI). In order to reduce the high oscillation during the switching transient of SiC devices, numerous research attempts have been carried out in the past few years [8]–[10]. As the direct control unit over SiC device, the gate driver plays a crucial role to address the issue of the oscillation. The conventional voltage source gate driver (VSG) generates constant gate voltage and charges the gate-source capacitance (C_{gs}) through the gate resistors. VSG works well with most Si devices but can limit the potential of SiC devices. It is reported that SiC MOSFETs have a lower switching speed compared to its counterpart Si (e.g. CoolMOS) using conventional VSGs [11]–[14]. Therefore, various gate driver topologies have been proposed to improve the switching performance of SiC MOSFET where the current-source gate (CSG) driver exhibits the superior features in controlling of switching transients [15]–[18]. However, all the proposed gate current generation methods require extra components and control signals, which increases the complexity of the circuity and cost. This paper proposes a relatively simple-structure and cost-effective circuit to convert the varying gate current in conventional VSG to be constant during switching transients without using any additional control signal. Thus, the gate driver can exhibit current-source characteristics as other CSG counterparts. Section II presents the theoretical analysis of the switching transient and the comparison of VSG and CSG. In section III, a simple-structure circuit is proposed to control the gate current, and the advantages of this structure over the widely-used resonant CSG structure have been discussed. Section IV presents the simulation verification of the proposed gate driver circuit using a developed circuit model. Moreover, the double-pulse test (DPT) platform is constructed to evaluate the performance of the proposed gate driver in section V. The conclusion of the research work is given in the last section.

This work was supported by the Engineering and Physical Sciences Research Council (EPSRC), UK, for the project of Reliability, Condition Monitoring and Health Management Technologies for WBG Power Modules (EP/R004366/1)

II. THEORECTICAL ANALYSIS

Despite the variety of CSG topologies that have been published to improve the gate driving performance [19]–[21], there is a lack of comparison between CSG and VSG. Thus, this section takes the turn-on transient as an example, illustrating the features of CSG and its advantage in improving the performance of SiC MOSFET compared to VSG.

The diagram of the key waveforms of MOSFETs turn-on transient is illustrated in Fig.1. The PWM turn-on signal comes at t_0, trigging the turn-on process of the MOSFET. The turn-on transient consists of the following 3 time intervals, namely pre-switching, switching and post-switching periods:

Stage 1: Pre-switching period (t_0~t_1). The gate current starts to charge the gate-source capacitor of the MOSFET until the gate voltage reaches gate threshold voltage. In this period, the drain current (i_D)remains nearly zero (usually < 1mA), while the drain-source voltage (v_{DS}) is kept at the DC bus voltage. Therefore, the power loss at this period ($P_{pre\text{-}sw}$) is negligible ($P_{pre\text{-}sw}$ is less than 1W if V_{DC} = 1000V).

Stage 2: Switching period (t_1~t_2). This period starts from the rising of drain current until the end of the Miller plateau where the drain-source voltage (v_{DS}) falls to zero. The gate current and gate voltage remain constant during this period,

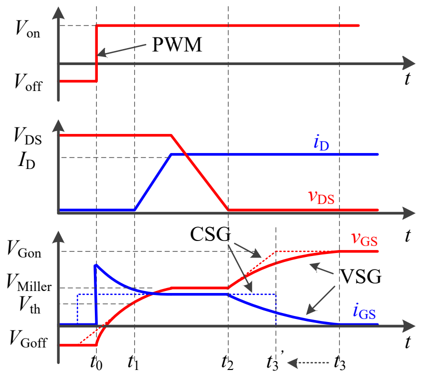


Fig.1. Diagram of the key waveforms of MOSFET turn-on transient using VSG and CSG

which determines the switching speed of the MOSFET. Also, this period is the main source for the switching loss as both the voltage and the current across the MOSFET are around rated values.

Stage 3: Post-switching (t_2~t_3). The gate voltage rises from the Miller plateau to on-state gate voltage (V_{Gon}). In this period, drain current (i_D) is around the rated current, the drain-source voltage is much less than DC bus voltage (V_{DC}), but as the gate voltage is lower than the on-state gate voltage, the drain-source voltage (v_{DS}) is several times higher than the on-state voltage drop of the MOSFET. Therefore, the quantified power loss during this period is much higher than pre-switching period.

Fig.1 also shows the comparison between VSG and CSG where the solid and dotted lines represent the waveform of VSG and CSG respectively. It is shown that the gate current is relatively high at the beginning of the switching transient in VSG. Therefore, VSG has a very short pre-switching period (t_0~t_1) compared to CSG. By contrast, the third stage (t_2~t_3) VSG switching takes much longer time as the gate current is much lower which results in longer switching time and more

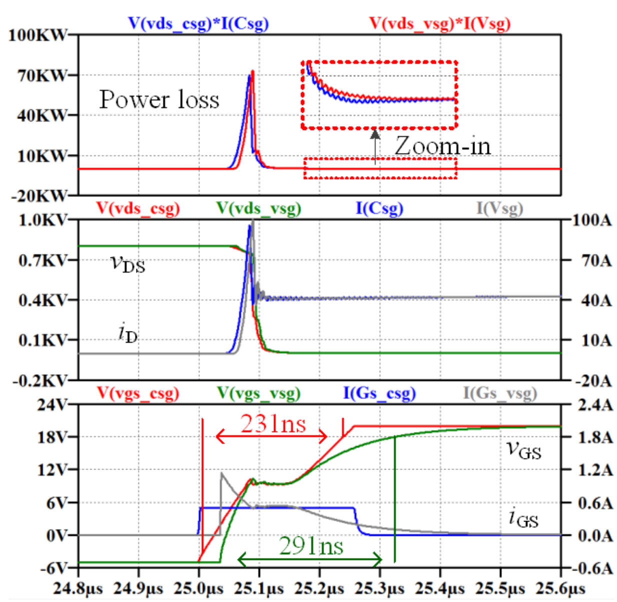


Fig.2. Simulation of the comparison between CSG and VSG

losses. To ensure the same switching speed (dv_{DS}/dt and di_D/dt), the constant gate current has the same value as the Miller gate current for VSG as shown in Fig.1. Therefore, the second stage (t_1~t_2) in CSG is the same as VSG, whereas the first stage is extended slightly and the third stage is shortend significantly (t_3 is shifted to t_3'). As what have been discussed above, the average power loss of stage 1 is much lower compared to stage 3. As a result, the overall switching loss and switching time in CSG is less than those in VSG.

Fig.2 illustrates the quantitative analysis of the performance of the gate drivers in simulation using the model developed from a commercial SiC MOSFET product. SiC MOSFET from CREE/Wolfspeed, CPM2-1200-0025B is used as the device under test, whose rated voltage is 1200V and rated current is 98A. The spice model of the chip is simulated under the test condition of 800V/40A. The conventional VSG with 20Ω gate resistor is compared with CSG with 500mA constant gate current. According to the simulation results, the waveforms of v_{DS} and i_D are almost the same as shown in Fig.2, which shows the same switching speed of the two gate drivers. However, it also demonstrates that the power loss of CSG is slightly lower than VSG during the post-switching period. Moreover, the switching time of CSG is reduced by 26% compared with VSG. In conclusion, CSG can reduce the power loss and switching time compared with VSG when they are applied to the same device.

III. Proposed Gate Driver Circuit

The proposed gate driver structure is presented in Fig.3(c), along with the structures of conventional VSG in Fig.3(a) and widely-used resonant current-source gate driver in Fig.3(b). This section firstly illustrates the principle for the proposed gate driver circuit, before the benefits and compromises are presented in comparison with the other two structures in the aspects of gate driver loss and complexity.

A. Working principle

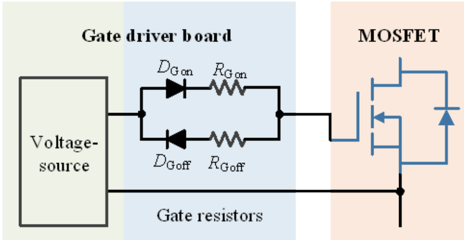
The proposed gate driver circuit consists of a pair of complementary bipolar transistors (Q_{Gon}, Q_{Goff}) and two resistors (R_{Gon}, R_{Goff}). During the turn-on transient, Q_{Gon} is turned on while Q_{Goff} is turned off, the gate current flows into the MOSFET is presented in the following equation:

$$I_{Gon} = \beta_{PNP} \cdot \frac{V_{Gon}}{R_{Gon}} \tag{1}$$

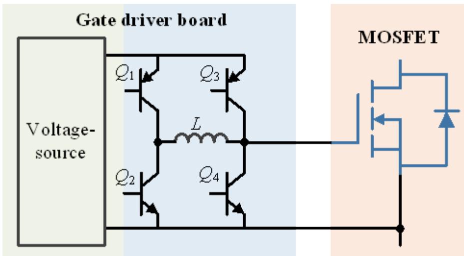
Similarly, the gate current during the turn-off transient is:

$$I_{Goff} = \beta_{NPN} \cdot \frac{|V_{Goff}|}{R_{Goff}} \tag{2}$$

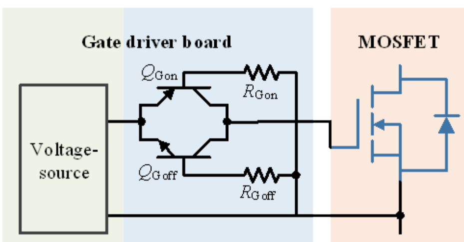
where I_{Gon} and I_{Goff} are the gate currents during turn-on and turn-off transient, respectively; V_{Gon} and V_{Goff} are the on-state and off-state gate voltage, respectively; β is the current gain of the BJTs. Since all the parameters keep constant with time, the gate current is clamped constant for both turn-on and turn-off transients. Moreover, the charging gate current is controllable with different values of the resistors.



(a) Conventional voltage-source gate driver



(b) Resonant current-source gate driver



(c) Proposed current-source gate driver

Fig.3. Schematic of (a) conventional voltage-source gate driver, (b) resonant current-source gate driver and (c) proposed current-source gate driver

B. Comparison

The proposed gate driver circuit is compared with conventional VSG and widely-used resonant CSG as is shown in Fig.3. In conventional VSG, the gate voltage is generated by the voltage-source and charges the gate capacitor through gate resistors. In the resonant current-source gate driver, gate current is generated in the inductor L. In terms of complexity, VSG and the proposed CSG are similar, as both of the topologies are very simple: only one gate driving control signal is required and components count is less than resonant CSG. The proposed CSG structure is easy to be integrated in most of the existing VSG as only two BJTs and resistors are included and the control system can be kept unchanged. In contrast, the resonant CSG requires an additional inductor and 4 switches with PWM control circuits to generate the constant current. Thus, the cost and circuit complexity are much higher than the proposed method.

Resonant CSG still shows some advantages on the flexibility to control the gate current value as i_G can be changed without hardware modification. Another advantage of resonant CSG is the lower power loss of the gate driver [19]. For the conventional VSG and the proposed CSG, the power loss of the gate driver can be calculated using (3).

$$E_{GD} = \int V_{Gon} \cdot i_{Gon} \cdot dt + \int V_{Goff} \cdot i_{Goff} \cdot dt \qquad (3)$$

where E_{GD} is the gate driver loss during the switching transient; V_{Gon} and V_{Goff} are the constant value of on-state and off-state gate voltage, respectively; i_{Gon} and i_{Goff} are the gate currents during turn-on and turn-off transient that is changing through the transient. Taking the constant value out of the integral, equation (4) can be derived.

$$E_{GD} = V_{Gon} \int i_{Gon} dt + V_{Goff} \int i_{Goff} dt \qquad (4)$$

The relationship between the gate current and the gate charge Q_G is shown as follows:

$$Q_G = \int i_{Gon} dt = \int i_{Goff} dt \qquad (5)$$

Thus, the expression of E_{GD} can be rewritten as:

$$E_{GD} = (V_{Gon} + V_{Goff}) \cdot Q_G \qquad (6)$$

The energy E_{GD} is consumed by the gate resistors in VSG. The loss for the proposed CSG is the same as VSG, except that E_{GD} is consumed by BJTs. For the resonant CSG, the gate driver loss is 10%~50% lower than conventional gate driver with different inductance [19].

In conclusion, resonant CSG has lower gate driver loss than conventional VSG and the proposed CSG circuit, but the structure is more complicated and expensive. The proposed CSG has a similar simple structure as VSG. Gate driver power losses are also similar. Therefore, the proposed CSG is an easy way to transform VSG into current-source behavior.

IV. Simulation Verification

In order to verify the effectiveness of the proposed circuit, a simulation double-pulse circuit was created as shown in Fig.4 using TINA, which is a simulation software from Texas Instruments (TI). The switching characteristics is simulated and presented in Fig.5.

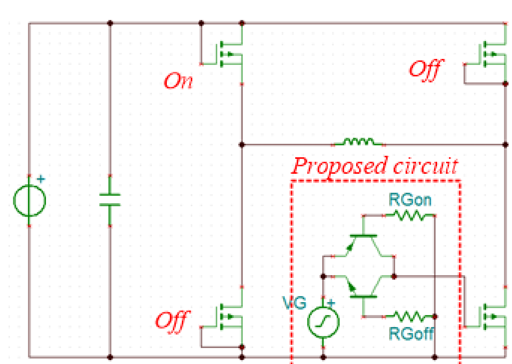
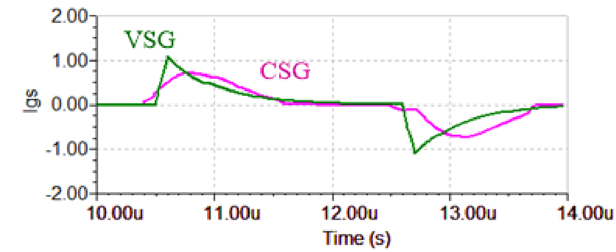
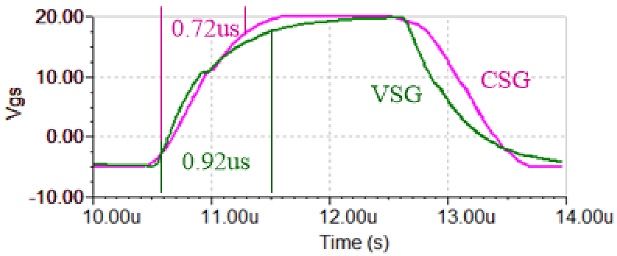


Fig.4. Schemetic of the simulation circuit

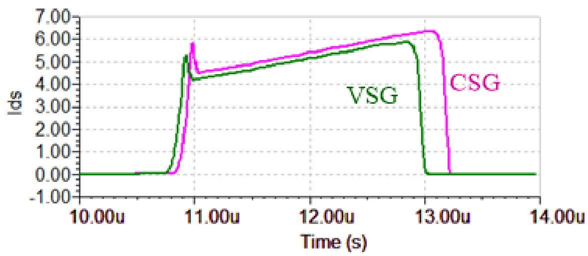
1200V rated voltage and 500A rated current. A picture of the



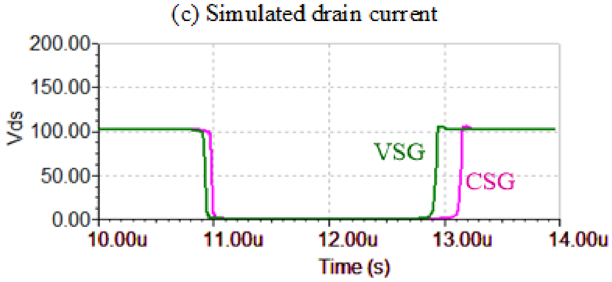
(a) Simulated gate current



(b) Simulated gate voltage



(c) Simulated drain current



(d) Simulated drain-source voltage

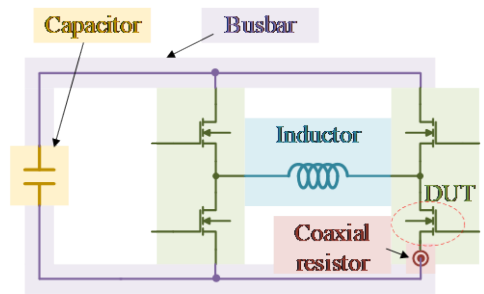
Fig.5. Simulation results

As shown in Fig.5(a), the peak gate current of the proposed circuit is 20% lower than the conventional VSG. Moreover, it is presented in Fig.5(b) that the turn-on time of the proposed circuit is 0.72us, which is shorter than the turn-on time of the conventional gate driver with 0.92us. The effectiveness of the proposed circuit to reduce the switching time is therefore verified in simulation.

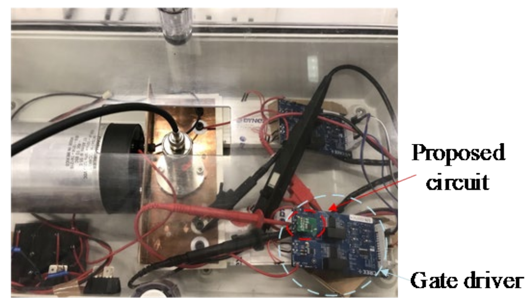
V. Experimental Comparison

The proposed circuit and a double-pulse test platform are constructed to evaluate the performance of the proposed CSG circuit in comparison with conventional VSG. The diagram of the test platform is shown in Fig.6(a) and the picture of the test platform is illustrated in Fig 6(b).

In the experiment, the SiC MOSFET module (DYN-NC-SIC) from Dynex is used as the device under test, which has



(a) Diagram of the test platform



(b) Picture of the test platform

Fig.6. Experiment test platform: (a) diagram of the test platform; (b) picture of the test platform

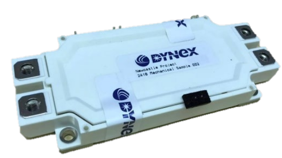


Fig.7. Picture of the device under test: DYN-NC-SIC

SiC MOSFET module is demonstrated in Fig.7. The module consists of 7 SiC MOSFET bare dies (CPM2-1200-0025B) from CREE, each has voltage rating at 1200V and current rating at 98A.

The double pulse tests are conducted using the proposed circuit and the conventional voltage-source gate driver (CGD15HB62P1 from CREE/Wolfspeed) separately. The test condition is set as follows: the drain-source voltage (V_{DS}) is 100V, the drain current (I_D) is 50A, the gate resistance (R_G) is 20Ω.

The comparison of the proposed current-source gate driver and voltage-source gate driver is presented in Fig.8. As is shown in Fig.8(c) and Fig.8(d), the drain-source voltage and drain current are almost the same with minor oscillation reduction. For the turn-on time, as analyzed above, the proposed CSG shows a shorter turn-on time (1.58us) than VSG (2.13us). However, the experiment shows that on-state gate voltage drops after the proposed circuit is used, for which the mechanism is under further investigation.

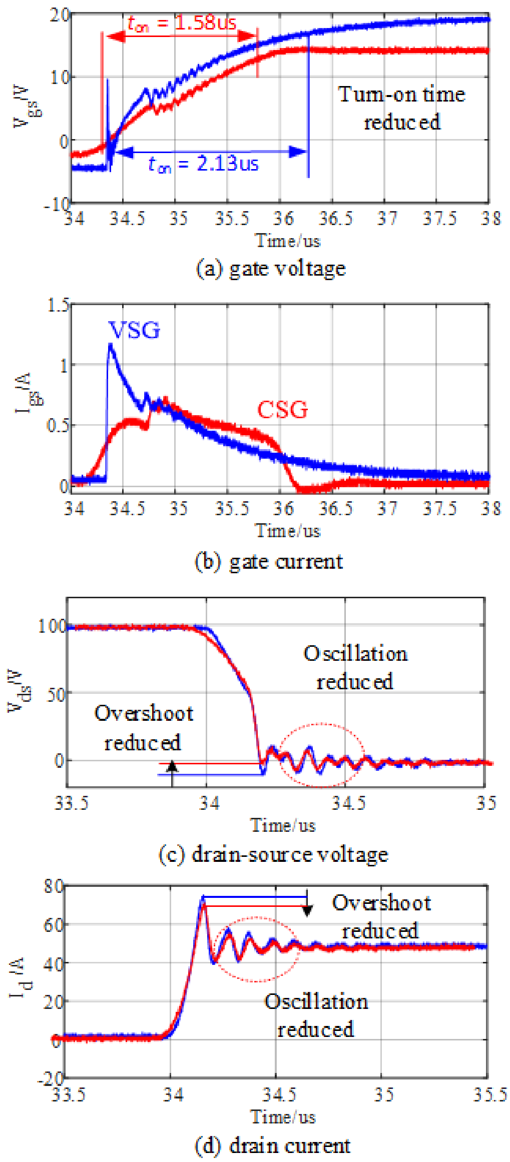


Fig.8. Experiment comparison between proposed current-source gate driver (red waveform) and voltage-source gate driver (blue waveform)

VI. Conclusion

This paper presents a comparative analysis between voltage-source gate driver and current-source gate driver. Moreover, a cost-efficient gate driver circuit is proposed to enable the commercial voltage-source gate driver to equip current-source characteristics, which can reduce the switching time significantly. The proposed circuit is compared with VSG and widely-used resonant CSG, showing advantages on the simple structure compared with resonant CSG. A gate driver circuit was designed and constructed to verify the effectiveness of the proposed method. The experimental results show that the turn-on time is reduced by 25% with the proposed circuit.

Acknowledgment

The authors thank the financial support provided by the Engineering and Physical Sciences Research Council (EPSRC), UK, for the project of Reliability, Condition Monitoring and Health Management Technologies for WBG Power Modules (EP/R004366/1).

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