Investigation into the Switching Transient of SiC MOSFET Using Voltage/Current Source Gate Driver

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Abstract

This paper investigates the influence of current-source and voltage-source gate driver on the switching transient performance of trench and planner SiC MOSFETs. Devices have been tested at different temperatures and switching speeds using the designed double-pulse testing system. To evaluate the performance of different gate driving approaches, the dynamic transients of SiC MOSFETs are analysed and discussed using different values of gate resistors and controlled gate currents. The results show that the current-source gate driver has a higher switching speed than voltage-source counterparts at the same transient changing rate of drain-source voltage, resulting in lower operating losses for the power devices. Therefore, current-source gate drivers can facilitate power converters to achieve higher efficiency compared with voltage-source gate drivers.

1 Introduction

SiC power devices have superior characteristics to traditional Silicon counterparts in terms of the conduction loss, switching frequency, voltage and temperature property [1]. The emergence of such device impels the power conversion circuits towards higher switching frequency and higher operating temperature. Today, SiC MOSFETs can be implemented as planar or trench structures. The planar structured SiC MOSFET has a lower switching loss at high voltage operation compared to trench-type MOSFET, but it has a higher on-resistance due to the structure of the JFET region [2]. In contrast, the SiC MOSFET with trench structure can achieve lower on-resistance with smaller conduction loss but has issues on oxide breakdown in the gate bottom because of higher electric field concentration [3]. To explore the influence of gate driving techniques to SiC MOSFETs, this paper compares the performance of the current and voltage source gate drivers operating on the Trench and Planar SiC MOSFET through evaluating the switching transients.

Conventional voltage source gate drivers (VS-GD) have been widely applied in the power conversion circuits such as dc/dc converters [4, 5], for example, to actively control the power switches due to the low cost and simple structure. The increase of the switching speed in SiC power device can generate problems such as overshoot, oscillation and additional losses [6, 7]. Therefore, several different types of VS-GD have been proposed to reduce the overshoots, oscillations, and losses issues of SiC [8, 9]. However, VS-GD has the disadvantages of the limited switching speed caused by the gate impedance network and inherently have a low output impedance that is prone to induce oscillation during the switching transients [10]. Also, the additional voltage drop on the gate resistor can lead to a significant influence on the gate current. In contrast, current source gate drivers (CS-GD) have a high output impedance to damp oscillation, and there is no impact of the voltage drop in the gate drive owing to the direct control of the gate current. Thus, some different types of current source gate driver have been proposed to improve the switching performance of power semiconductors, such as constant current gate driver [11], resonant current gate driver [12], hybrid gate driver [13] and programmable current driver [14-16]. Despite using different structures, the fundamental features of such gate drivers are similar because of the same inherent current-source characteristics.

This paper analytically investigates the turn-on and turn off transients of SiC MOSFETs using voltage and current-source gate driver, respectively. Also, the influence of the temperature to the switching transients has been experimentally studied when applying both gate drivers. Furthermore, the comprehensive comparison and discussion of utilising different gate resistors and controlled gate current have been given in detail.

2. Structures of the Voltage/Current-source Gate Driver and SiC MOSFETs

2.1 Structure of the VS-GD/CS-GD

It is well known that the gate driver can significantly influence the dynamic performance of the power switches. To explore the impact of the different gate driving approaches to switching transients, two gate drivers have been utilised for comparative study. The voltage source gate driver used in the paper is the gate driver board CRD-001 from Wolfspeed (CREE). The structure of this gate driver is illustrated in Fig. 1(a), which is normally utilised in mature commercial gate driver board. A photo of the voltage source gate driver used in

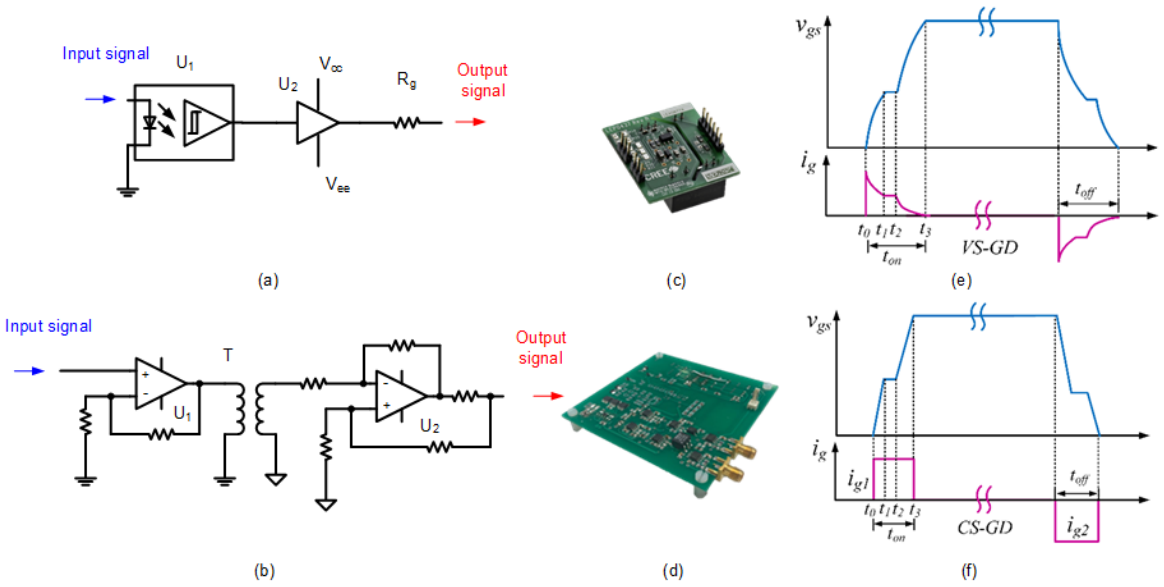

Fig. 1 (a) Diagram of VS-GD; (b) Diagram of CS-GD; (c) Photo of VS-GD; (d) Photo of CS-GD; (e) Voltage-source gate driving waveform; (f) Current-source gate driving waveform

the paper is shown in Fig.1(c). In the conventional voltage source gate driver structure, a fast opto-isolator U1 with high common-mode transient immunity is used to isolate high voltage from the controller, and a gate driver IC boosts the output voltage and current to the required values. The gate resistor can be populated to provide optimum turn-on and turn-off performance while the specific value of the gate resistor is commonly determined by compromising between the switching losses and voltage overshoots. Compared with the mature voltage source gate driver, the current source gate driver is not widely commercially available. The schematic of the proposed current-source gate driver with high-frequency transformer and amplifier is shown in Fig.1(b), and Fig.1(d) presents a photo of the proposed current source gate driver. This current-source gate driver has a simple structure with three functional parts: signal amplification, signal isolation and signal conversion. The input signal can be generated by the controller before the signal is amplified using the amplifier U1. In order to isolate the high voltage from the control system, a transformer T is used before the amplified signal is converted into the corresponding current signal with the assistance of amplifier U2. There are 3 main functions of the proposed gate driver: firstly, amplification: the small input signal generated by the controller is amplified from less than 1V to the gate voltage level (-5V to 15V); secondly, isolation: the control system can be isolated from the high-voltage power circuit; thirdly, conversion: the voltage control signal is converted into the gate current signal, therefore, the constant gate current can be generated once a constant voltage signal is input into the gate driver.

2.2 Gate driving waveforms

Fig.2(c) shows the diagram of SiC MOSFETs with parasitic capacitors. The typical waveforms of the gate current and

Table 1 Gate voltage and gate current expressions

Time period	Voltage source gate driver		Current source gate driver	
	V_{gs}	I_g	V_{gs}	I_g
$t_0 \sim t_1$	$V_{gon}(1-e^{\frac{-t}{R_g(C_{gs}+C_{gd})}})$	$\frac{V_{gon}}{R_g}e^{\frac{-t}{R_g(C_{gs}+C_{gd})}}$	$\frac{I_g t}{C_{gs}+C_{gd}}$	I_g
$t_1 \sim t_2$	$V_{gs(pl)}$	$\frac{V_{gon}-V_{gs(pl)}}{R_g}$	$V_{gs(pl)}$	
$t_2 \sim t_3$	$V_{gon}-(V_{gon}-V_{gs(pl)})e^{\frac{-(t-t_2)}{R_g(C_{gs}+C_{gd})}}$	$\frac{V_{gon}-V_{gs(pl)}}{R_g}e^{\frac{-(t-t_2)}{R_g(C_{gs}+C_{gd})}}$	$\frac{I_g(t-t_2)}{C_{gs}+C_{gd}}+V_{gs(pl)}$	

voltage using VS-GD and CS-GD are illustrated in Fig.1 (e) and Fig.1 (f) respectively. The switch-on process can be generally divided into three subintervals using both gate drivers. For VS-GD, in the subinterval of $t_0 \sim t_1$, there is a step voltage stress across the gate capacitors through gate resistor R_g, which results in a gate current surge, and the expression of the gate current is obtained as:

$$\frac{V_{gon}}{R_g} e^{\frac{-t}{R_g (C_{gs}+C_{gd})}} \quad (1)$$

where V_{gon} is the on-state gate voltage, C_{gs} and C_{gd} represent the gate-source and gate-drain capacitors, respectively. When the gate voltage reaches the Miller plateau voltage $V_{gs(pl)}$ in the subinterval of $t_1 \sim t_2$, the gate current becomes relatively constant and the value is given as:

$$\frac{V_{gon} - V_{gs(pl)}}{R_g} \quad (2)$$

In the subinterval of $t_2 \sim t_3$, the gate current drops as

$$\frac{V_{gon} - V_{gs(pl)}}{R_g} e^{\frac{-(t-t_2)}{R_g (C_{gs}+C_{gd})}} \quad (3)$$

The corresponding expressions of the gate voltage are given in Table I. In contrast, for CS-GD, the gate current remains the set value I_g in the entire switching transients and the change of V_{gs} is proportional with the coefficient of $I_g/(C_{gs}+C_{gd})$ except during the Miller Plateau region. The specific expression of the gate voltage in each subinterval can also be found in Table I.

2.3 Planar/ Trench structure SiC MOSFETs

Fig. 2 (a) and (b) shows a typical cross-section view of the structure of planar and trench MOSFETs, respectively, and

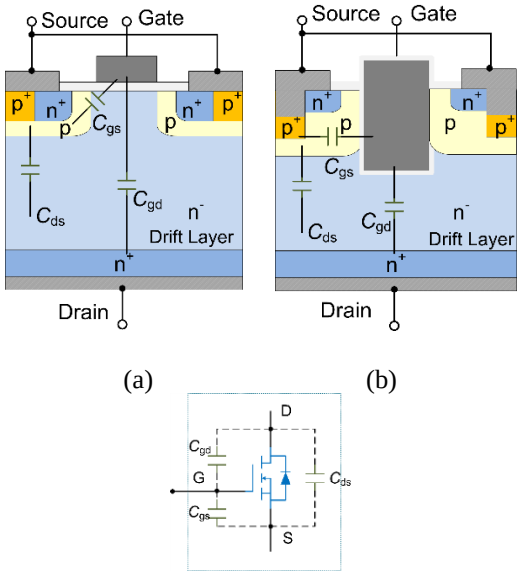

Fig.2 (a) Planar structure SiC MOSFETs (b) Trench Structure SiC MOSFETs (c) Simplified diagram of SiC MOSFET

Fig.2 (c) is the simplified diagram of SiC MOSFET. According to the difference of the structure, planar MOSFETs can realise higher voltage rating owing to the thicker drift layer, but with increased on-resistance which is caused by the current flowing path and the existence of the inner JFET region. Moreover, the channel mobility of planar MOSFETs is usually lower because of the manufacturing technique. Therefore, the higher percentage of resistance is coming from the channel in the planar structure. Trench MOSFETs usually have lower on-resistance due to the higher channel density and a shorter flowing path, but the breakdown voltage is commonly lower because of the thinner drift layer. Also, generally speaking, the input capacitance C_{iss} ($C_{iss} = C_{gs}+C_{gd}$) of SiC planar MOSFETs is smaller than that of the Trench MOSFETs which is also determined by the structure of thicker drift layer, thereby, the SiC planar MOSFETs can achieve higher switching speed with less switching loss, compared with the trench counterparts.

3 Experiment Results

3.1 Double-pulse Test Set-up

As is shown in Figure 3 (a), the half-bridge topology is used in the double-pulse test set up where the two MOSFETs are of the same type. The top switch is always off which is used as the diode. The bottom switch is connected with the gate driver. When the DUT is turned on, the current is conducted through the inductor, and it increases to reach the test current. Then the DUT is turned off and the current path changes from the DUT to the top MOSFET body diode; after a short period, the DUT is turned on again, and the switching transient of the device under test is captured using an oscilloscope. The photo of the double pulse test setup is presented in Fig. 3(b). A temperature adjustable heatplate is assembled underneath the power circuit.

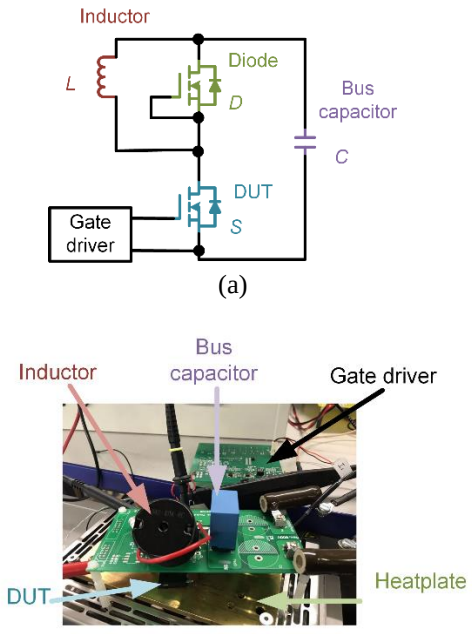

Fig. 3 (a) schematic of the double pulse test set up (b) photo of the double pulse test setup

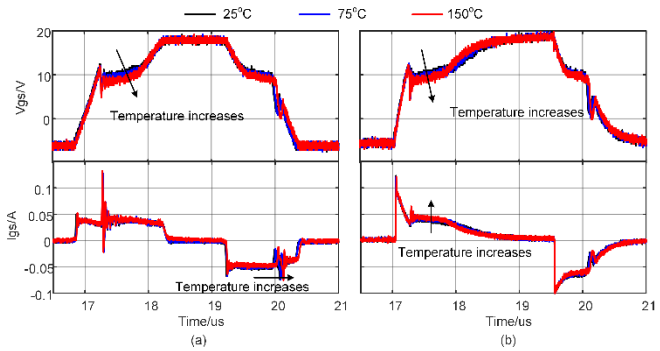

Fig.4 switching transient of trench SiC MOSFET under different temperature. Test condition: V_{DS} = 400V, I_{DS} = 10A. (a) current source gate driver, I_{GS} = 40mA; (b) voltage source gate driver, R_g = 235Ω

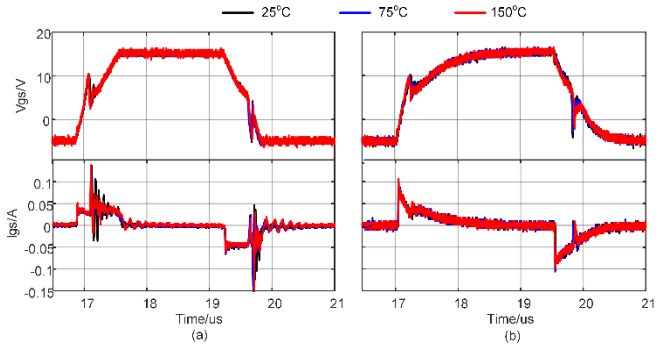

Fig.5 switching transient of planar SiC MOSFET under different temperature. Test condition: V_{DS} = 400V, I_{DS} = 10A. (a) current source gate driver, I_{GS} = 36mA; (b) voltage source gate driver, R_g = 235Ω

board, which is adhesive with power MOSFETs using thermal grease.

3.2 Temperature influence to switching transients

The double pulse test is conducted on two types of SiC MOSFET, SiC trench MOSFET (SCT3060AL) rating at 650V/39A and SiC planar MOSFET (C3M0065090D) rating at 900V/36A. The SiC MOSFET gate driver board CRD-001 from Wolfspeed (CREE) has been utilised as the VS-GD.

The switching transient of the trench SiC MOSFET under different temperature is presented in Fig. 4, where the MOSFETs have been tested at three different temperatures: 25, 75 and 150 °C. In general, the temperature has a small impact on the switching transient, and the gate voltage at Miller plateau region is slightly decreased with the temperature rise from 25 °C to 150 °C, which is in agreement with the study in [17]. The same test procedure has been applied to the planar SiC MOSFET, the similar results can be obtained as is illustrated in Fig. 5.

3.3 Gate current to switching transients

Fig. 6 and Fig. 7 shows the influence of the gate current to the switching transients. The gate current has been set at four

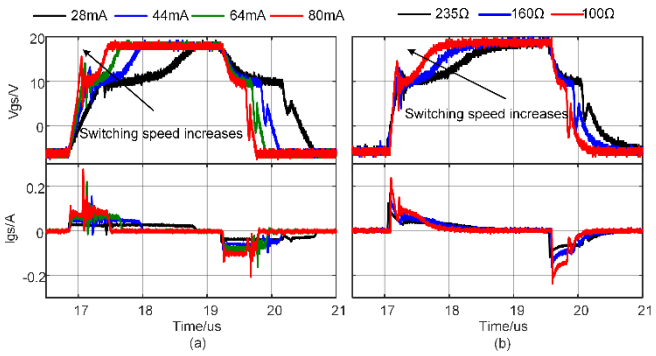

Fig.6 switching transient of trench SiC MOSFET under different switching speed. Test condition: V_{DS} = 400V, I_{DS} = 10A, Temperature = 25°C. (a) current source gate driver; (b) voltage source gate driver

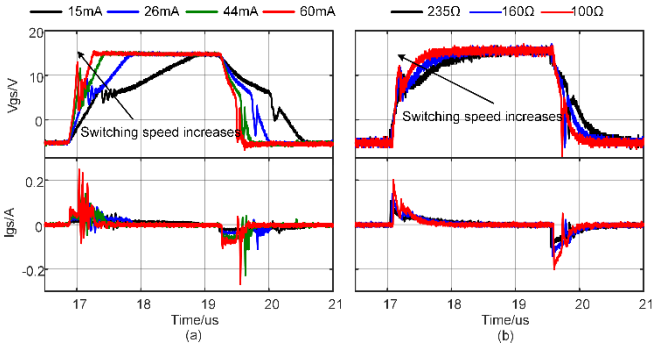

Fig.7 switching transient of planar SiC MOSFET under different switching speed. Test condition: V_{DS} = 400V, I_{DS} = 10A, Temperature = 25°C. (a) current source gate driver; (b) voltage source gate driver.

different values: 28, 44, 64 and 80mA in the CS-GD, and three different gate resistors have been applied in the VS-GD: 235, 160 and 100 Ω. Unlike the temperature, it is evident that the direct-controlled gate current in the CS-GD and the variation of gate resistors in the VS-GD has a significant impact on the switching performance of the SiC MOSFET: higher gate current increases the switching speed of the device but introduces the higher oscillation on both the gate voltage and gate current. In Fig.6, it can be seen that different programmed gate current generates different rising time to reach Miller plateau using the CS-GD, whereas, it is an almost identical time when using different gate resistor using the VS-GD. This phenomenon can also be observed when employing the planar SiC MOSFET as illustrated in Fig.7. It is also noted that the planar SiC MOSFETs have faster turn-on and turn off transient compared with trench counterparts, which is relevant to the smaller gate-source capacitance.

Fig.8 illustrates the switching performances of MOSFETs using the CS-GD and the VS-GD when the same switching speed has been realised. In other words, the device has the same dV/dt and dI/dt during the switching transients. The experiment has been conducted when V_{DS} = 400V, I_{DS} = 10A and the temperature = 25°C. Meanwhile, the gate current I_{gs} is set as 60mA in the CS-GD, and the gate resistor R_g is 160 Ω in the VS-GD. The results show that CS-GD provides shorter

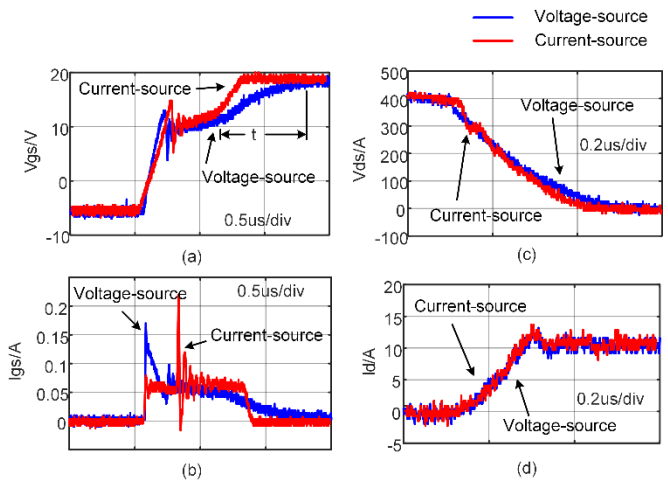

Fig.8 comparison of the current source and voltage source gate driver. Test condition: V_{DS} = 400V, I_{DS} = 10A, Temperature = 25ºC, I_{gs} = 60mA (for current source gate driver), R_g = 160Ω (for voltage source gate driver). (a) gate voltage comparison; (b) gate current comparison; (c) dV/dt comparison; (d) dI/dt comparison.

switching time than the VS-GD. Furthermore, as indicated in Fig. 8, it is can be observed that the gate voltage of the current source gate driver is higher than the gate current during the time *t* after the Miller plateau, which means it can reduce the on-state voltage of the device as well as the operating losses.

4 Conclusion

This paper presents a comparative study of the switching transient of SiC MOSFETs using voltage source gate driver and current source gate driver. Both planar and trench SiC MOSFETs have been tested to investigate the switching performance at different gate driving techniques. It is found that the temperature has a relatively negligible impact on the switching performance for both SiC MOSFETs, and higher switching speeds introduces higher oscillation for both driver technologies. Experimental results show also, that the current source gate driver can achieve faster switching transient at lower switching losses, which is beneficial for the high-efficiency power conversion.

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6 Reference

[1] A. Castellazzi, A. Fayyaz, G. Romano, L. Yang, M. Riccio, and A. Irace, "SiC power MOSFETs performance, robustness and technology maturity," *Microelectronics Reliability*, vol. 58, pp. 164-176, 2016.

[2] ROHM. "Ultra Low Ron SiC Trench Devices." https://www.rohm.com.tw/documents/11405/851226/120517.pdf (accessed 2012).

[3] L. Cao, Q. Guo, and K. Sheng, "Comparative Evaluation of the Short circuit Capability of SiC Planar and Trench Power MOSFET," in *2018 IEEE 2nd International Electrical and Energy Conference (CIEEC)*, 2018: IEEE, pp. 653-656.

[4] P. James, A. Forsyth, G. Calderon-Lopez, and V. Pickert, "DC-DC converter for hybrid and all electric vehicles," in *The 24th International Battery, Hybrid and Fuel Cell Electric Vehicle Symposium and Exhibition (EVS 2009)*, 2009.

[5] H. Wu, V. Pickert, D. Giaouris, and B. Ji, "Nonlinear Analysis and Control of Interleaved Boost Converter Using Real-Time Cycle to Cycle Variable Slope Compensation," *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 7256-7270, 2017.

[6] T. Liu, R. Ning, T. T. Wong, and Z. J. Shen, "Modeling and analysis of SiC MOSFET switching oscillations," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 747-756, 2016.

[7] A. P. Camacho, V. Sala, H. Ghorbani, and J. L. R. Martinez, "A Novel Active Gate Driver for Improving SiC MOSFET Switching Trajectory," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9032-9042, 2017.

[8] A. Niwa, T. Imazawa, T. Kimura, T. Sasaya, T. Isobe, and H. Tadano, "Novel dead time controlled gate driver using the current sensor of SiC-MOSFET," in *Industrial Electronics Society, IECON 2015-41st Annual Conference of the IEEE*, 2015: IEEE, pp. 001651-001656.

[9] Y. Yang, Y. Wang, and Y. Wen, "An active gate driver for improving switching performance of SiC MOSFET," in *2018 7th International Symposium on Next Generation Electronics (ISNE)*, 2018: IEEE, pp. 1-4.

[10] W. Frank and Z. Zheng, "Performance Comparison Between Voltage Source and Current Source Gate Drive Systems," in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2018: VDE, pp. 1-5.

[11] I. A. Mashhadi, E. Ovaysi, E. Adib, and H. Farzanehfard, "A Novel Current-Source Gate Driver for Ultra-Low-Voltage Applications," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 8, pp. 4796-4804, 2016.

[12] P. Anthony, N. McNeill, and D. Holliday, "High-speed resonant gate driver with controlled peak gate voltage for silicon carbide MOSFETs," *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 573-583, 2014.

[13] C.-M. Wang, "A Revisit to Resonant Gate Driver and a Hybrid Driver to Improve EMI vs. loss Tradeoff for SiC MOSFET," in *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of*, 2016: VDE, pp. 1-7.

[14] X. Wang, H. Wu, and V. Pickert, "Design of an Advanced Programmable Current-Source Gate Driver for Dynamic Control of SiC Device," in *2019 IEEE*

Applied Power Electronics Conference and Exposition (APEC), 2019: IEEE, pp. 1370-1374.

[15] H. Obara, K. Wada, K. Miyazaki, M. Takamiya, and T. Sakurai, "Active gate control in half-bridge inverters using programmable gate driver ICs to improve both surge voltage and switching loss," in *Applied Power Electronics Conference and Exposition (APEC), 2017 IEEE*, 2017: IEEE, pp. 1153-1159.

[16] K. Miyazaki *et al.*, "General-Purpose Clocked Gate Driver IC with Programmable 63-Level Drivability to Optimise Overshoot and EnergyLoss in Switching by Simulated Annealing Algorithm," *IEEE Transactions on Industry Applications*, 2017.

[17] J. O. Gonzalez, O. Alatise, J. Hu, L. Ran, and P. A. Mawby, "An investigation of temperature-sensitive electrical parameters for SiC power MOSFETs," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7954-7966, 2016.