Phenomenon of Short-Time Threshold Voltage Shift and Its Application in Junction Temperature Estimation

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***Abstract*—Silicon carbide (SiC) has seen tremendous advancement in high-efficiency, high-frequency, and high-temperature applications during recent years. However, the gate oxide of SiC MOSFET is reported to be less reliable compared with its Si counterpart, introducing the problem of threshold voltage (V_{th}) shift. Recent publications have investigated V_{th} shift which are mainly based on the long-time scale ranging from seconds to several days. However, the V_{th} shift in a shorter time scale has not been widely discussed and studied due to its high bandwidth requirement in measurement. This paper proposed an investigation into the short-time V_{th} shift using a developed current-controlled gate driver. The phenomenon of short-time V_{th} shift is captured and analyzed, which shows that it occurs within the first microsecond of the gate voltage being applied. Moreover, a modelling approach using the logarithm equation is proposed to describe the relationship between the short-time V_{th} shift and the gate stress time. Experiments are conducted under different temperatures, illustrating the temperature dependency of the short-time V_{th} shift process.**

Keywords—SiC MOSFET, threshold voltage, V_{th} shift, TSEP

I. Introduction

In recent years, Silicon carbide (SiC) has experienced rapid development gaining an increasing widespread use in high-efficiency, high-frequency, and high-temperature applications [1]. As a potent alternative to current silicon (Si) technology, SiC power electronics shows superior characteristics such as higher voltage ratings, lower voltage drops, faster switching speeds, and higher thermal conductivities[1]. Among all the SiC switches (e.g. SiC BJTs, JFETs, MOSFETs and IGBTs), the SiC MOSFET has become the most prevalent switch in the recent 2-10 years[2][3]. However, recent publications show that SiC MOSFET have less reliable gate oxide performance [4], [5]. It is well known that the threshold voltage (V_{th}) is an important parameter to estimate the health condition of a MOSFET[6] and the shift of V_{th} has been investigated in various publications[7][8], which reveals a close relationship between the V_{th} and the gate stress time. On the other hand, the experiments are all conducted in the time scale over seconds which do not cover the study of the short-time V_{th} shift issue that is at switching periods. The phenomenon of short-time V_{th} shift is difficult to observe because of the requirement for high bandwidth sampling circuit in the measurement. This paper presents an investigation into the shot-time V_{th} shift with a new measurement method using a developed current-controlled gate driver. It is shown that the short-time V_{th} shift introduces the dissimilarity between experiment and simulation. Moreover, the investigation into short-time V_{th} shift can provide an a new angle for the gate oxide degradation mechanism. New parameters that are contained in the short-time V_{th} shift process can be used for the area of health condition monitoring.

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II. Mechanism of V_{TH} Shift

V_{th} shift is generally regarded as the results of gate charges trapped in the gate oxide defects. Fig. 1 shows the establishing process of V_{th} shift, including the MOSFET structure, formation of the inversion layer, establishment of the inversion layer and the charge trapping period in oxide which introduces the V_{th} shift.

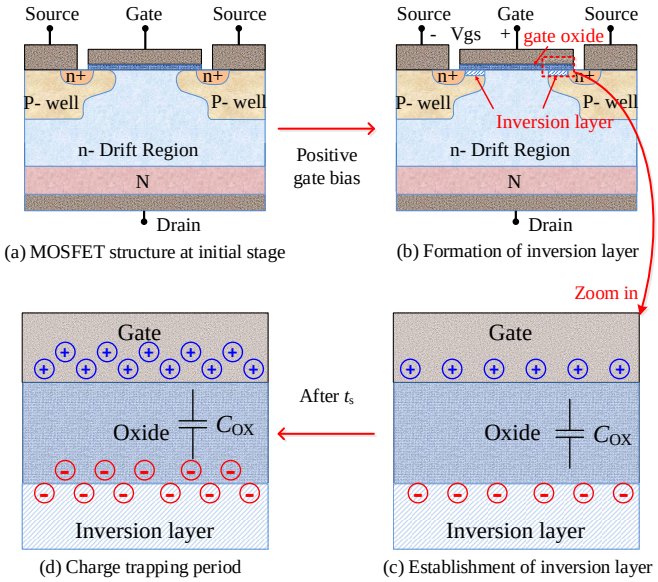

Fig. 1. V_{th} shift mechanism: (a) MOSFET structure at initial stage; (b) Formation of inversion layer; (c) Establishment of inversion layer; (d) Charge trapping period.

The initial structure of MOSFET is shown in Fig. 1(a) without applying gate bias. When a positive gate bias (V_{gs}) is applied across the gate and source terminals and V_{gs} is higher than V_{th}, the inversion layer is formed beneath the gate oxide as shown in Fig. 1(b). The established structure of the inversion layer is demonstrated in Fig. 1(c). The inversion layer is formed by electrons gathering beneath the gate oxide due to the gate bias voltage. The gate charges (Q_g) can be determined by the gate voltage with the equation $Q_g = V_{gs} \cdot C_{OX}$, where C_{OX} is the gate capacitance. After the stress time t_s,

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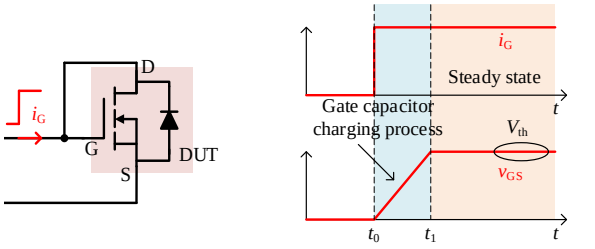
some of the electrons are trapped by the defects inside the oxide, as shown in Fig. 1(d). These trapped charges can no longer move from source to drain. However, the number of charges to form the inversion layer is not changed. Therefore, more charges are needed to conduct the same current, resulting in the positive shift of V_{th}. The shift of V_{th} reflects the number of charges trapped inside the oxide. The negative Vth shift is a similar process when the electrons inside the defects of the oxide are dragged out under negative gate bias. The shift of V_{th} may introduce the breakdown of the gate oxide. When more charges are trapped inside the gate oxide, the electrical field in the gate oxide increases as the distance is narrowed between the gate terminal and the electrons. Therefore, the estimation of V_{th} shift is an important parameter to reflect the health condition of the MOSFET.

III. Phnomenon of Short-Time V_{TH} Shift

The conventional V_{th} shift test consists of 3 steps: firstly, the initial V_{th} is measured before the gate stress; next, the device under test is stressed under a gate voltage for a certain period from 1s to hours; Finally, the V_{th} after the gate stress is measured again. The differences between the V_{th} before and after the gate stress is regarded as the V_{th} shift. However, the gate stressed time under investigation is higher than 1s in publications [9][10]. It is difficult to evaluate the short-time V_{th} shift within 1s, because high bandwidth is require for fast V_{th} measurement. In this section, a new method is proposed to investigate the short-time V_{th} shift using a current-source gate driver.

A. Principle of the Proposed Measurement Method

The diagram of the test circuit and the conceptual waveforms are illustrated in Fig.2(a) and Fig.2(b). In the test, the drain and gate terminals of the MOSFET are shorted. A controlled gate current is generated and injected into the gate of the MOSFET as the blue waveform shown in Fig.2(b). The red waveform is the corresponding gate voltage of the MOSFET, which consists of the charging process and the steady state. The charging process is a linear slope, representing the increase of gate voltage on the gate capacitor under a constant current. After the gate voltage reaches the threshold voltage (V_{th}) at t_1, the gate voltage stops increasing and stays at V_{th}. The behaviour of the gate voltage after t_1 is determined by the short-time V_{th} shift. In the conventional analysis, the gate voltage keeps unchanged, which can be verified by the simulation.



(a) Test circuit (b) Conceptual waveforms

Fig. 2. Principle of the proposed measurement method: (a) test circuit; (b) conceptual waveforms.

B. Simulation Results

The simulation is conducted to verify the analysis of the proposed measurement method as is shown in Fig.3. The Pspice model used in the simulation is SCT3060 provided by its manufacturer ROHM. A step current signal with a magnitude of 25mA is injected into the gate terminal of the MOSFET. It is shown that the charging process starts at 1μs and the gate voltage stops increasing after 1.2μs. The gate voltage then stays at 5.2V after 1.2μs, therefore, the simulated V_{th} is 5.2V. The simulation shows that there is no short-time V_{th} shift identified in the Pspice model from its manufacturer.

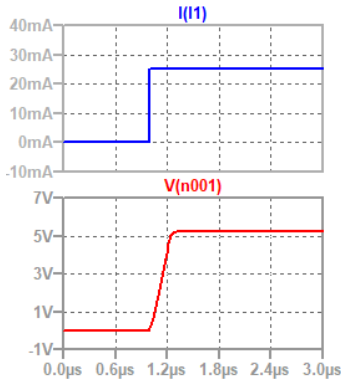


Fig. 3. Simulation result of the proposed measurement method.

C. Experiment results

A current-controlled gate driver is designed to investigate the behaviour of the MOSFET via the proposed method. The diagram of the experimental setup is presented in Fig.4. The step current signal is programmed and stored in the DSP controller. The signal is transmitted to a Digital-to-Analog Converter (DAC) via Serial Peripheral Interface (SPI) communication. The step signal is generated by the DAC and input into the current-controlled gate driver to control the gate current of the MOSFET. The details of the gate driver are demonstrated in [8]. It is worth noting that the magnitude of the step current signal can be changed according to the requirement of the test.

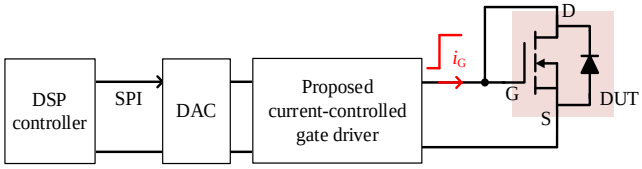


Fig. 4. Diagram of the experiment setup.

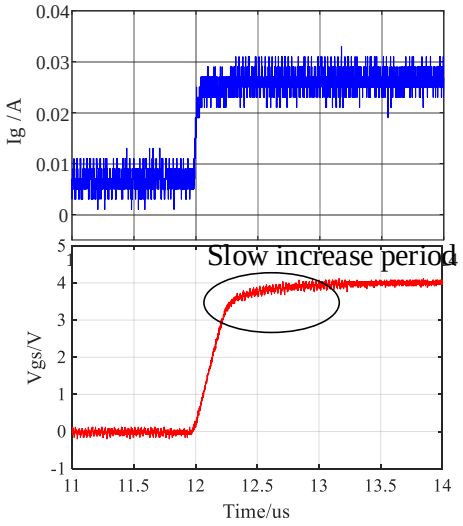


Fig. 5. Experiment result of the proposed measurement method.

The experiment result is different from the simulation. Fig.5 illustrates the test waveform of the MOSFET under the same condition as the simulation. The device under test is SCT3060, the magnitude of the step current signal is 25mA. Similar to the simulation result, there is also a charging process, where the gate voltage increase linearly in the beginning. However, after the linear increase period, there is a slow increase period, which is not presented in the simulation. Considering that the charging process of the gate capacitor is finished after the linear period, this slow increase period is introduced by the V_{th} shift.

D. Influence of Short-Time V_{th} Shift on Switching Transient

The short-time V_{th} shift phenomenon is can also be observed from the switching behaviour, which increases Miller plateau of the MOSFET.

Fig.6 shows the turn-on v_{gs} of SCT3060 at 250V/10A. It is demonstrated that the Miller plateau is not flat but increases slightly, which is different from the expectation of a flat Miller plateau. Comparing the practical result with the simulation waveform shown in Fig.7, it is obvious that the Miller plateau in the simulation is flat while the experiment waveform presents an increasing Miller plateau. The increasing Miller plateau is supposed to be introduced by the short-time V_{th} shift. This phenomenon also illustrates that the V_{th} shift happens so fast that it presents influences on the turn-on gate voltage waveform. The influences on the switching loss and other performances require further investigation.

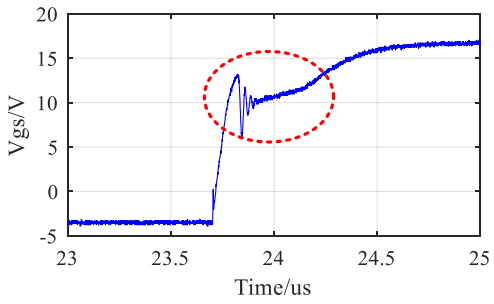


Fig. 6. Experiment waveform of the gate voltage during turn-on transient.

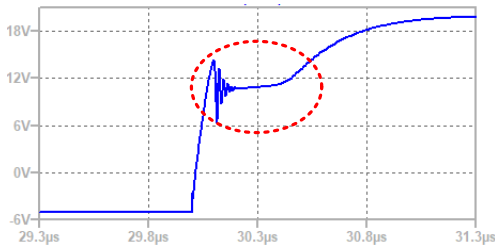


Fig. 7. Simulation waveform of the gate voltage during turn-on transient.

E. Modification of Pspice Model

It is stated that the provided Pspice model of the device under test has not included the effect of V_{th} shift, introducing the difference in the simulation results. By modifying the Pspice model, the simulation can also presents the increasing Miller plateau as shown in Fig.8. The equivalent circuit of the MOSFET can be built based on the code of Pspice model. Fig. 9 demonstrates the modified Pspice model where an additional voltage source VS1 is used to simulate the effect of short-time V_{th} shift. The equation of the VS1 is presented in the following section. The left part of the circuit is to simulate the output characteristics of the MOSFET, while the right circuit is to simulate the control of the gate signal. The increase on gate voltage is therefore presented in the turn on transient. Simulation is conducted under the same condition as in Fig. 7. Comparing the simulation results before (Fig.7) and after (Fig.8) the simulation, it is shown that the modified Pspice model presents the slow increasing Miller plateau as the experimental results (Fig.6).

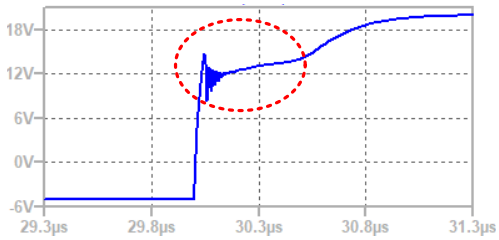


Fig. 8. Short-time V_{th} shift process in a linear time axis.

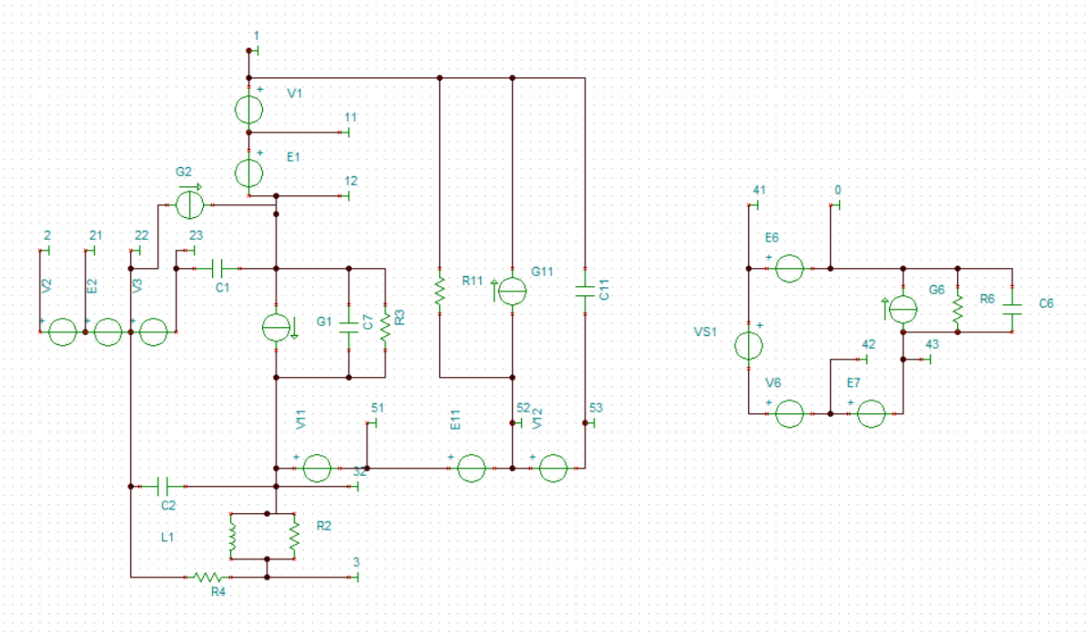


Fig. 9. Modified equivalent circuit of the MOSFET Pspice model considering short time V_{th} shift.

IV. Investigation into Short-Time V_{TH} Shift

A. Modelling of Short-Time Vth Shift

The short-time V_{th} shift can be modelled using the curve fitting tool. Fig.10 illustrates the zoomed-in details of the slow increase period of the gate voltage when the gate current is 70mA.

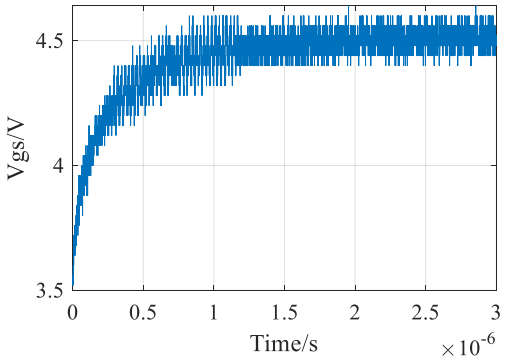


Fig. 10. Short-time V_{th} shift process in a linear time axis.

The time interval selected under investigation is the first 3μs after the linear increase process. It is shown that the gate voltage increases from 3.5V to 4.5V in the first 1μs, and then stays at 4.5V. If the time axis is transformed from the linear axis into the logarithm axis as shown in Fig.11, there is a linear relationship between the short-time V_{th} shift and the logarithm of time that can be obtained.

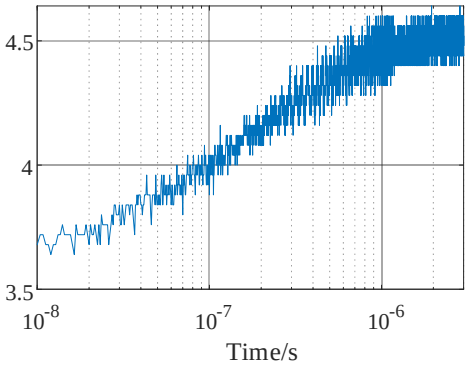


Fig. 11. Short-time V_{th} shift process in a logarithm time axis.

The quantitative relationship can be analyzed using the curve fitting tool. The equation used to model the process is presented in (1):

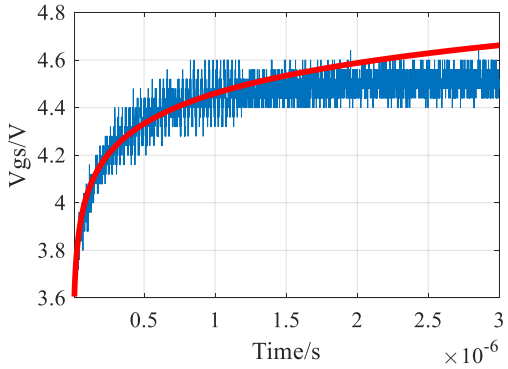
$$V_{th} = K \cdot \ln t + B \tag{1}$$

where t is the positive bias time of the MOSFET, V_{th} is the threshold voltage, K and B are two parameters that describe the shifting process. It is worth noting that this model can only describe the shifting process in a certain time range (10ns to 1us). The parameter B represents the initial value, while K reflects the shift speed. A higher K results in a larger shift in the same stressed time.

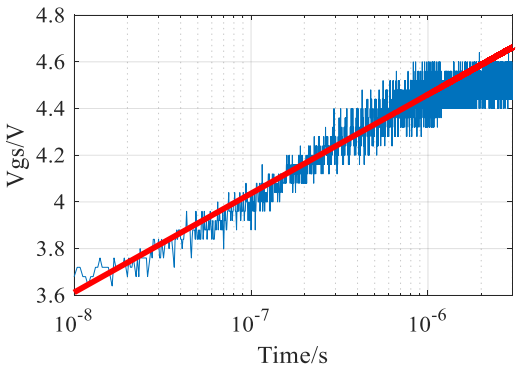
The experiment waveform is fitted using the equation, the result is shown in (2):

$$V_{th} = 0.184 \cdot \ln t + 7.002 \tag{2}$$

Fig.12 demonstrates the curve fitting results of the proposed logarithm model. The blue waveform is the measured V_{gs}, while the red curve is the calculated mathematic relation between V_{th} and the gate stress time. It is shown that in the first 1μs V_{th} shifts, the logarithm model can be used to describe the short time shift of V_{th} under the gate stress.



(a) Linear time axis



(b) Logarithm time axis

Fig. 12. Curve fitting result of V_{gs} in the slow increase period: (a) linear time axis; (b) logarithm time axis.

B. Short-Time Vth Shift as Temperature Sensitive Electrical Parameters (TSEP)

As is stated that the parameter K in equation (1) reflects the shift speed of the short-time V_{th} shift, which is also the speed for electrons to be trapped inside the oxide in Fig.1(d). The behaviour of electrons is influenced by the temperature, therefore, it is supposed that the parameter K is influenced by temperature.

Fig.13 presents the influence of the temperature on the electrical field in the gate oxide. In the condition of higher temperature, the electrons required for the inversion layer are less than at lower temperature [11]-[15]. The decrease of the charges in the inversion layer reduces the electrical field. Therefore, it is expected that the slope rate of the short-time V_{th} shift is reduced at a higher temperature.

Experiments are conducted under different temperatures to verify the above analysis. The gate current used in the measurement is 70mA. The gate voltage waveforms in different temperature of the device under test are captured and evaluated using the logarithm model. Thereby, the relation between the slope of the short-time V_{th} shift and the temperature can be obtained, which is presented in Fig. 14. The negative correlation verified the analysis based on the proposed model. It is worth noting that the measured V_{th} (the gate voltage in the steady state in Fig.2(b).) after short time shift period is reduced from 4.64V to 4.11V along with the

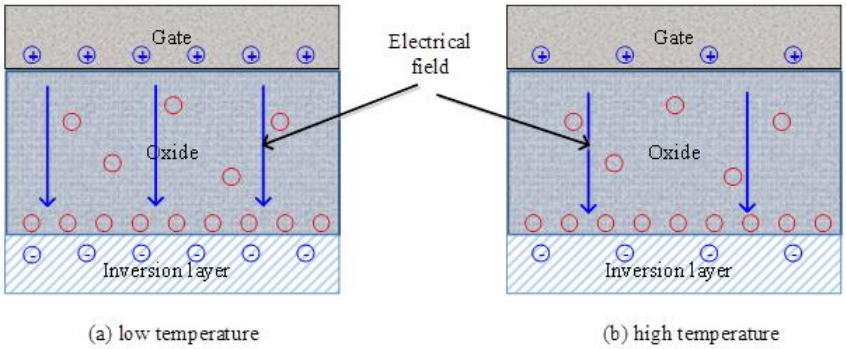


Fig. 13. Influence of temperature on the electrical field in the gate oxide.

increase of temperature as shown in Fig.15. It is concluded that the short-time V_{th} shift process can be used as an indicator for junction temperature.

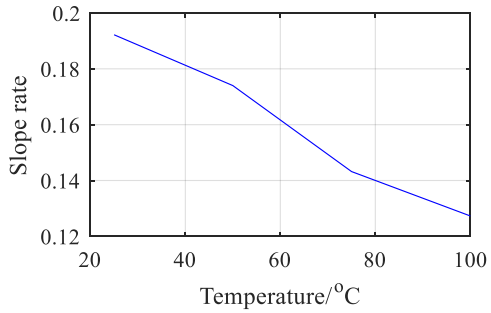


Fig. 14. Short-time V_{th} shift process in a linear time axis.

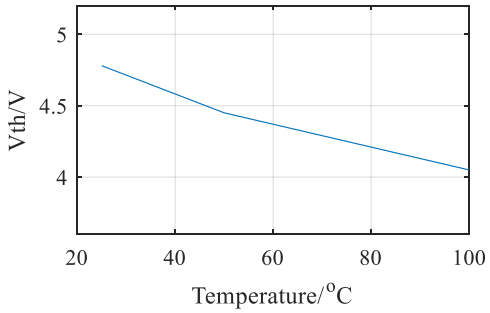


Fig. 15. Relation between V_{th} shift and the temperature.

V. Conclusion

This paper provides an investigation into the short-time V_{th} shift. The test circuit used to observe the short-time V_{th} shift is presented, whose experimental waveforms illustrate the V_{th} increase more than 0.5V in 1μs. Also, a Pspice the model of MOSFET has been developed which can reflect the short-time V_{th} shift effect. This process can be described and quantitated byusing a logarithm equation. In addition, the slope rate of the equation reflects the speed of the short-time V_{th} shift, which can be used to estimate the junction temperature as a TSEP. At last, the linear relationship of the slope rate and temperature is verified in the experiments.

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