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An Improved DC Circuit Breaker Topology Capable of Efficient Current Breaking and Regeneration

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***Abstract*—The DC power system, due to its convenience of conversion, integration, and use, is getting immense attention in the field of power transmission and distribution. It is superior to traditional AC systems in terms of efficiency, reliability, and control simplicity as well. A DC circuit breaker is one of the important elements of any DC power system. It is a sophisticated technology designed to break DC current only. The breaking of a DC current is always challenging compared to the breaking of an AC current, as DC current does not have natural zero crossing points like AC current has. Moreover, DC current breaking becomes more critical when the current is inductive as energy stored in the network inductance opposes instantaneous current breaking. Hence, this energy needs to be absorbed and dissipated as heat during the current breaking operation, which is exactly what is done in the traditional DC circuit breaker topologies. This paper introduces a new topology for DC circuit breakers with a mechanism to reuse this stored energy instead of dissipating it. The mechanism is analogous to regenerative braking in electric drive systems and can enhance the overall system efficiency. The proposed scheme was analyzed through rigorous computer simulation and was experimentally validated.**

***Keywords*—DC circuit breaker, regeneration, current breaking**

I. INTRODUCTION

DC power system has demonstrated its superiority over AC systems in many ways, e.g. in terms of reliability, efficiency, control simplicity, integration of Distributed Energy Resources (DERs), and connection of loads etc., and dealing with DC power systems has become significantly easier thanks to the continuous development of power electronics. DC microgrid concept is becoming more popular for remote area electrification and HVDC transmission has already outclassed the traditional AC transmission in almost all aspects. In addition, the concept of the HVDC grid system is also gaining ground and, may be, in the near future, the HVDC grid will be the best alternative to the traditional HVAC grid system [1]. Despite these numerous advantages, there are still significant challenges in designing appropriate DC switchgear equipment. A DC Circuit Breaker (DCCB) is one such critical switchgear equipment that plays a crucial role not only during interrupting fault currents but also during normal load switching.

In order to break current in a network, Circuit Breakers (CBs) are used. Circuit breakers usually make a break in the current path by separating the breaker contacts mechanically or by a solid state turn off process. In the mechanical turn off process, as the contacts separate, an arc is initiated between them, and this arc needs to be extinguished quickly to break the current efficiently as well as to keep the contacts undamaged. In an AC network, due to the sinusoidal nature of the current, a natural current zero situation arises twice in a full cycle. Using different arc extinguishing techniques, AC circuit breakers usually break the current at current zero instances [2]–[4]. This process of current breaking is quite straightforward in AC network, but in a DC network it is not that simple. Natural current zero is not available in DC current and that makes the AC circuit breaker unsuitable for the breaking of DC current. Furthermore, a DC network tends to offer significant network inductance as the converters acting as DC sources use inductance for many reasons, such as for current smoothening, for filtering, for emulating current sources etc. In addition to that, reactors are also used to limit the fault current in DC networks. As a whole, the DC network consists of significant inductances that store energy while current flows through it. Breaking current in this type of network becomes more challenging as this stored energy creates high potential stress across the breaker contacts, creates and maintains an arc for a longer period of time and damages the contacts in the process.

Similarly, in the solid state turn off process, sudden cessation of current flow in an inductive DC network will cause high potential stress across the device and may damage it. Hence, for safe and efficient breaking of DC current, it must be reduced to zero and the stored energy of the network must be absorbed and dissipated during the process. Snubber networks or nonlinear resistors or a combination of them are used as absorber elements in the conventional DCCB topologies to absorb and dissipate that energy as heat and to assist in current reduction [5], [6]. This conventional current breaking process is almost analogous to the obsolete dynamic breaking once used in electrical drives, where a running motor is slowed down by forcing the motor to run as a generator, converting the rotor kinetic energy into electrical energy and then dissipating this electrical energy as heat in a resistor. But this wastage of energy does not make sense and, hence, regenerative braking comes into play to reuse this energy to be fed back to the source instead of dissipating it and making the overall system much more efficient. Inspired by a similar concept, a new DCCB topology is proposed in this paper that ensures efficient current breaking without dissipating any energy and can regenerate energy to feed it back to the source, much like the regenerative braking in electrical drives does. The structure of this paper is as follows: Section II reviews the literature on conventional DC circuit breakers. Section III introduces and discusses the new DCCB topology. The mathematical model and working principles of the proposed topology are thoroughly discussed. Section IV presents the simulation and experimental results and thus validates the proposed concept.

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II. REVIEW OF DC CIRCUIT BREAKERS

This section gives a brief overview of conventional DCCB topologies and later discusses the hybrid DCCB topologies in detail and finally formulates the problem statement. DC circuit breakers are basically divided into the following four categories:

1) Mechanical Circuit Breaker: Mechanical Circuit Breakers (MCB) are similar to traditional mechanical switches and are composed of three main parts, including a mechanical switch, a commutation circuit, and a Metal Oxide Varistor (MOV) as a voltage limiter device. The scheme of a typical MCB is shown in Fig. 1 (a). Both the commutation circuit and the MOV act as the absorber element during current breaking. Due to the limited current interruption capability and slow operating speed, this topology has fewer prospects in the wider application areas [7], [8].

2) Solid-State Circuit Breaker: Solid-State Circuit Breakers (SSCB) perform current interruption by power electronic devices such as thyristor, GTO, IGCT, and IGBT etc. A MOV is used in parallel with the switching device to limit the voltage surge during current interruption and, by doing that, it dissipates the energy stored in the network inductance [9], [10]. Typical SSCB is shown in Fig.1 (b). Some upgraded versions of SSCB, such as active thyristor-based DCCB [11], SSCB with self-adaptive fault current limiting capability [12], self-powered SSCB with fault current limiter [13] etc., are proposed. Though SSCBs are faster in response, they cause higher conduction loss and do not provide galvanic isolation.

3) Z-Source Circuit Breaker: The Z-Source Circuit Breaker (ZSCB) is an upgraded version of the solid-state topology. A scheme of the original ZSCB is shown in Fig. 1 (c). One of the major benefits of the ZSCB is that it is self-operative, meaning that once a short circuit fault occurs on the load side, the breaker trips automatically without the need for a tripping signal from the protective relay. A damping resistor functions as an absorber element. Some modified versions, such as bidirectional ZSCB based on series or parallel connection, bidirectional ZSCB based on coupled inductors, and a few active ZSCB topologies are also proposed in [14], [15]. Though ZSCB provides automatic and faster operation, it often fails to self trip under highly inductive fault current and also dissipates energy as heat as usual, just like the other topologies do.

4) Hybrid Circuit Breaker: The Hybrid Circuit Breaker (HCB) is a new class of DCCB that combines both the MCB and the SSCB to take advantage of both and is the most prominent technology as of now. A typical HCB has three main parts, including a Fast Mechanical Switch (FMS), IGBTs as the Main Breaker (MB) unit, and a MOV as shown in Fig. 1 (d). When a trip command is received, the FMS opens and sends a turn-on signal to the MB. Due to the arc voltage across the FMS, current I_S shifts naturally from the FMS to the MB. Once the FMS opens completely and gains sufficient breakdown strength, the MB is turned off, ceasing the flow of current I_{IGBT}. The voltage surge induced due to this current chopping is clamped by the MOV while the stored energy of network inductance is dissipated through it. A Current Limiting Reactor (CLR) and a Residual Current Breaker (RCB) are used respectively to limit fault current and to provide galvanic isolation [16].

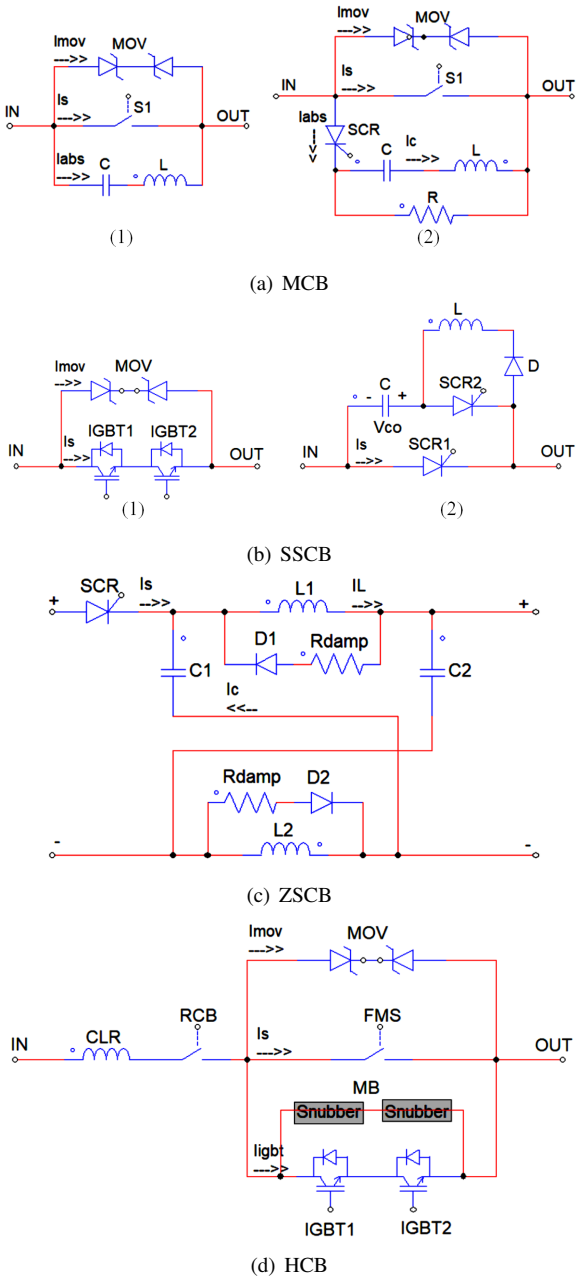

Fig. 1. Conventional DCCB Topologies

A substantial number of studies have been done on HCB technology and new versions such as vacuum interrupter based HCB [17], current flow controlling HCB [18], thyristor full-bridge-based HCB [19], HCB based on series connected thyristors and IGBT half-bridge submodules [20], superconductor based HCB [21], Multiport HCB [22], Gas Discharge Tube (GDT) based HCB [23] etc. have been proposed. HCB topology has a wider application area and is the best fit for high voltage, high current applications. Though HCB possesses better current interruption capability and also provides galvanic isolation, it is very expensive with a complex architecture. And, of course, like any other topology, it also dissipates energy in the MOV and snubber network during current interruption.

A. Problem Statement

The current breaking mechanism in the existing topologies uses lossy impedance networks like RLC network or RC snubber or nonlinear resistors like MOV or a combination of them as an absorber circuit to absorb and dissipate the stored

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energy of the network as heat during current reduction. Hence, energy is wasted in the conventional topologies during every current breaking operation. No matter how fast the breaker operates, the stored energy of the network inductance must be removed for successful current breaking. Since the energy stored in the network inductance is equal to $\frac{1}{2}LI^2$, the energy wastage might even become more significant in a high current or highly inductive DC network like DC microgrid, HVDC transmission, electric traction load etc., where the network inductance might range from several millihenry to hundreds of millihenry and the current may range from several hundred to thousands of amperes.

Although [24] proposed a new type of HCB based on a disconnector voltage control technique that can reduce peak current as well as energy wastage. And [25] proposed a LVDC HBD topology that was shown to dissipate less energy. But none of them can completely eliminate energy dissipation. Meanwhile, a new topology that can store the energy instead, and can feed it back to the source is proposed in [26]. It functions much like the regenerative braking in an electrical drive system works. But issues such as low energy recovery efficiency, spiky wave shape of regenerated current and power, network disturbance during regeneration etc. could not be resolved in that topology. Hence, an improved DCCB topology with higher energy regeneration capability, smoother regenerated current with less network disturbance is presented in this paper with simulation and experimental validation. This improved topology can save a lot of energy in a high current, highly inductive DC network and can improve the overall system performance. The detailed mathematical modeling and working principals of the proposed topology are discussed in the next section.

III. PROPOSED WORK

This section describes the construction of the proposed topology, discusses the mathematical modeling and working principles thoroughly, and presents the control algorithm for the proposed topology.

A. DCCB Construction

The proposed DCCB topology as shown in Fig. 2 is constructed based on the hybrid CB concept. The breaker is composed of both mechanical and solid-state components. The main branch contains two mechanical switches (S1 and S2), where S1 is a fast-operating switch and S2 is a normal switch. A MOV is connected across S1 to limit the voltage stress across it. The secondary branch, or the commutation circuit, consists of a thyristor T1, a capacitor C_1 and an inductor L. An IGBT, capacitors (C_1 & C_2), inductor L, diodes (D1 & D2) form the regenerating circuit. A freewheeling diode D3 is attached across the output terminals of the breaker to freewheel load current if the load is inductive in nature. It is to be noted, however, that this topology focuses on regenerating energy from the source inductance only. Hence, the energy stored in the load inductance is allowed to freewheel through D3.

B. Working Principal

1) Current Breaking: When the CB is on, both the mechanical switches S2 and S1 remain closed and current $i_s(t) = i_{LOAD}(t) = I_0$ flows through the network as shown in

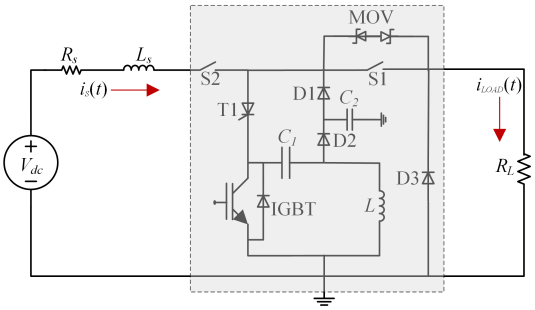

Fig. 2. Proposed DCCB Topology

Fig. 3 (a). At this moment, the source inductance L_S becomes energized by this current. Once the CB receives a trip signal at an instant, $t = t_o$; the fast-operating switch S1 opens quickly and simultaneously gate pulses are sent to the thyristor T1. As the switch S1 opens, an arc voltage is initiated which forces the source current to divert from the main branch to the secondary branch as shown in Fig. 3 (b). At this point, the secondary branch, along with the source network, forms a series resonant circuit which generates a growing current oscillation at its resonant frequency. This growing current diverts the main branch current completely, and thus the arc voltage cannot go very high and the arc is extinguished very quickly. As the source current is diverted, the load becomes isolated from the source network and the load current reduces to zero or freewheels to zero through D3. Now, the current oscillation is governed by (1).

$$L'\frac{di_s(t)}{dt} + R_s i_s(t) + \frac{1}{C_1}\int i_s(t)\,dt = V_{dc}, i_s(t = t_o) = I_o \tag{1}$$

where, V_{dc}= DC source voltage, L_s= source inductance, R_s= source resistance, $i_s(t)$= source current, I_o= source current before tripping initiates, L= breaker inductance, C_1= breaker capacitance, and $L' = L_S + L$. It is to be noted, however, that the average current drawn by the capacitor C_2 in steady state is very negligible. Hence, the current drawn by it is assumed to be zero for simplicity of analysis, and accordingly, the current path is shown in Fig. 3 (b) and the mathematical modeling is done. Now, the solution to (1), i.e., the current response, can be written as follows:

$$i_s(t) = e^{-\alpha t}\ (A\ cos\ \beta t + B\ sin\ \beta t) \tag{2}$$

where, $\alpha = \frac{R_s}{2L'}$ is the damping factor, $\omega_r = \frac{1}{\sqrt{L'C_1}}$ is the resonance frequency, $\beta = \sqrt{\omega_r^2 - \alpha^2}$ is the ringing frequency provided that $\omega_r > \alpha$, $A = I_o$ and $B = \frac{V_{dc} - I_o R_s}{\beta L'} + \frac{\alpha I_o}{\beta}$. Equation (2) can be further simplified as follows:

$$i_s(t) = e^{-\alpha t}\ C\ cos\ (\beta t - \phi) \tag{3}$$

where, $C = \sqrt{A^2 + B^2}$ and $\phi = \tan^{-1}\frac{B}{A}$. Equation (3) is an under damped oscillation which eventually decays to zero, but at the first zero-crossing point of this oscillating current, the thyristor T1 turns off by natural commutation, accomplishing a successful current breaking. The first zero crossing point as well as the apparent current breaking time $T_{trip}\prime$ can be found by solving (3) for $i_s(t = T_{trip}\prime) = 0$. Then, taking the switching delay (T_{OFF}) of S1 into account, the actual current breaking time T_{trip} is calculated as follows:

$$T_{trip} = T_{trip}\prime + T_{OFF} = \frac{1}{\beta}(\frac{\pi}{2} + \phi) + T_{OFF} \tag{4}$$

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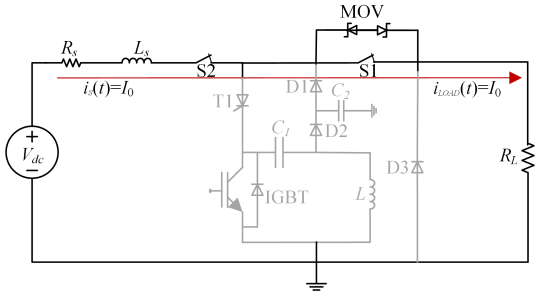
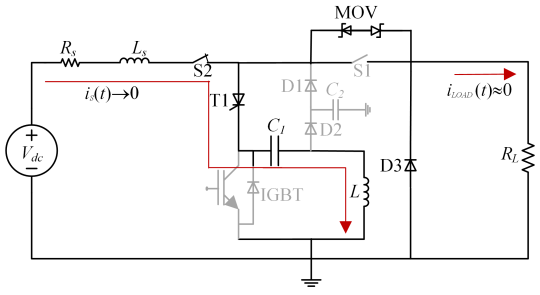


(a) Source current path before tripping initiated



(b) Source current path after tripping initiated

Fig. 3. Current breaking in the proposed DCCB topology

The higher the β, the faster is the current breaking. The capacitor C_1 on the other hand, is being charged as source current flows through it. When the source current stops, C_1 remains charged up to V_{co}. Now, the equation for capacitor voltage $v_{c_1}(t)$ can be derived from (3) as $v_{c_1}(t) = \frac{1}{C_1}\int i_s(t)\,dt$ and by solving it for $v_{c_1}(t = T_{trip}\prime) = V_{co}$, the final capacitor voltage is found as follows:

$$V_{co} = D(cos\ (-\phi + \phi') + e^{-\alpha T_{trip}\prime} sin\ \phi') \tag{5}$$

where, $D = \frac{1}{C_1}\sqrt{\frac{A^2+B^2}{\alpha^2+\beta^2}}$ and $\phi' = \tan^{-1}\frac{\beta}{\alpha}$. Now, the charged capacitor holds energy as (6) where, E_S is the energy released from the source during the tripping interval, E_{LOAD} is the energy leaked to the load due to the switching delay of S1 and E_{c_1} is the energy stored in C_1.

$$E_{c_1} \approx E_S - E_{LOAD} \tag{6}$$

Though E_S contains energy from both the source inductance and the voltage source itself, the main contributor to E_S is the stored energy $\frac{1}{2}L_sI_o^2$ from the source inductance, which is usually wasted in the conventional topologies but is stored in the capacitor in the proposed scheme. Equation (6) can be rewritten as (7) where $I_{s_{(avg)}}$ is the average source current during T_{trip}.

$$E_{c_1} \approx \frac{1}{2}L_sI_o^2 + (V_{dc}I_{s_{(avg)}} - I_{s_{(avg)}}^2R_s)T_{trip} - (V_{dc}I_o - I_o^2R_s)T_{OFF} \tag{7}$$

C. Current Regeneration

Once the source current becomes zero, the CB initiates the regeneration sequence. The IGBT turns on and the capacitor C_1 discharges through the inductor L, and thus the stored energy of the capacitor is transferred to the inductor as shown in Fig. 4 (a). The discharging of the capacitor to the inductor is governed by (8), whose solution is (9) where, $i_r(t)$= regenerated current and $\omega_r' = \frac{1}{\sqrt{LC_1}}$ is the resonant frequency.

$$L\frac{di_r(t)}{dt} + \frac{1}{C_1}\int i_r(t)\,dt = 0, i_r(t=0) = 0, V_{c_1}(t=0) = V_{co} \tag{8}$$

$$i_r(t) = V_{co}\sqrt{\frac{C_1}{L}} sin\ \omega_r' t) \tag{9}$$

But instead of a continuous turn on signal, a PWM switching signal of a specific duty cycle and frequency (d & f) is applied to the IGBT gate terminal to regulate the current and the energy flow. During every switching interval of the PWM signal, when the IGBT turns off, the inductor L releases energy towards the source through diodes (D1 & D2) as shown in Fig. 4 (b). Capacitor C_2, smooths out the regenerated current, and in order to ensure smooth regenerated current, it has to be in continuous conduction mode (CCM). Now, the equivalent circuit during the regeneration operation, as shown in Fig. 4 (b) resembles a buck-boost converter topology whose frequency requirement can be found from (10) and (11) where $I_{R(average)}$ is the average regenerated current and ΔI_r is the ripple in inductor current.

$$C_2 = \frac{I_{R(average)}d}{\Delta V_{c_2} f} \tag{10}$$

$$L = \frac{V_{c_1}d}{\Delta I_r f} \tag{11}$$

The transfer of energy from the inductor to the source defined as regeneration is governed by (12) and its solution is (13), where, I_{ro}= inductor current when the IGBT turns off during the PWM interval.

$$(L_s + L)\frac{di_s(t)}{dt} + R_s i_s(t) = V_{dc}, i_s(t=0) = -I_{ro} \tag{12}$$

$$i_r(t) = -I_{ro}e^{-\frac{R_s}{L_s+L}t} + \frac{V_{dc}}{R_s}(1 - e^{-\frac{R_s}{L_s+L}t}) \tag{13}$$

The average regenerated current is given by (14) where, T_R= duration of regeneration. To avoid voltage disturbance during injection of regenerated current, the current magnitude should be kept low and the wave shape should be as flat as possible. This is achieved by increasing the duration of the regenerated current through PWM duty cycle adjustment. The lower the duty cycle, the longer is the duration.

$$I_{R(average)} = \frac{1}{T_R}\int_0^{T_R} i_r(t)dt \tag{14}$$

Once the capacitor C_1 is completely discharged and the capacitor voltage becomes sufficiently low, the PWM signal stops and the control system waits for the residual regenerated current to become zero. Once the residual current becomes zero, switch S2 turns off and the breaker resets for the next operation. A control algorithm developed based on the above discussion generates the different control and switching signals for the CB operation.

D. Design Approach

This subsection presents the design guidelines for the proposed CB construction and also gives an insight into its scalability. As the proposed topology is network specific, the network particulars need to be known for calculating CB parameters. For simplicity, a DC source with a source

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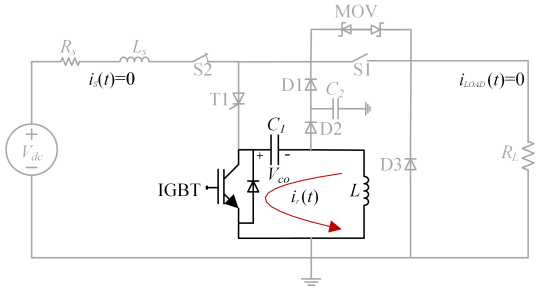
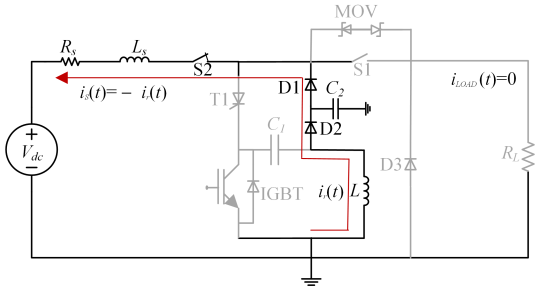


(a) Capacitor transfers energy to the inductor



(b) Inductor releases energy to the source network

Fig. 4. Current regeneration in the proposed DCCB topology

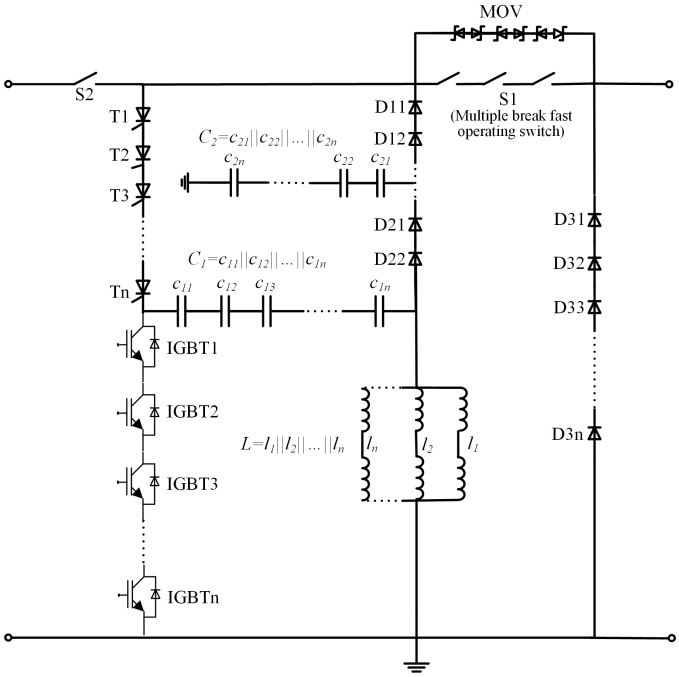


Fig. 5. Design approach for high voltage application

resistance and inductance was considered as the equivalent of a DC power system with the following network particulars as mentioned in TABLE I. The network particulars for simulation were chosen based on the studies [27]–[29] with a little modification so that it becomes a high current network with moderate network inductance. The experimental setup was designed as a 200 V, 1 A DC power system depending on the equipment ratings and available resources. The radial DC network as shown in Fig. 2 was used for simulation and experimental studies. Now, if the maximum fault current I_o, allowable maximum system voltage V_{max}, and allowable maximum tripping time T_{max} of a network are known, then by setting $V_{co} < V_{max}$ and $T_{trip} < T_{max}$, equation (4) and (5) can be rearranged as follows:

$$\frac{1}{\beta}(\frac{\pi}{2} + \phi) + T_{OFF} < T_{max} \tag{15}$$

$$D(cos\ (-\phi + \phi') + e^{-\alpha T_{trip}'} sin\ \phi') < V_{max} \tag{16}$$

When the values of $\alpha, \beta, \omega_r, \phi, \phi', A, B, C, D$ are entered into (15) and (16), the only unknown variables remain L and C_1. Using the numerical solution method, these two parameters can be calculated by successive iteration. Then the PWM frequency is chosen based on the limitations of the control system. Once the frequency is chosen, and the values of average regenerated current, ripple in inductor current and allowable voltage variation across C_2 are set, (10) and (11) can lead to the selection of C_2 and d. Finally, the ratings of the different devices and components used in the circuit breaker were chosen based on the network particulars and are presented in TABLE II. A prototype of the proposed topology was built using Lab Volt modules to demonstrate its current breaking and regenerative action. As the current rating of the experimental setup was limited to 1 A, the network inductance was chosen as high as possible to demonstrate the robustness of the prototype, and then depending on the network particulars, the breaker parameters were selected. An Arduino UNO microcontroller board was used as the main control unit for generating the control and switching signals for the prototype. Though the proposed topology is network specific, it is largely scalable and can be designed for any network application. The breaker parameters can be calculated in line with the above discussion, whereas the ratings can be chosen based on network requirements. Such a design approach for high voltage applications is shown in Fig. 5 where the devices and capacitors are connected in series to meet the high voltage requirement, whereas the inductances are connected in parallel to meet the high current requirement. The performance of the newly proposed topology is evaluated in the following section through computer simulation and experimentation.

TABLE I
NETWORK PARTICULARS

PARAMETERS	SIMULATION	EXPERIMTN.
DC voltage (V_{dc})	400 V	200 V
Source inductance (L_s)	200 mH	2.6 H
Source resistance (R_s)	0.1 Ω	20 Ω
Load resistance (R_L)	0.9 Ω	180 Ω
Maximum network current ($I_S = I_o$)	400 A	1 A
Maximum tripping time (T_{max})	50 ms	50 ms
Maximum system voltage (V_{max})	5000 V	500 V

IV. RESULTS

This section discusses the results of simulation and experimental studies. It is to be noted that all the parameters, i.e., voltage, current, power, etc., referred to the source were measured at the input terminal of the CB, while those referred to the load were measured at the output terminal of the CB. DCCB performance indicators such as current breaking time, conduction loss, voltage stress on the breaker, energy recovery efficiency, voltage disturbance in the network etc. were thoroughly investigated and evaluated based on the results.

A. Simulation

The proposed DCCB topology was modeled and simulated in PSIM software. The PSIM simulation model is shown in

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TABLE II
DESIGN PARAMETERS

DEVICES	PARAMETERS	VALUES FOR SIMULATION	VALUES FOR EXPERIMTN.
IGBT	Maximum Blocking Voltage	5 kV	690 V
	Maximum Current	400 A	1.5 A
	Saturation Voltage	1.8 V	1.5 V
	On State Resistance	0.5 Ω	0.4 Ω
	Diode Threshold Voltage	1.7 V	1.3 V
	Diode Resistance	0.5 Ω	0.35 Ω
Thyristor	Maximum Blocking Voltage	5 kV	1200 V
	Maximum Current	400 A	1 A
	Voltage Drop	1 V	0.8 V
	Holding Current	5 mA	2 mA
	Latching Current	10 mA	2 mA
Diode	Maximum Reverse Blocking Voltage	5 kV	1200 V
	Maximum Current	400 A	1 A
	Diode Threshold Voltage	0.8 V	0.7 V
	Diode Resistance	0.5 Ω	0.3 Ω
MOV	Breakdown Voltage	5 kV	500 V
	Equivalent Series Resistance	0.04 Ω	0.06 Ω
	Energy Withstand. Capacity	266 kJ/s	1.6 kJ/s
Mechanical Switch (S1 & S2)	Maximum Voltage	5 kV	500 V
	Maximum Current	400 A	3 A
	Turn on Time	15 ms	20 ms
	Turn off Time	15 ms	20 ms
Breaker Parameters	Capacitance (C_1)	2000 μF	50 μF
	Capacitance (C_2)	200 μF	25 μF
	Inductance (L)	5 mH	325 mH
	PWM frequency (f)	2 kHz	980 Hz
	PWM duty cycle (d)	20%	30%

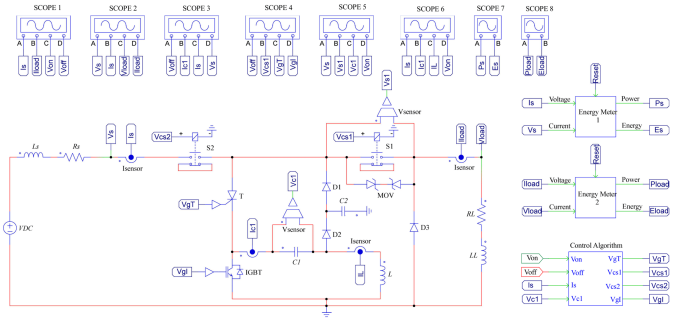

Fig. 6. PSIM simulation model

Fig. 6. The following two subsections describe the current breaking and current regeneration characteristics of the proposed topology based on simulation results.

1) Current Breaking: The DCCB turns ON at $t = 0.277$ s upon receiving a closing pulse and the load current rises and reaches 400 A as shown in Fig. 7 (a) and (b). A trip signal received at $t = 8.77$ s initiates the breaker tripping process. Hence, the main contact S1 opens and the thyristor T1 turns ON, as discussed earlier. This action results in shifting the source current into the secondary branch, which creates current oscillation due to resonance as shown in Fig. 7 (c) and (d). The corresponding control signals are shown in Fig. 7 (k), (l) and (m). As the source current is diverted, the load becomes isolated from the source network and, hence, the load current reduces to zero quickly as shown in Fig. 7 (b). Meanwhile, in the secondary branch, T1 turns off at the first zero crossing point of the source current oscillation, and thus the current breaking is accomplished. The transient moment of the breaking of source current and load current is shown in Fig. 8 (a) and (b), where the source current breaking time is measured as 45.85 ms while the load current breaking time is found to be 15.18 ms. The source current breaking time is considered as the characteristic current breaking time of the DCCB in this study. Fig. 8 (c) and (d) demonstrate the shifting of source current from the main branch into the secondary branch and the creation of zero crossing point. The capacitor C_1 charges as the current flows through the secondary branch and approaches zero. The voltage across S1 and the capacitor voltage are shown in Fig. 7 (g) and (h). As shown in Fig. 7 (e), the diversion and reduction of the source current induces a transient voltage surge due to high di/dt. This surge voltage is clipped off by the MOV and quickly settles down to the nominal supply voltage followed by a slight fluctuation during regeneration. A power surge caused by sudden energy released from the source inductance is visible in Fig. 7 (i) and this is the energy which is usually wasted in the conventional topologies.

2) Current Regeneration: Once the source current is reduced to zero and the thyristor T1 turns OFF, the CB becomes ready for the regeneration sequence. The energy stored within the capacitor C_1 needs to be transferred smoothly towards the source. For this to happen, the stored energy of the capacitor is converted into pulsed current by turning on the IGBT at a 2 kHz PWM signal under a 20% duty cycle as shown in Fig. 7 (j). The discharging pulsed current as shown in Fig. 8 (c) becomes smooth through the inductor L as shown in Fig. 8 (d), and each time the IGBT turns OFF during the PWM cycle, the inductor L forces the current towards the source through D1 and D2. Capacitor C_2 smooths out the injected current further, and the smoothed regenerated current is shown in Fig. 8 (a) with a peak value (magnitude) of -188.16 A and an average value of -120.88 A. The magnitude of the regenerated current depends on the PWM duty cycle. A higher duty cycle causes higher magnitude with less regeneration duration. The source voltage, the voltage across S1 and the capacitor voltage during the injection of regenerated current are shown in Fig. 7 (e), (g) and (h). The regeneration continues as long as the capacitor holds charge, and the moment the capacitor is completely discharged, the PWM signal stops and the breaker control system waits for the residual regenerated current to become zero. Once the current becomes zero, the control system resets the breaker and gets ready for the next operation cycle. As can be seen from Fig. 8 (e), the energy content of the power surge during CB tripping is measured as $E_s = 20.98$ kJ out of which some fraction is leaked to the load due to delayed switching of S1. This leaked energy as shown in Fig. 8 (f) is measured as $E_{LOAD} = 1.87$ kJ. Fig. 8 (e) also shows that around -50.8 kW of average power with a peak value of -116.15 kW is regenerated from the breaking of the 400 A current. The amount of regenerated energy is measured as $E_R = 13.09$ kJ. Hence, the actual energy recovery efficiency achieved by this topology is calculated as $\eta = \frac{E_R}{E_s - E_{LOAD}} = 68.24\%$. The simulation results are summarized in TABLE III.

B. Experimentation

The experimental setup is shown in Fig. 9. All the experimental data was collected using the LabVolt Data Acquisition and Control Interface (DACI 9063-A) for plotting and analysis. One complete breaker operation cycle is shown in Fig. 10, which shows the current, voltage, and power responses along with the coordinated switching signals. The frequency and duty cycle of the PWM control signal were chosen as 980 Hz and 35% respectively, and the complete switching signals

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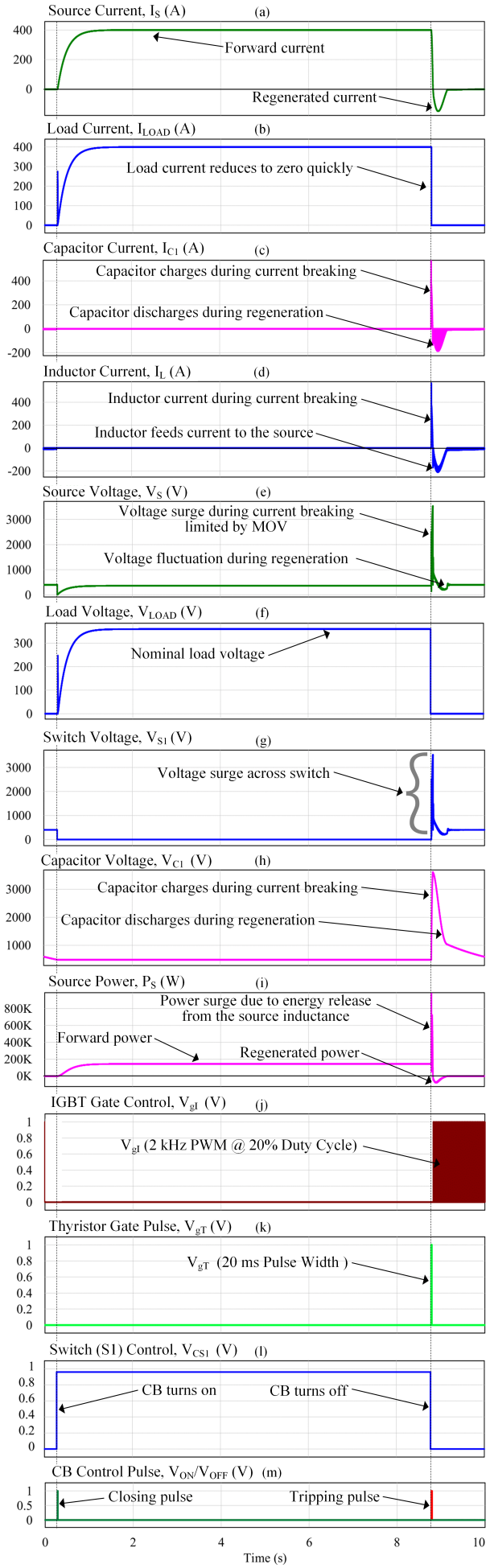

Fig. 7. Current and voltage responses synchronized with control signals during one complete operation cycle

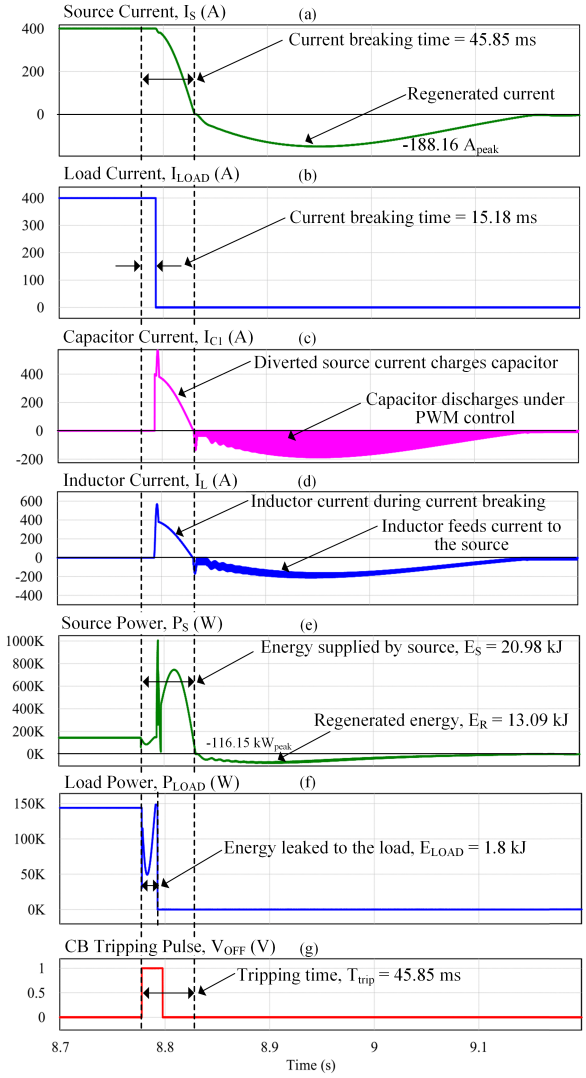

Fig. 8. Transient moment of current breaking and regeneration operation

TABLE III
SUMMARY OF SIMULATION AND EXPERIMENTAL RESULTS

INDICATORS	SIMULATION RESULTS	EXPERIMENTAL RESULTS
Current Breaking Time (T_{trip})	45.85 ms	38.9 ms
Regenerated Current (I_R)	-188.16 A (Peak) -120.88 A (Avg.)	-0.32 A (Peak) -0.21 A (Avg.)
Regenerated Power (P_R)	-116.15 kW (Peak) -50.80 kW (Avg.)	-71.24 W (Peak) -13.7 W (Avg.)
Regenerated Energy (E_R)	13.09 kJ	3.32 J
Energy Recovery Efficiency (η)	68.24%	82.79%

are shown in Fig. 10 (j), (k), (l) and (m). Fig. 10 (a) and (b) show the diversion and reduction of the source current and load current to zero. The shifting of source current from the main branch into the secondary branch is shown in Fig. 10 (c) and (d). The voltage responses of the source, switch S1 and the capacitor are shown in Fig. 10 (e), (g) and (h), which resemble the simulated responses. The transient responses of the breaker operation are shown in Fig. 11, where the source current breaking time is measured as 38.9 ms while the load current breaking time is approximately 22.48 ms. It is found from the experimental studies that the peak value of the regenerated current is -0.32 A with an average value of -0.21 A. Around -13.7 W of average power with a peak value of -71.24 W is regenerated from the breaking of 1 A current. The amount of regenerated energy is measured as $E_R = 3.32$ J. As can

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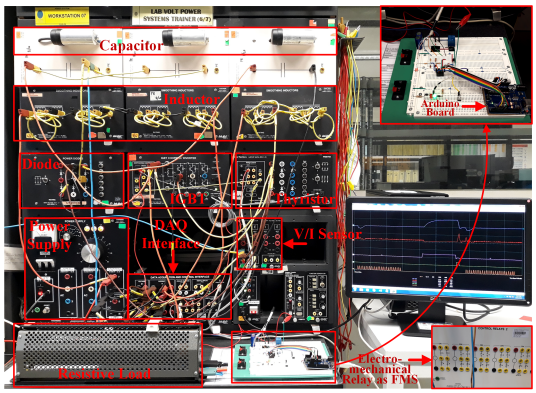

Fig. 9. Experimental set up

be seen from Fig. 11, the energy content of the power surge during CB tripping is measured as $E_s = 7.21$ J and the energy leaked to the load is measured as $E_{LOAD} = 3.2$ J. Hence, the energy recovery efficiency is calculated as $\eta = 82.79\%$, which is higher than the one achieved in the simulation studies and is caused by the higher PWM duty cycle e.g., 35%. The experimental results are summarized in TABLE III. It is noteworthy to mention that the voltage and current responses found in the experiment are quite similar to those found in the simulation, and thus the experimental results validate the mathematical modeling as well as the simulation results.

C. Performance Comparison

To compare the performance of the proposed topology, four conventional topologies, such as MCB, SSCB, ZSCB, and HCB, were simulated as well to evaluate their performance under similar network configurations. Breaker parameters were kept the same as those of the proposed topology for ease of comparison. Current breaking mechanisms of other modified topologies mostly rely on the snubber network or MOV and their operating characteristics are almost similar to these four in terms of energy dissipation. Hence, simulating those topologies is redundant. The current breaking characteristics of the conventional topologies along with the proposed one based on simulation studies are presented in Fig. 12. It is worthy to mention here that the ZSCB fails to trip under such a highly inductive network and requires higher values for the breaker parameter. Though the SSCB and HCB are very fast in operation, they cause hard switching of the solid state devices and their current breaking mechanism depends largely on the MOV. Contrary to that, the proposed topology provides soft switching by creating zero current switching and puts less stress on the components. However, the current breaking mechanism in the proposed scheme can be made faster by changing the breaker parameters. In terms of component count, the proposed topology is also quite reasonable. Apart from the regeneration, the proposed topology also provides galvanic isolation, negligible conduction loss and faster load isolation. The comparison of their performances is presented in TABLE IV which clearly shows the superiority of the proposed scheme.

To justify the scalability approach, the proposed topology was then simulated for higher voltage applications, starting from 1 kV up to 20 kV. Other network parameters were kept unchanged. To check the flexibility of the mathematical modeling, the breaker parameter, e.g., LC_1 was also changed. Performance parameters such as tripping time, energy recovery efficiency, voltage stress, etc. were evaluated against the voltage and parameter variations. Fig. 13 (a) shows the variation in tripping time with respect to the change in system voltage and breaker parameters. It is found that the tripping time does not depend on the system voltage, but it can be flexibly adjusted by changing LC_1. The lower the LC_1, the quicker the tripping time is. The energy recovery efficiency, on the other hand, is only slightly affected by the system voltage, but it varies significantly depending on LC_1, as shown in Fig. 13 (b). Higher efficiency can be achieved by higher value of LC_1. Hence, there is a trade off between the tripping time and

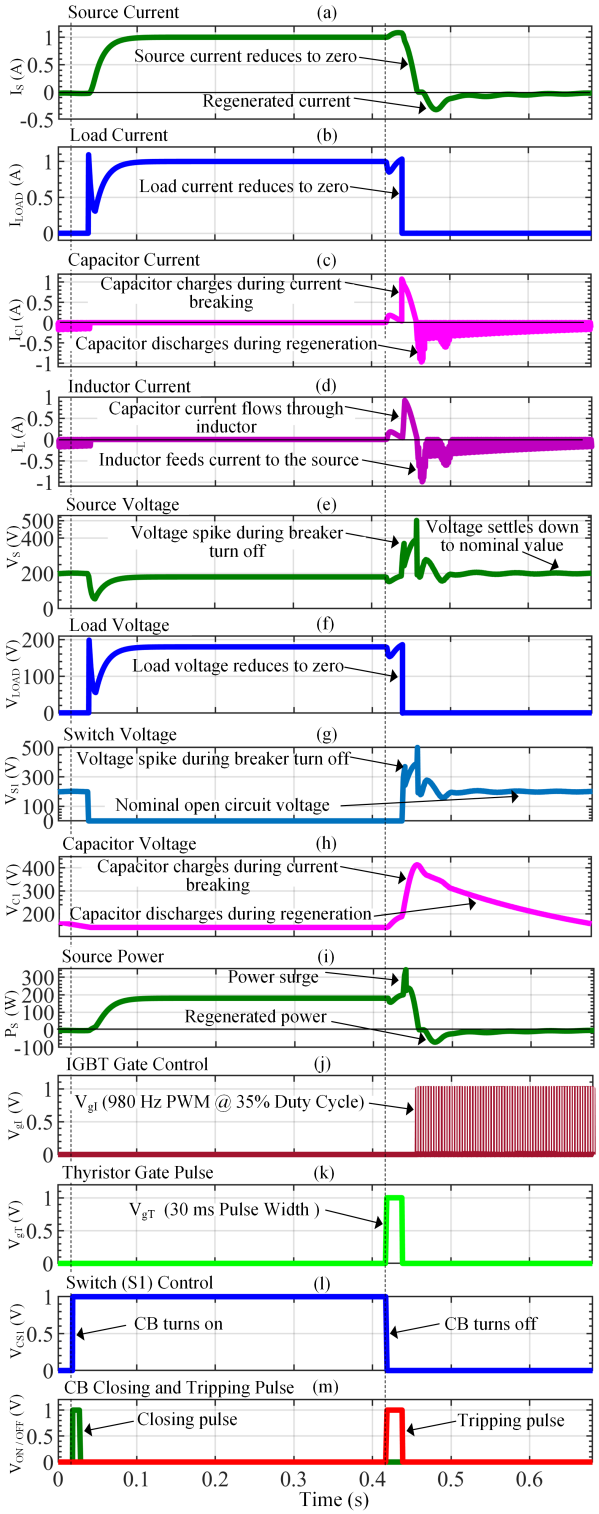

Fig. 10. Current and voltage responses synchronized with control signals during one complete operation cycle

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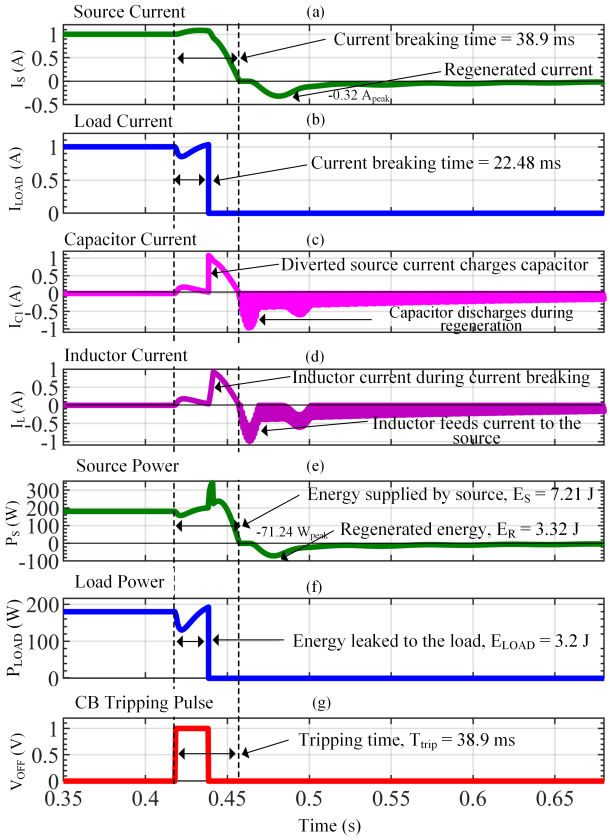

Fig. 11. Transient moment of current breaking and regeneration operation

TABLE IV
PERFORMANCE COMPARISON

	TOPOLOGY				
INDICATORS	MCB	SSCB	HCB	ZSCB	Proposed
Tripping time (ms)	48.11	17.33	32.56	*	45.85
Load current breaking time (ms)	48.11	17.33	32.56	*	15.18
On-state loss (kW)	0	16.55	0	1.15	0
Voltage stress (kV)	5.02	5.01	5.01	*	4.27
Energy recovery efficiency (η)	0	0	0	0	68.24%
Galvanic isolation	Yes	No	Yes	No	Yes
Component count	9	10	6	9	11
Mechanism	**CC	**CC	**CC	**CCB	**RC
References	[8]	[12]	[17]	[15]	

*Fails to trip in highly inductive network. Requires higher values for CB parameter.

**CC: Conventional Commutation, RC: Resonant Commutation, CCB: Counter Current Breaking.

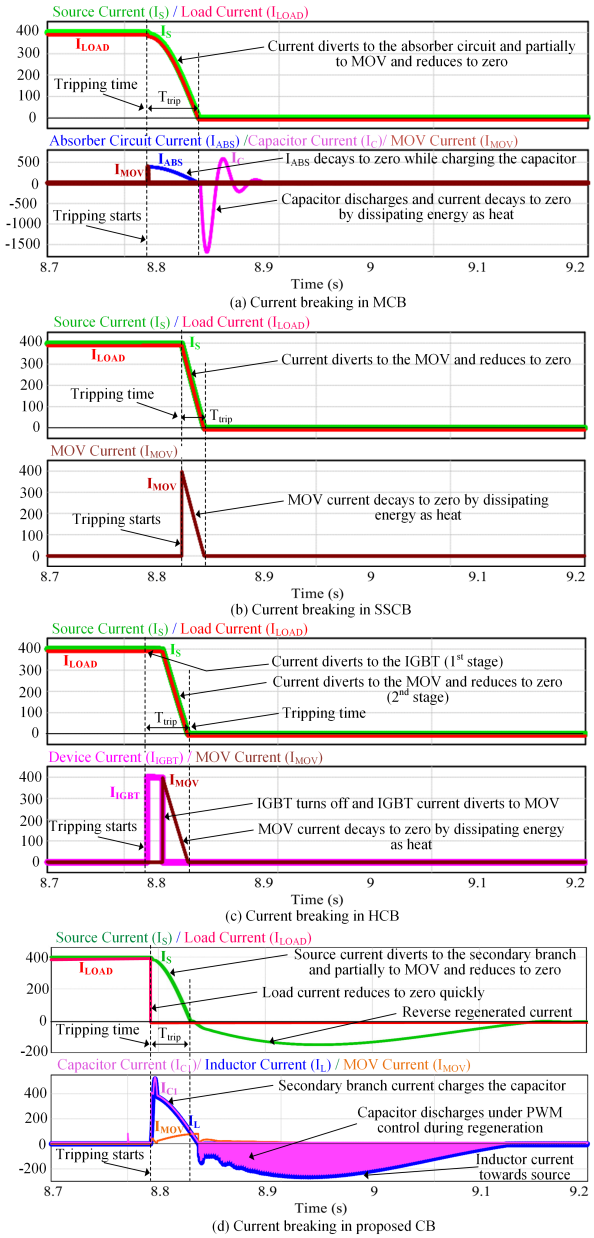

Fig. 12. Comparison of current breaking characteristics in different topologies

energy recovery efficiency, and the parameters L and C_1 need to be carefully chosen. In order to check the maximum voltage stress on the breaker components, the MOV was removed from the topology. The voltage stress is shown in Fig. 13 (c), which states that the lower the LC_1, the higher the voltage stress is.

V. Conclusion

In this study, a new and improved DCCB topology was designed and developed. This topology is superior to the conventional versions in several ways. The main feature of the proposed topology is that, instead of wasting energy, it conserves energy during every current breaking operation and regenerates it for feeding back to the source. This new regeneration capability ensures the energy efficient operation of DCCB and enhances the overall performance of the DC power system. The amount of energy that can be regenerated totally depends on the current that needs to be broken and the network inductance. Hence, high current inductive networks are going to be a very suitable application area for this topology. In this topology, the current breaking time does not depend on the load as the load current is separated from the source current upon receiving the trip signal. Hence, the switching of load is faster and more effective. However, it was observed that the PWM duty cycle has a great influence on the wave shape of the regenerated current. The smaller the duty cycle, the more smooth the regenerated current will be. But too low duty cycle takes longer time to regenerate and causes unnecessary energy wastage in the devices. Hence, a smart control algorithm can be developed to adjust the duty cycle dynamically so that optimum regeneration with smoother injected current is possible. Furthermore, this topology focuses on recovering energy from the source side inductance only and does not have any mechanism to recover energy from the load side inductance if there is any. In addition to that, the lack of bidirectional power flow capability, the requirement for a higher voltage rating for the capacitor and the dependency of trip time on the network parameter etc. are few of the issues that need to be resolved in future studies.

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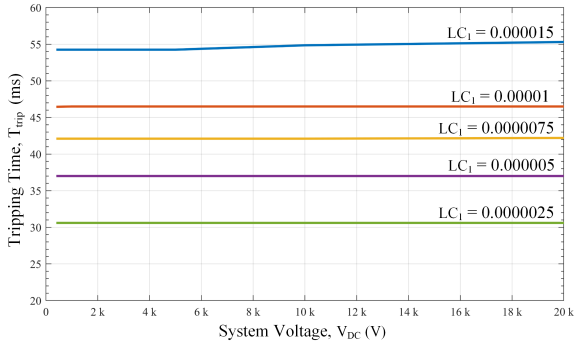
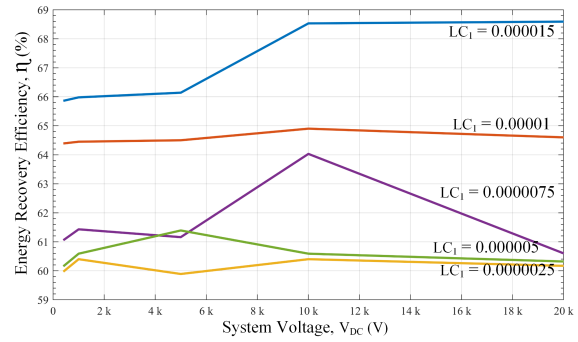
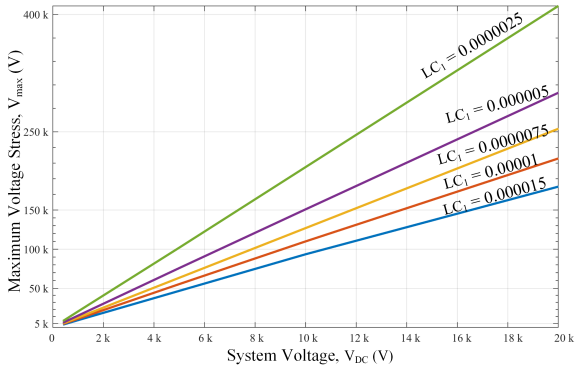


(a) Variation of tripping time with respect to system voltage



(b) Variation of energy recovery efficiency with respect to system voltage



(c) Variation of voltage stress with respect to system voltage

Fig. 13. Performance evaluation for high voltage application

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