GATE THRESHOLD VOLTAGE MEASUREMENT METHOD FOR SIC MOSFET WITH CURRENT-SOURCE GATE DRIVER

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Abstract

Gate threshold voltage is a classic thermo-sensitive electrical parameter (TSEP) for the junction temperature estimation and the gate oxide degradation, which is considered as a promising precursor for the online condition monitoring of power MOSFET. However, due to the fast switching transient, the gate threshold voltage of SiC MOSFET is much more difficult to measure than its Si counterpart. More specifically, the conventional measurement method mentioned in the datasheet obtains the gate threshold voltage during the turn-on transient, which requires the measurement to be completed within tens of nanoseconds. This paper presents a new approach to evaluate the gate threshold voltage with the assistance of a current-source gate driver. The advantage of the proposed measurement method is its lower requirement for the bandwidth of the measurement circuit, compared with the conventional method. The principle of the proposed method is demonstrated, followed by the simulation validation. A current-source gate driver is designed and constructed to assess the proposed method in experiment which shows that the measurement results can be used to evaluate the junction temperature effectively.

1 Introduction

Knowledge of the junction temperature of power devices in dc/dc converters[1] or battery chargers [2]are essential for safe operation. Gate threshold voltage (V_{th}) is commonly the minimum gate-to-source voltage required to create a conducting path between the source and drain terminals to turn-on the device . It is widely-regarded as an effective thermal-sensitive electrical parameter (TSEP) for junction temperature evaluation of MOS based devices (MOSFET and IGBT) [3]–[9]. Compared with other TSEPs, the gate threshold voltage has a higher temperature resolution [3] and higher linearity [10]. Therefore, it is regarded as the most suitable parameter for junction temperature estimation [2][9] . However, the measurements of V_{th} in most of the works are conducted in laboratory condition and cannot be applied in practical converters. In order to measure V_{th} online, the concepts of "quasi-threshold voltage" [2][7] and "pre-threshold voltage" [8] are proposed. Nevertheless, high-speed circuitry is required to detect the events of gate voltage rise and drain current rise from a zero level [10] in all the aforementioned works. Furthermore, the faster the devices switch, the higher must be the bandwidth of the measurement circuitry. Therefore, it is more challenging to apply the conventional V_{th} measurement method on the new-generation devices like SiC devices.

Silicon carbide (SiC) power electronics is regarded as a potent alternative to state-of-the-art silicon (Si) technology with its superior properties in the aspects of frequency, efficiency, power density and operating temperature [13]–[17]. However, SiC brings not only the benefits, but also the challenges. The low on-state resistance, fast switching transient and high susceptibility of noise increase the difficulty to measure most of the TSEPs as it requires higher resolution and higher bandwidth for the sampling circuit. On the other hand, the measurement of V_{th} is even more important for SiC MOSFET, because it is widely-reported that SiC MOSFET has more vulnerable gate oxide than its Si counterpart [18]–[20] and V_{th} is the potential indicator for the gate oxide degradation [21][22]. In order to conduct online TSEP measurement on SiC device, various approaches are proposed: the switching speed is slowed down intentionally [23] to make it easier for sampling circuit; the complicated logic control circuitry is constructed in [9]. However, none of the proposed methods is suitable for in-situ cost-effective realisation of V_{th} measurement.

This paper presents a new approach to evaluate the gate threshold voltage with the assistance of a current-source gate driver. The advantage of the proposed measurement method is its lower requirement for the bandwidth of the measurement circuit, compared with the measurement methods in the works mentioned above.

The structure of the paper is organised as follows: the principle of the measurement method is proposed in section 2, illustrating the measurement process and the signal sequence used in the measurement. Then simulation is presented in section 3 to evaluate the accuracy of the proposed measurement method, compared with the conventional measurement method from datasheet. Moreover, the prototype of the current-source gate driver is designed and constructed in section 4, and the experimental results in section 5 verify the effectiveness of the proposed method for junction temperature evaluation. The conclusion is drawn in the last Section.

2 Proposed Vth measurement method

The circuitry of the proposed V_{th} measurement method is relatively simple, compared with the method proposed in [9]. A current-source gate driver is used to generate the operating gate current as well as the measuring current. A controlled high voltage switch *S* introduces two modes: operating mode and measuring mode. The gate terminal of the device and the drain terminal are connected through a switch *S* as is shown in the diagram of the proposed method in Fig 1. The operating mode is that the switch S is turned off and the device works normally to be turned on and off. In this mode, a high voltage is blocked by the switch S and the operating gate current is generated by the current-source gate driver to turn the device on and off. The system can be changed to the measuring mode when the switch S is turned on. In this mode, the gate and drain terminal are shorted and a constant gate current is generated by the current-source gate driver. The gate current firstly charges the gate-source capacitance of the device and boosts the gate voltage from off-state gate voltage to the gate threshold voltage. When the gate voltage reaches the threshold voltage, a conducting path between the drain and source terminals starts to form.

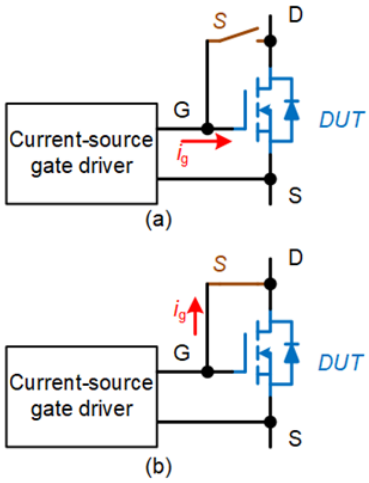

Fig. 1 Diagram of the proposed V_{th} measurement method
(a) operating mode (b) measuring mode

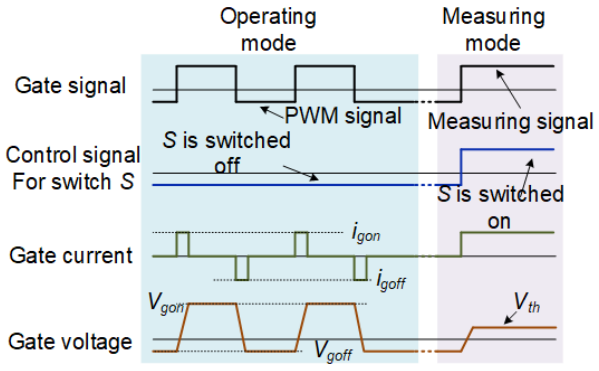

Fig. 2 Signal sequence of the proposed V_{th} measurement method

Once the gate current is conducted through drain to source, the gate voltage stops to increase and stays constant at threshold voltage. The signal sequence of the operating mode and measuring mode is demonstrated in Fig. 2. When working under operating mode, the gate voltage of the device is toggling from off-state gate voltage to on-state gate voltage. In contrast, the gate voltage remains at the gate threshold voltage in the measuring mode. Therefore, the gate threshold voltage can be easily measured during this interval.

3 Simulation verification

From the analysis above, the threshold voltage is obtained when the gate voltage stops increasing and the generated constant gate current flows through drain and source. However, this is not the common process of threshold voltage measurement in the datasheets. In order to compare the results of the proposed V_{th} measurement method with the V_{th} measurement method defined in the datasheets, a simulation is conducted using the software platform, TINA, from Texas Instruments (TI). The device model used in the simulation comes from ROHM, the spice model of the 3rd generation

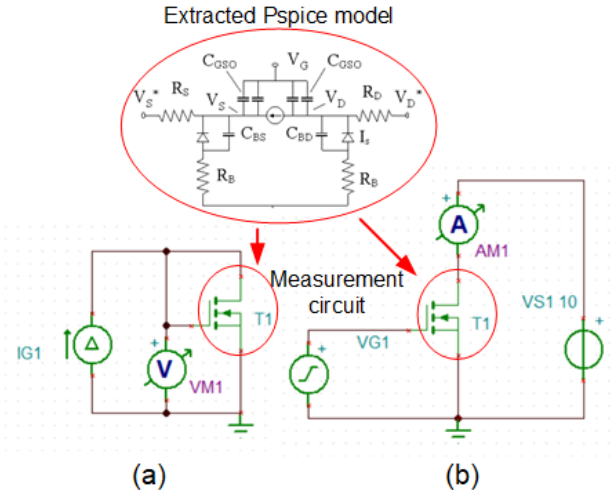

Fig. 3 Schematic of the simulation circuit
(a) proposed V_{th} measurement method
(b) V_{th} measurement method from the datasheet

trench-type SiC MOSFET SCT3060AL, where the detailed parameters in the model provide similar performance as the practical device. In the datasheet, the threshold voltage is defined as the gate voltage when drain current reaches 6.67mA under 10V drain-source voltage. In comparison, the proposed measurement method should be the gate voltage when the constant gate current is 6.67mA and the drain terminal is shorted with the gate terminal. The schematic of the simulation circuit is illustrated in Fig.3, and the simulation results are presented in Fig.4 and Fig.5 respectively. In the proposed V_{th} measurement method, a step current (IG1) with a value of 6.67mA is generated which flows through drain and source while drain and gate terminals are shorted. Fig.4 presents the simulation results of the proposed measurement method: the top waveform is the generated current IG1, whose magnitude jumps at 6.67mA after 5us. The corresponding gate voltage signal is demonstrated in the bottom waveform (VM1). The

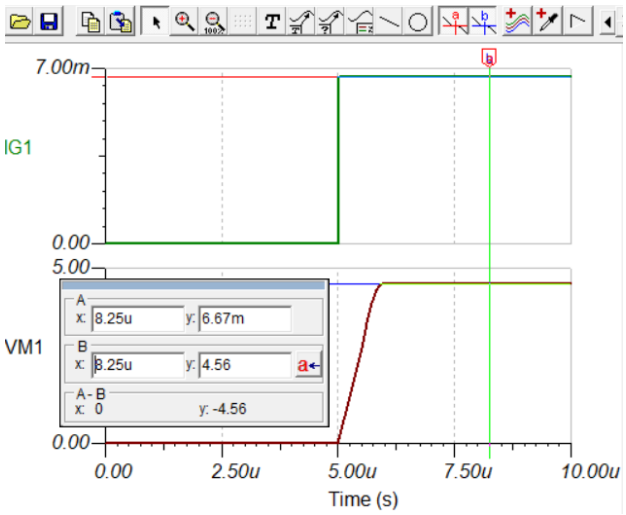

Fig. 4 Simulation results of the proposed V_{th} measurement method

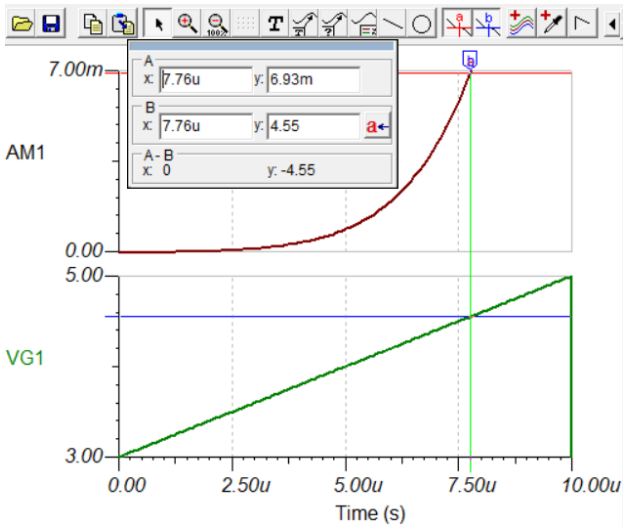

Fig. 5 Simulation results of the V_{th} measurement method from datasheet

measured threshold voltage is 4.56V. In the V_{th} measurement method from datasheet, a slope gate voltage is generated ranging from 3V to 5V after 10us, 10V bias drain-source voltage is applied and the drain current is monitored. When the drain current reaches 6.67mA, the corresponding gate voltage is obtained as the threshold voltage. Fig.5 presents the simulation results of the V_{th} measurement method from datasheet, the top waveform shows the drain current (AM1), while the bottom waveform is the generated slope gate voltage. It is shown when the drain current reaches around 6.67mA, the corresponding gate voltage is 4.55V, which is almost the same with the proposed V_{th} measurement method. Therefore, it is verified that there is only a slight difference between the proposed V_{th} measurement method and the conventional V_{th} measurement method from datasheet. Moreover, the advantage of the proposed V_{th} measurement method is obvious in the simulation: both the gate voltage and the drain current stay constant during the measurement interval in the proposed method, whereas both the gate voltage and the drain current vary in large in the conventional measurement method. The requirement for the bandwidth of the sampling circuit is extremely high for measuring the gate voltage at a specific time point. In contrast, the proposed method makes it much easier for the sampling circuit and provides higher accuracy.

4 Proposed current-source gate driver

In the proposed method presented in section 2, the most significant unit is the gate driver, which is supposed to generate constant current in the measuring mode while working as a conventional gate driver in the operating mode. In order to evaluate the effectiveness of the proposed measurement method, a current source gate driver is proposed and designed. Fig 6 illustrates the schematic of the proposed current-source gate driver. This current-source gate driver has a simple structure with three functional parts: signal amplification, signal isolation and signal conversion. The input signal can be generated by the controller, before the signal is amplified using the amplifier U1. In order to isolate the high voltage from the control system, a transformer T is used before the amplified signal is converted into the corresponding current signal with the assistance of amplifier U2. There are 3 main functions of the proposed gate driver: firstly, the small input signal generated by the controller is amplified from less than 1V to the gate voltage level (-5V to 15V); next, the control system is isolated from the power circuit high voltage; finally , the voltage signal is converter into a gate current signal. Therefore, the constant gate current is generated once a constant voltage signal is fed into the gate driver. With the proposed current-source gate driver, the gate current is fully controlled by the output signal of the controller. In the operating mode, turn-on and turn-off gate current is generated with the time interval corresponding to the on-state and off-state time. In the measuring mode, constant gate

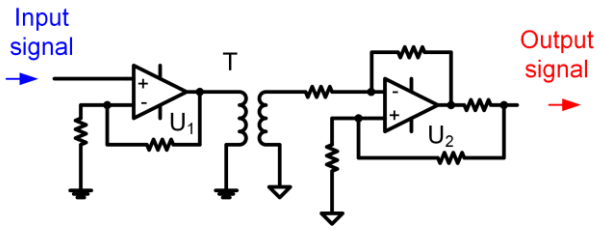

Fig. 6 Structure of the proposed current-source gate driver

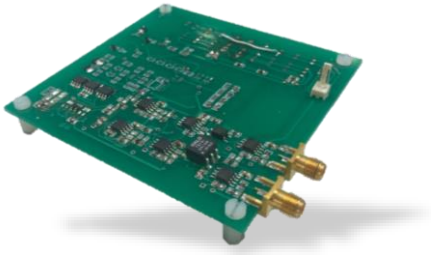

Fig. 7 Photo of the gate driver prototype

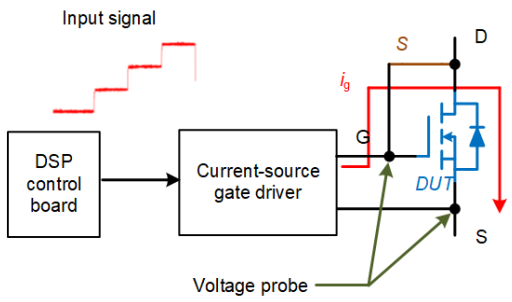

Fig. 8 Diagram of the experiment setup

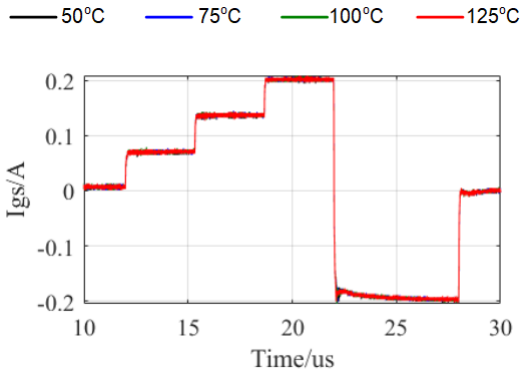

Fig. 9 Waveforms of the gate current signals at different temperatures

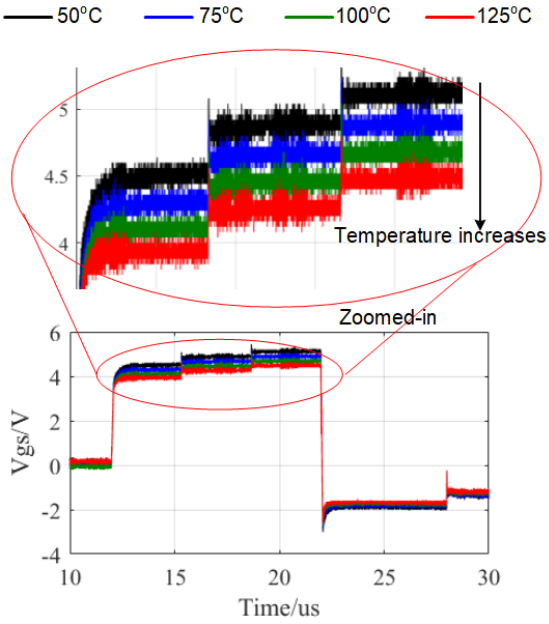

Fig. 10 Waveforms of the gate voltage signals at different temperatures

current is generated to keep the gate voltage at threshold voltage for several microseconds. Therefore, it is much easier for the sampling circuit than measuring the gate voltage during the turn-on transient, whose time scale is tens of nanoseconds. A photo of the gate driver prototype is presented in Fig 7.

5 Experimental verification

As the effectiveness of the proposed V_{th} measurement method is validated in simulation presented in section 3, this section presents the experimental verification of using the proposed V_{th} measurement method for junction temperature evaluation with the current-source gate driver demonstrated in section 4. In the experiment, the aforementioned ROHM SiC MOSFET SCT3060AL is used as the device under test. As the focus is the measuring mode, only the performance of the device under measuring mode is evaluated in the experiment. As is shown in Fig.8, the diagram of the experiment setup is presented. The DSP serves as the controller to generate the signal, before the signal is input into the proposed gate driver presented in section 4. After signal processing, the gate current with the exact profile as the input signal is generated. The gate current is then input into the gate terminal of the device. While the 6.67mA gate current is too small for the used current probe to catch the waveform, a higher current is generated in the experiment. Furthermore, in order to investigate the influence of current value on the measurement, the 3-step signal is taken as an example as shown in Fig.8. While the experiments are repeated 4 time under different temperatures from 50ºC to 125ºC, the variation of the measured threshold voltage against temperature is evaluated.

The waveforms of the gate current signals at different temperatures are presented in Fig.9. It is shown that the gate current signal stays the same under different temperatures with the values of 3-step are 67mA, 133mA and 200mA respectively. Although the current signals are the same, the corresponding measured gate voltage gets lower at higher temperatures as is shown in Fig.10. The experimental results confirm the simulated results shown in Fig.11. More specifically, the variation of the 3-step gate voltage value over temperature is illustrated in Fig.12. The solid lines represent the experiment results while the dotted lines are the simulated results. The blue line with circle points is the gate voltage measured in the first step, where the current flow through drain-source is 67mA. The green line with square points is the gate voltage measured in the second step, where the current flow through drain-source is 133mA. The red line with diamond points is the gate voltage measured in the final step, where the current flow through drain-source is 200mA. It is shown that no matter what value the current is, the measured gate voltage declines as the temperature gets higher. All the experimental results and simulated results show linear relation with temperature as is shown in Fig.12. The sensitivities of the experimental results are 7.7mV/ºC at 67mA, 8.2 mV/ºC at

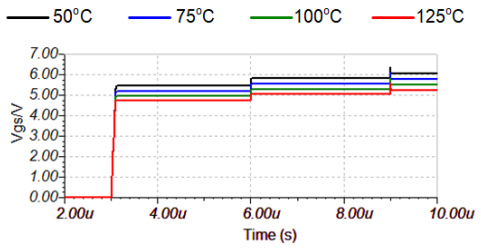

Fig. 11 Gate voltage simulation of the 3-step signal

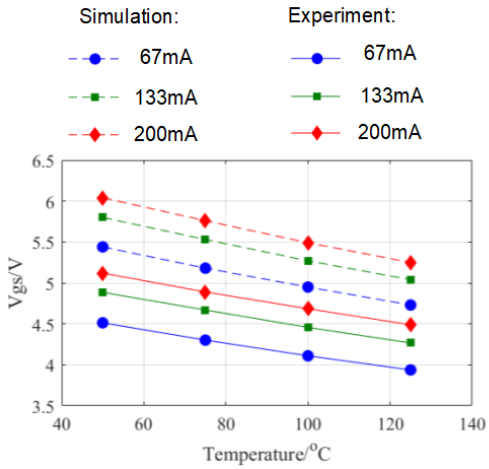

Fig. 12 Experimental results of the proposed measurement method compared with the simulation at different currents and temperatures

133mA, 8.4 mV/ºC at 200mA, while the sensitivities of the experimental results are 9.4mV/ºC at 67mA, 10.1mV/ºC at 133mA, 10.5mV/ºC at 200mA. The difference between experimental and simulated results is within the threshold voltage variation (2.9V) provided in the datasheet (from 2.7V to 5.6V). It is shown that the sensitivity of the measured voltage increases with rising gate currents . Once the gate voltage of the proposed method is measured, the junction temperature can be estimated with the linear relationship between measured gate voltage and temperature. Therefore, the effectiveness of the proposed measurement method for junction temperature evaluation is verified.

6 Conclusion

This paper presents a new gate threshold voltage measurement method with a current-source gate driver. Compared with conventional V_{th} measurement method, the proposed method has lower requirement for the bandwidth of the sampling circuit. The proposed method is simulated and compared with the conventional measurement method, which shows the almost identical measurement results. In addition, a current-source gate driver is designed and constructed to evaluate the proposed measurement method in experiment. The experiment results validate the effectiveness of the proposed measurement method for the junction temperature evaluation.

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