AN INVESTIGATION INTO THE INHERENT ROBUSTNESS AND OPTIMAL HARMONIC PERFORMANCE OF THE ADVANCED STATIC VAR COMPENSATOR (ASVC)

A thesis submitted to

THE UNIVERSITY OF NORTHUMBRIA AT NEWCASTLE

for the degree of

DOCTOR OF PHILOSOPHY

by

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April 2001

Declaration

No portion of the work referred to in this thesis has been submitted in support of an application for another degree or qualification in this or any other university or institution of learning.

Dedication

To Lorraine,

Maureen & Sophie

Thank you

Acknowledgements

I would like to thank all the technical, administrative and academic staff at the University of Northumbria at Newcastle (UNN) for their continuous encouragement and guidance throughout the work. Particularly I would like to thank Dr. Richard Binns, Dr. Li Ran and Dr. Gavin Armstrong for continual academic and technical assistance. Also, I would like to thank Mr. Ed Holmes for his technical assistance in the laboratory.

Gratitude is expressed to my director of studies, Dr. G. A. Putrus. Extensive appreciation is also expressed to the Power Systems research group at UMIST, in particular Professor Nick Jenkins, for allowing time and facilities in the final stages of the work.

For the support and encouragement I have received throughout the project, I would like to thank Adrian Hawkins and James Allen. Also, Dan Joyce for substantial support at times when it was most needed.

Within my family I would like to thank my sister, for giving me strength and determination, my brother for his eccentricity and flair and my dogs (Sophie and Macey) for reminding me of the simplicity of laughter.

Lorraine, a classic novelist could never describe the depth of appreciation and admiration I have for you for helping me through this period of my life. So, as I'm just a simple working class northerner, I'll just say cheers.

Finally to my mother, it may have taken some time but I have eventually realised that it's the love in your life and the smile on your heart that's the true measure of the achievement in your life. So open your heart and smile on you crazy diamond.

ABSTRACT

For many years, it was generally understood that a.c. transmission systems could not be controlled fast enough to handle dynamic system conditions. The dynamic system problems were usually handled by over-design, which resulted in under utilisation of the system. Flexible AC Transmission System (FACTS) devices play an important role in improving the dynamic performance of a power system and hence achieve better utilisation of the available system. They are principally employed to 'rapidly' control one or more of the three main parameters directly affecting a.c. power transmission, namely the system impedance, magnitude and phase angle of the system voltage. The Voltage Source Inverter (VSI) is the basic building block of most FACTS devices. The multi-level VSI topologies are becoming the favourite power circuits for the 2nd generation of FACTS shunt compensators.

The research reported in this thesis is to investigate the reliability of Voltage Source Inverter topologies that are used in high power applications, mainly the Advanced Static VAr Compensator (ASVC). The inherent redundancy of the diode-clamped multi-level VSI topology, with respect to short-circuit and open-circuit device faults, is investigated using a space-vector nodal representation. The harmonic performance of the ASVC under normal and during 'device fault' operating conditions is also investigated.

A new multi-level inverter topology is proposed to improve the robustness of the conventional diode-clamped VSI topology. Harmonic spectrum 'recovery' techniques to be utilised in the event of device failure are also investigated and discussed. An adaptive PWM controller is proposed to maintain an acceptable low order harmonic performance for the ASVC under normal and abnormal operating conditions. The results obtained show that the proposed system can maintain uninterrupted operational performance throughout certain device failure conditions.

An experimental 3-level discharge path protection switch clamped (DPPSC) VSI system has been designed, constructed and analysed. To demonstrate the 3-level adaptive SHEM strategy, the adaptive DPPS controller was implemented on a TMS320F240 DSP evaluation module (EVM). The results were in good agreement with those predicted in the analytical and simulation parts of the work.

The research carried out in this work showed that under loaded operating conditions, the low frequency harmonic components targeted by SHEM techniques are not fully eliminated from the output voltage spectrum. This investigation revealed that this is due to the harmonic interaction between the a.c. and d.c. sides of the multi-level inverter. A new 'Dynamic Selective Harmonic Elimination Modulation (DSHEM)' scheme is proposed to overcome this problem. The DSHEM dynamically adjusts the switching angles according to the system operating point. The proposed method is verified using simulation and the experimental model.

CONTENTS

NOMENCLATURE

α	SHEM firing angle
β	Modulation angle
a.c.	Alternating current
ADC	Analogue to digital converter
ASVC	Advanced static VAr compensator
B	Blue
C	Capacitor
CD_{XY}	Clamp diode (x indicates phase, y indicates limb position)
CSI	Current source inverter
d.c.	Direct current
DAC	Digital to Analogue converter
DCMLI	Diode-clamped multi-level inverter
DPPS	Discharge path protection switch
DSHEM	Dynamic selective harmonic elimination modulation
DSP	Digital signal processor
DSSPC-MLI	Discharge path protection switch clamped multi-level inverter
FACTS	Flexible AC transmission systems
FC	Fixed capacitor
FFM	Fundamental frequency modulation
GTO	Gate turn-off thyristor
HVDC	High voltage direct current
I	AC current
I/O	Input / output
i_{cap}	Capacitor current
IGBT	Insulated gate bi-polar transistor
L	Inductor
MSC	Mechanically switched capacitor
MSR	Mechanically Switched reactor
NPC	Neutral point clamped
p.u.	Per-unit

PLL	Phase locked loop
PWM	Pulse width modulation
R	Red
R	Resistor
rms	Root mean square
SHEM	Selective harmonic elimination modulation
SVC	Static VAr compensator
$\mathbf{S_{XY}}$	Switch (x indicates phase, y indicates limb position)
TCR	Thyristor controlled reactor
THD	Total harmonic distortion
TSC	Thyristor switched capacitor
UFC	Unrestricted frequency changer
V	AC voltage
VAr	Volt-amperes reactive (reactive power)
$\mathbf{V_{ASVC}}$	ASVC output voltage
$\mathbf{v_{cap}}$	Capacitor voltage
$\mathbf{V_{CE}}$	Collector-emitter voltage
$\mathbf{V_{dc}}$	DC voltage across each capacitor unit
$\mathbf{V_S}$	AC system voltage
VSI	Voltage source inverter
X	Inductive reactance
Y	Yellow

1 INTRODUCTION

1.1 THE ELECTRIC POWER SYSTEM

The continual research and analysis over the last few decades has led to a worldwide acknowledgement throughout electric power engineering that the a.c. electric power system, at transmission and distribution levels, requires parameter control as an integral design factor to ensure a reliable and secure provision of electrical energy to the consumer.

The concept of network control through implementation of reactive power (VAr) compensators, to increase the transmittable power in an a.c. power system, is a well-established technique [1]. At the beginning of the 20th century, basic fixed quantity VAr compensators were implemented to improve the steady-state characteristics of the power system. The necessity for a dynamic controllable reactive power compensation system was recognised in 1931 with Friedlander's shunt connected saturated reactor [2]. These early controllers were implemented essentially to improve the overall transmission capabilities that were being restricted due to the reactance associated with a long transmission line and to compensate for predetermined loads throughout the system.

More recently, since the Electricity Act of 1989, the deregulation of the UK electric supply industry has had a profound effect upon the need for the optimum utilisation of the currently available transmission and distribution networks. The electrical utilities and power industry throughout the world are experiencing radical changes due to a generalizing world economy and trend towards liberalisation. This progress will effect not only the traditional electrical power generation but also the transmission and distribution of energy [3]. Whilst the last few decades has shown a growing worldwide demand for electrical energy, the new generation of environmentalists have canvassed for the restriction of the construction of new transmission lines with the knowledge of under-utilisation of existing networks.

Coupled with the economic restrictions is the resultant competitive market factor of the deregulation and privatisation of the electrical power industry. Throughout the world, utilities are recruiting customers that may, in some cases, be located thousands of miles from the utilities regular operational location. In the UK this has filtered through in the last few years to the domestic customer with various energy suppliers offering a cheap yet reliable provision of power irrespective of the consumers location. This epitomises the criticality of a reliable interconnection of transmission and distribution systems and the radical improvements required in the dynamics and methodologies of a.c. system control.

1.2 FLEXIBLE AC TRANSMISSION SYSTEMS (FACTS)

The necessity of improved control techniques to meet the worldwide increasing demands for more power, higher quality and improved reliability has led to the development of power electronic configurations of the conventional reactive power (VAr) controllers. In the late 1980's the Electric Power Research Institute (EPRI) commissioned a new technology referred to as Flexible AC Transmission Systems (FACTS). The term FACTS is defined by the IEEE PES Task Force of the FACTS Working Group as [4]:

Flexible AC Transmission System (FACTS). *Alternating current transmission systems incorporating power electronic- based and other static controllers to enhance controllability and increase power transfer capability.*

The technology was intended to offer solutions for transient stability control and hence improve utilisation of transmission networks. The FACTS controllers immediately arrived in two generations. The currently implemented a.c. system controllers using thyristors were grouped as 1st generation. Whilst proposals of improved solid-state inverter based topologies were classified as the 2nd generation of FACTS. A wide range of power electronic-based FACTS controllers are becoming routinely employed in order to enhance the power transfer capabilities of the otherwise under-utilised parts of an interconnected network.

One of the first representatives of the large 2nd generation FACTS controllers to be constructed was known as the Advanced Static VAr Compensator (ASVC). Proposed by Gyugyi [5], the shunt reactive power compensation topology offers a dynamically responsive improvement to the conventionally implemented synchronous condenser. The voltage source inverter (VSI) is thought off as the building block of the ASVC and many other FACTS controllers. With the series and shunt control techniques being established, the development of various multi-level inverter topologies has become the focus of many research establishments. The sections of the network that FACTS devices are applied to are typically integral in terms of maintaining system stability and optimal power flows. Therefore, it is crucial that the VSI topology implemented within the FACTS controller offers a reliable and optimum level of performance.

1.3 Scope of the Research Project

The research presented in this thesis studied the steady-state (open-loop) performance of the diode clamped multi-level voltage-source-inverter topology applied to the Advanced Static VAr Compensator. Initially, an overview of shunt VAr compensation and possible topologies for VAr compensators are presented. An investigation of the inherent redundancy and overall robustness of the diode clamped multi-level inverter (DCMLI) in the event of a power circuit device fault is described. Low frequency switching scheme harmonic analysis is presented to illustrate how the limitations of the investigated topology can be overcome. A 'new' adaptive DCMLI topology and control scheme is proposed.

To verify the validity of the new system, a 3-phase multi-level adaptive DCMLI, implemented with a TMS320F240 digital signal processor (DSP), was developed. Comparative analysis between theoretical predictions and practical results is observed. Finally, the harmonic and overall performance of the DCMLI based ASVC under VAr compensation conditions are investigated. The effect of the 'idealised' PWM schemes on the overall performance of the DCMLI is investigated and a Dynamic Selective Harmonic Elimination Modulation (DSHEM) scheme is proposed. The improved performance is verified through practical implementation.

1.4 OVERVIEW OF THE THESIS

Chapter 2: A summarized historical background of power system reactive power (VAr) compensators, specifically shunt, to assist in the steady-state and dynamic stability of a transmission system is presented. Conventional compensators and new concepts used in FACTS technologies are introduced. An overview of the principles of the Advanced Static VAr Compensator (ASVC) is also presented.

Chapter 3: The topologies of 1st generation – variable reactive admittance – Static VAr Compensator (SVC) and 2nd generation – solid-state converter – Advanced Static VAr Compensator (ASVC) are presented. Voltage source inverter (VSI) topologies suitable for high power ASVC application such as the conventional six-pulse VSI, the multi-level VSI topologies and the multi-phase configurations are discussed.

Chapter 4: The inherent redundancy of the stand-alone diode-clamped multi-level voltage-source-inverter (DCMLI) is investigated. Representation of the 3-level DCMLI topology in the space vector nodal plane is derived. Short-circuit and open-circuit device fault investigations are demonstrated. The Chapter is concluded with an observation of the robustness and the possibility of redundancy in the event of a device fault.

Chapter 5: Harmonic analysis of the stand-alone VSI structures suitable for the ASVC applications is presented. Firstly, optimised strategies for fundamental frequency modulation (FFM) are presented. Secondly, the selective harmonic elimination modulation (SHEM) harmonic recovery strategies are presented and discussed.

Chapter 6: This Chapter describes a new topology proposed to increase the robustness of the DCMLI system. The DCMLI topology implementing an adaptive discharge-path protection switch is presented. Operational considerations together with a new adaptive control scheme are discussed. Simulation results of

the adaptive 3-level VSI ASVC topology are given to illustrate the operation under normal and abnormal conditions.

Chapter 7: The construction of the laboratory model adaptive multi-level VSI employing a DSP controller is explained in this Chapter. Development of the power circuit and associated drivers together with the adaptive controller is presented. Fault sensing requirements and programming of the TMS320F240 DSP are also described.

Chapter 8: In this Chapter, the performance of the experimental laboratory model adaptive 3-level VSI based ASVC is analysed. The results of the three-phase 3-2 level VSI operation are discussed. Reactive power flow is demonstrated using a generalised machine and open-loop control.

Chapter 9: This Chapter investigates the harmonic interaction between the a.c. and d.c. sides of a 3-level inverter used as an Advanced Static VAr Compensator (ASVC). It is illustrated that due to the 3^{rd} harmonic voltage across each d.c. side capacitor, the conventional SHEM scheme may not actually eliminate the target harmonics when the system is on load. A new modulation method, which dynamically adjusts the switching angles according to the operating point, is proposed to overcome this difficulty. The proposed method is verified using experimental and simulation results.

Chapter 10: This Chapter summarises and discusses the conclusions drawn from the theoretical analysis, simulations and the laboratory work of the entire project. Suggestions are given for further work.

2 REACTIVE POWER (VAR) COMPENSATORS

2.1 INTRODUCTION

The overall operation of the a.c. transmission system is governed by the following interrelated parameters: series impedance, current, voltage and phase angle [4]. These parameters can be controlled, corresponding to the utility demand, by conventional controllers and recently by rapid-response power electronics in the form of FACTS controllers. The available controllers can generally be categorised into series, shunt and combined (series-shunt) controllers which can be applied individually or in coordination with each other to provide control of one or more of the system parameters. Although there is a necessity for all types of system controller, strategically positioned throughout a power system network, this project concentrates on the shunt VAr compensator only.

This Chapter presents the importance of shunt VAr compensation together with a review of the conventional and state of the art FACTS controllers available for such an application. The final section presents a detailed description of the principles of the Advanced Static VAr Compensator (ASVC), the FACTS controller to which this project is focussed upon.

2.2 SHUNT VAR COMPENSATION

If a power system is separated into its basic elements it can generally be categorised into three main components: generation, transmission or distribution and loads. This project investigates the concept of reactive power compensation, where the main objective is to strengthen the transmission and distribution systems. The most basic representation of the transmission line is with reactive ladder networks composed of series inductors and shunt capacitors [4,6]. From inductor (L) and capacitor (C) component first principles it is apparent that the series inductance determines the maximum transmittable power, whereas the shunt capacitance influences the voltage profile and thereby the power

transmission along the line. The problem of reactive power control therefore runs hand in hand with the voltage control problem, as a reactive power imbalance results in an inherent voltage deviation in the transmission line. This is further discussed in Appendix A.

Reactive power (VAr) control in the form of shunt compensation is a scheme that provides voltage support and assists in improving the overall performance of the a.c. power system. Shunt VAr compensation may be applied at a number of points such as intermediate switching stations or at load tee-off points along the transmission line [2]. The optimum positioning of the shunt VAr compensator is dependent upon the infrastructure of the transmission line. If a line is interconnecting two a.c. system buses then midpoint compensation is the most effective for voltage support. Whereas for a radial line, which is typical in a decentralised form of generation such as wind turbines, it is evident that the end of the line is the best location for the compensator. This is because the largest voltage variation is experienced at the end of the line that may, under extreme transient conditions, suffer from voltage collapse. The implementation of reliable and fast VAr compensators is becoming ever more critical with the increasing complexities of the modern a.c. power system.

2.3 CONVENTIONAL SHUNT COMPENSATORS

The requirement of VAr controllers has long been recognised. The simplest and cheapest form of shunt VAr compensation is the fixed capacitor (FC) and its counterpart the fixed shunt reactor, shown in Figure 2.1(a). This type of compensation has been used for a.c. power transmission since the beginning of the last century. It is the 'belt and braces' technique and simply acts upon the steady-state transmission characteristics. Fixed capacitors are used to compensate for known large inductive load points and to provide voltage support throughout the transmission network, hence maintaining the required voltage profile. Whereas, fixed shunt reactors are used to limit the transient and temporary overvoltages due to load rejection, faults or line energisation. Unfortunately this fixed form of compensation reduces the power transfer capacity and surge impedance power by about 20% [6].

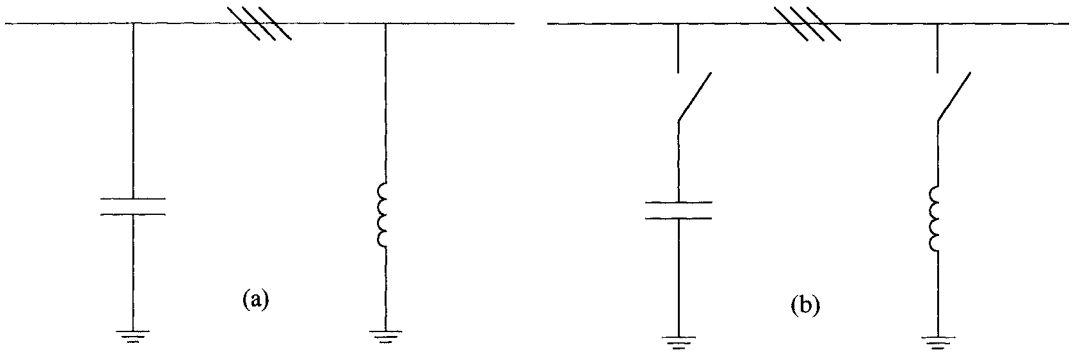


Figure 2.1 – (a) Fixed Capacitor and Reactor, (b) Mechanically Switched Capacitor (MSC) and Mechanically Switched Reactor (MSR)

Resulting from this risk of system instability these basic fixed system controllers were complemented by controlled reactive compensation in the form of mechanically switched capacitors (MSC) and reactors (MSR), illustrated in Figure 2.1(b). The MSC and MSR enable provision of additional VAr generation or absorption in the event of large variation in system loading or voltage levels. Modern power capacitors have a high unit-capacity, small losses, good reliability

and long time of operation and it is not uncommon to find them implemented into a hybrid scheme with more advanced FACTS technology [4,7].

The severe limitation of these compensators is that they could only compensate for steady-state slow variations and offered no continuously variable compensation. The necessity of compensation controllers offering a dynamic response with continuously variable generation or absorption of reactive power was traditionally satisfied with the implementation of rotating synchronous machines or synchronous condensers. By controlling the excitation of a mechanically unloaded synchronous machine, shown in Figure 2.2, the a.c. power system could be supplied with a controllable quantity of capacitive or inductive reactive power. At times of high inductive loading on the power system the compensator runs over-excited and generates reactive power. At times of light loads the machine is under-excited to absorb reactive power. Later, the dynamic stability and therefore the security and reliability of the a.c. power system was further assisted by the implementation of saturated reactors in conjunction with fixed capacitors [4].

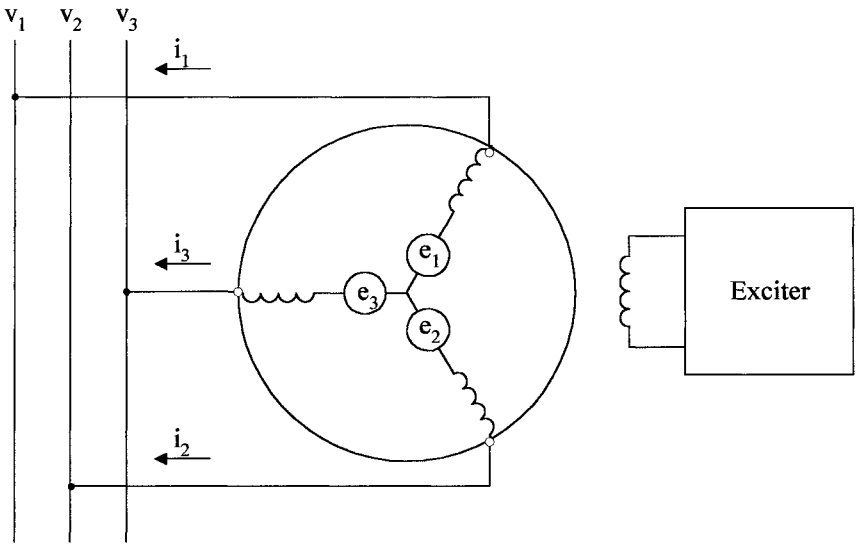


Figure 2.2 - Synchronous Condenser

The critical downfall of these conventional techniques is that they simply cannot provide the accuracy, of the controllable power flow, that is essential due to the complexities of today's power networks. Also, due to the speed of response being restricted to the mechanical switching time, in the case of the MSC and MSR, or the slow response of the synchronous machine the conventional controller cannot realize the dynamic response requirements necessary to maintain an operable secure system functional at close to its maximum transmittable power. While the saturated reactor compensator has a faster response it is bulky, expensive and its control is not flexible. It is well known that in the past this resulted in the under utilisation of the transmission system and very generous stability limits. This resulted in the system being operated far below its thermal rated capacity. Another major drawback of these system controllers is the maintenance required and the relatively short lifespan when compared to the more modern topologies.

2.4 1ST GENERATION FACTS SHUNT COMPENSATORS

Advances in high-power thyristor technology, increasing demands for improvements of the performance of transmission systems and the need for compensation of large industrial loads (such as electric arc furnaces), prompted the development of improved continuously variable VAr compensators. The first development was simply to replace the mechanically switched control with thyristor power switches, and precision controllers, to improve the response time and accuracy. By the late 1960's several large installations of shunt VAr compensators had started to appear using these new controllable static VAr sources [5].

The 1st generation of shunt FACTS static VAr generators (SVG's) maintained the variable reactive admittance technique of the traditional controller by still utilising the passive (L and C) components to vary the transmission line system parameters, but improved control precision with the use of thyristors. The term SVG is defined by the IEEE PES Task Force of the FACTS Working Group as [4]:

Static VAr Generator or Absorber (SVG): *A static electric device, equipment, or system that is capable of drawing controlled capacitive and/or inductive current from an electric power system and thereby generating or absorbing reactive power. Generally considered to consist of shunt-controlled, thyristor-controlled reactor(s) and/or thyristor-switched capacitors.*

2.4.1 THYRISTOR SWITCHED CAPACITOR (TSC)

The thyristor switched capacitor (TSC) VAr compensator utilises a capacitor in series with a bi-directional thyristor pair and a small reactor, as shown in Figure 2.3. The operation of the TSC is quite simple with the thyristors switching in a fixed quantity of shunt capacitive admittance if reactive power compensation is required. The purpose of the reactor is to limit switching transients, to damp inrush currents and to form a filter for harmonics coming from the power system or from any parallel-connected reactive power compensator. For 3-phase systems the delta connection of the 3-phase TSC is preferred as the 3rd harmonic is cancelled out under symmetrical conditions. The delta connection of the TSC is shown in Figure 2.4.

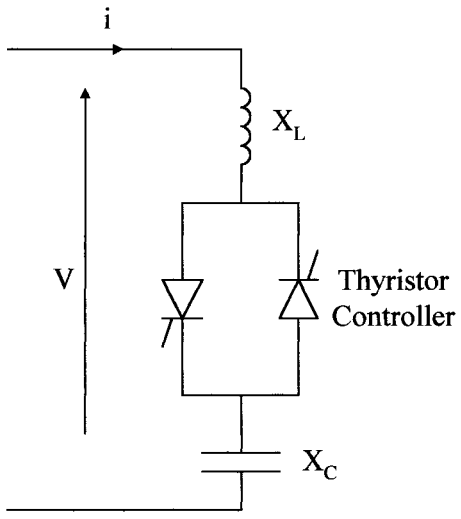


Figure 2.3 – Thyristor Switched Capacitor (TSC)

By connection of several TSC branches in parallel, it is possible to make the compensation as accurate as desired. A technique that is utilised is the binary system in which the total number of capacitors is divided into groups with each group taking the subsequent binary value, i.e. 1, 2, 4, 8, 16, etc. The smallest capacity is chosen in order for the required precision. This binary system gives a greater flexibility of compensation [8]. The TSC suffers mainly from high cost and the complexity of controls.

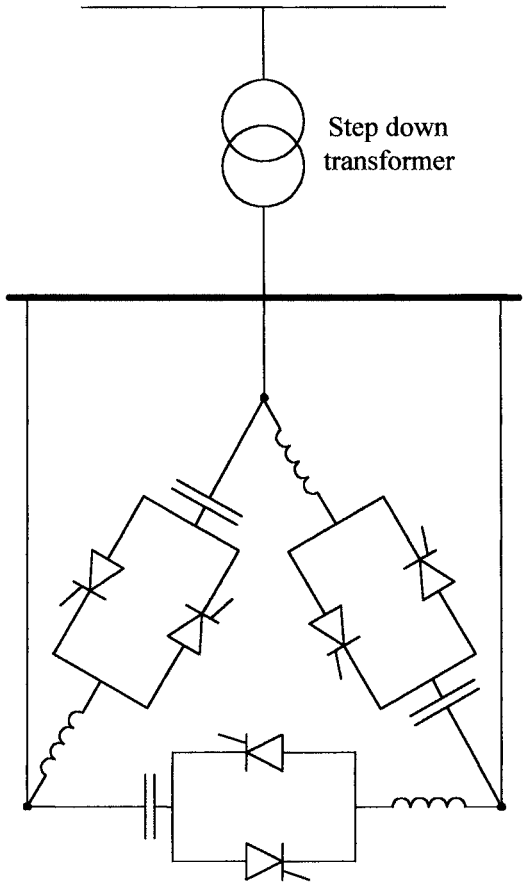


Figure 2.4 – Delta connected 3-phase Thyristor Switched Capacitor (TSC)

2.4.2 THYRISTOR CONTROLLED REACTOR (TCR)

The basic thyristor controlled reactor (TCR), shown in Figure 2.5, consists of a reactor in series with a bi-directional thyristor pair. The compensator operates by the thyristors conducting on alternate half cycles of the supply frequency.

Adjusting the conduction interval of the inverse parallel-connected thyristors controls the current flow in the inductor (L). This is achieved by delaying the turn-on of the thyristor switch by a firing angle (α) in each half cycle with respect to the voltage zero. If $\alpha = 90°$ the current is essentially reactive and sinusoidal [9]. Conduction is obtained with firing angles between 90° and 180°. Conduction angles of the two thyristors must be kept equal, as unequal conduction angles will produce even harmonic components in the current, including a d.c. value.

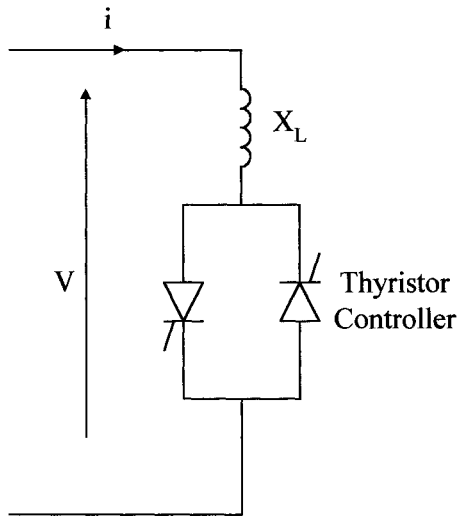


Figure 2.5 – Thyristor Controlled Reactor (TCR)

Even with symmetrical positive and negative half cycles of current the phase control operation of the TCR results in the generation of unwanted odd harmonics (in addition to the required fundamental current). This is due to the non-sinusiodal current waveform in the reactor. TCR configurations to improve the harmonic quality of the output current are presented in Chapter 3. For 3-phase applications the TCR can be connected in star or delta. As with the TSC the delta connection, shown in Figure 2.6, is preferred for the 3-phase TCR. This is due to the improved harmonic performance as under balanced conditions the triplen harmonics (3^{rd}, 9^{th}, 15^{th}, etc.) circulate in the delta and therefore do not enter the power system.

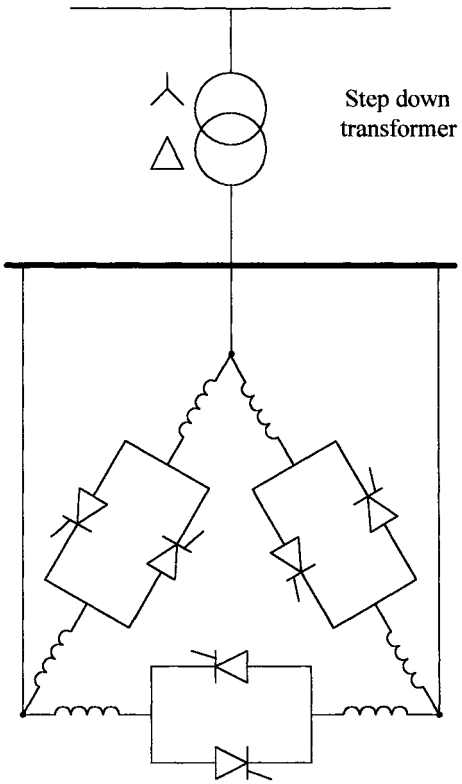


Figure 2.6 – Delta connected 3-phase Thyristor Controlled Reactor (TCR)

The thyristor controlled reactor (TCR) or thyristor switched capacitor (TSC) found much commercial success. This was due to their 'acceptable' cost, response time, control flexibility, very little maintenance and relatively simple thyristor switch arrangements [5]. It should be noted however that although these SVG's could be used individually, they were more effectively implemented combined (TSC-TCR) as a hybrid static VAr Compensator (SVC). The term SVC is defined by the IEEE PES Task Force of the FACTS Working Group as [4]:

Static VAr Compensator (SVC): *A shunt-connected static VAr generator or absorber whose output is adjusted to exchange capacitive or inductive current so as to maintain or control specific parameters of the electrical power system.*

The Static VAr Compensator (SVC) is one of the most commonly used compensation techniques in power systems [10]. There are many hybrid arrangements reported and various topologies to improve the operational

characteristics of these systems, as will be further described in Chapter 3. The SVC schemes consisting of either thyristor switched capacitors (TSC), thyristor controlled reactors (TCR), or both, provided a means of improved dynamic VAr compensation. However, as the SVC utilises passive components, the capacitor or inductor needs to be fully rated to generate or absorb the required reactive power. Also, a thyristor switching circuit rated at the sum of the maximum capacitive and inductive output is also required to control it. Therefore, SVC's are large systems that involve a number of major components, requiring a considerable size facility, particularly for the passive components.

When the first SVC's were developed, the solid-state power electronics represented the major share of the total equipment cost. By the 1980's the power handling capability of the power electronic devices had increased and devices such as high power Gate Turn Off (GTO) thyristors had started to emerge. This resulted in a drastic reduction in the total cost of switching devices required for a high power SVC [11]. Even with the advances in solid-state technology the effects on the total cost and size of the SVC was negligible, due to the large cost of the passive elements. Therefore a move towards an entirely solid-state compensation system was inevitable in order to achieve improvements in size, cost, control and dynamic performance.

2.5 2ND GENERATION FACTS SHUNT COMPENSATORS

The new solid-state inverter based compensator, proposed by Gyugyi in 1979 [5], defined the 2nd generation of FACTS shunt compensator. The principle is to replace the large passive elements that are used for generation or absorption of reactive current with force-commutated power electronic inverter topologies resulting in fully solid-state compensators.

In the 2nd generation of FACTS shunt compensators, which was essentially the 3rd generation of shunt compensators, the generation of reactive power is obtained by switching devices with minimum passive elements. Static solid-state reactive power (VAr) compensators were proposed based on three topologies, current source inverter (CSI), unrestricted frequency converter (UFC) and voltage source inverter (VSI) as illustrated in Figures 2.7-2.9, respectively. Gyugyi's principle encapsulated both leading and lagging current to voltage phase quadrature requirements for an entire SVC in one unit. These systems are known as static synchronous compensators (STATCOM) and in Europe are more commonly referred to as Advanced Static VAr Compensators (ASVC). The term STATCOM or ASVC is defined by the IEEE PES Task Force of the FACTS Working Group as [4]:

Static Synchronous Compensator (STATCOM): *A static synchronous generator operated as a shunt-connected static VAr compensator whose capacitive or inductive output current can be controlled independent of the a.c. system voltage.*

This definition assumes that the compensator is used to provide reactive support at an infinite busbar. Throughout this project the compensator will be referred to as an ASVC unless reference literature (IEEE) is quoted. The characteristics and operation of the three topologies of solid-state VAr compensators proposed by Gyugyi [5] are summarised in this section. A more detailed description of the voltage source inverter (VSI) based shunt compensator, currently considered the most practical compensator for high power applications, is given in the subsequent section.

2.5.1 THE CURRENT SOURCE INVERTER (CSI) BASED SVC

By utilising an inductively loaded a.c./d.c. six-pulse converter, shown in Figure 2.7, a current source type VAr generator can be realised. The converter may be line-commutated or force-commutated utilising conventional thyristors or devices with a turn off capability. The naturally (line) commutated converter can only provide lagging (absorb) reactive power compensation. To enable leading (generating) reactive current the converter must have its inputs shunted by three appropriately rated capacitor banks such that the combined current drawn from the a.c. system becomes leading as the converter current is decreased [5]. The force-commutated configuration will have anti-parallel diodes with its power switching devices and therefore will provide both lagging and leading VArs.

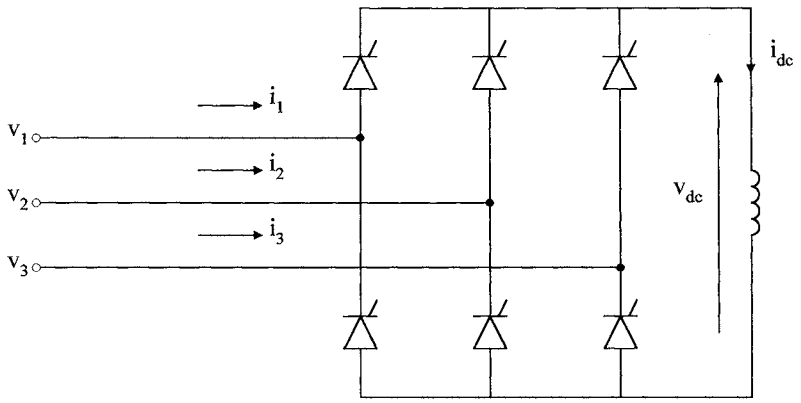


Figure 2.7 – Current Source Inverter (CSI) power circuit

2.5.2 THE UNRESTRICTED FREQUENCY CHANGER (UFC) BASED SVC

The unrestricted frequency changer based SVC is an alternative method of the operating principles of the rotating synchronous condenser, shown in Figure 2.2. The UFC SVC topology, as illustrated in Figure 2.8, can be implemented in two forms. Either utilising a high frequency generator or a multi-phase static oscillating LC tank circuit with a static a.c./a.c. frequency converter such as a force commutated cycloconverter. Considering Figure 2.8(a), a generator of relatively high frequency feeds a static a.c./a.c. frequency changer that converts

the generator frequency to the a.c. system frequency. By controlling the converter output voltages, in phase with the a.c. system voltages, by simple amplitude control the reactive power can be supplied in either direction to the a.c. system. Since the high frequency generator theoretically handles only reactive power it can be replaced with a multi-phase static oscillating LC tank circuit, as shown in Figure 2.8(b) [5].

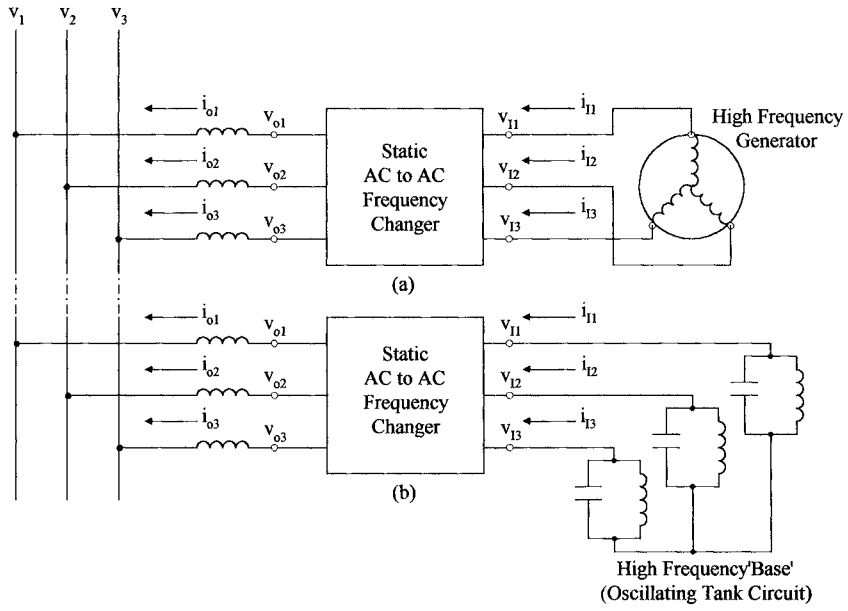


Figure 2.8 – Voltage Source SVC using a.c. to a.c. frequency changer. (a) Conventional high frequency a.c. source arrangement. (b) Self-sufficient LC tank circuits (HF base) operation.

2.5.3 THE VOLTAGE SOURCE INVERTER (VSI) BASED SVC

The voltage source inverter based SVC, shown in Figure 2.9, is essentially a static realisation of the conventional rotating synchronous condenser shown in Figure 2.2. The 'exciter' or d.c. voltage source shown in Figure 2.9 can be one of two forms, a d.c. voltage supply or storage capacitor, as illustrated in Figure 2.9.

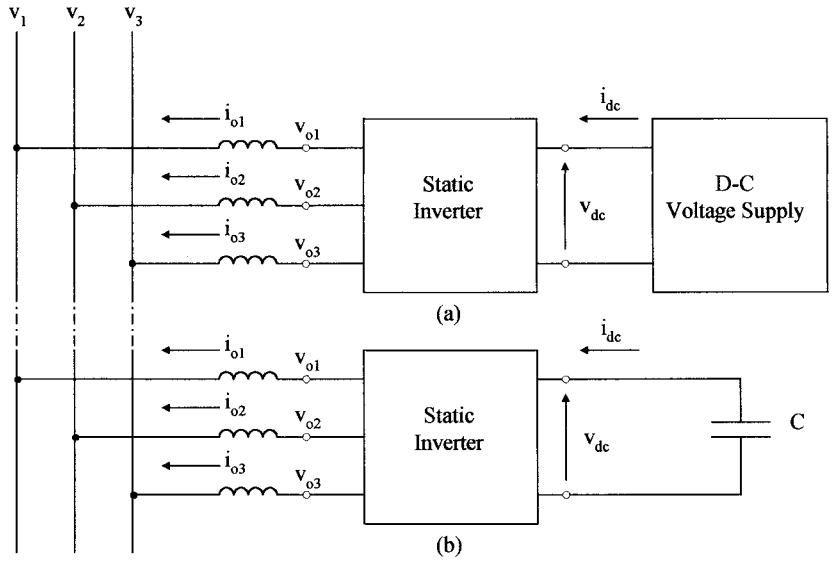


Figure 2.9 – Voltage Source SVC using a d.c./a.c. inverter. (a) Conventional d.c. supply arrangement. (b) Self-sufficient storage capacitor operation.

By controlling the 3-phase inverter output voltages to be in phase with the a.c. system voltage the direction and magnitude of reactive current can be controlled through amplitude control of the output voltages. As with the excitation principles of the synchronous condenser, increasing the amplitude of the inverter output voltages (V_{o1} - V_{o3}) above the a.c. system voltages ($V_1 - V_3$) causes the generation of reactive power, whereas decreasing the inverter output voltage below the a.c. system voltage causes absorption of reactive power. It should be noted that due to the losses associated with the system a small amount of real power is made to flow from the a.c. system under both leading and lagging compensation modes.

The first reported solid-state static VAr compensator using force-commutated thyristors was reported for a 20 MVAr installation by Sumi in the early 1980s [12]. Edwards then demonstrated the feasibility of the new generation of reactive power compensators using GTO's in a ±1 MVAr experimental installation [13]. Then, in 1993 Mori reported an ±80 MVAr installation in Japan [14]. Since the initial proposal of the solid-state VAr compensator both CSI and VSI inverter

topologies have been investigated for suitability as a stand-alone compensator [15,16,17,18]. The development of the practical installations and research has shown the VSI topology to be most suitable, and therefore favoured, for the application due to comparatively low losses and overall improved performance.

OPERATING PRINCIPLES OF THE VSI BASED ASVC

Many publications have demonstrated the operating principles and overall control of the VSI based ASVC. The general operating principles are described here assuming a 'black-box' VSI power circuit. Initially the harmonic performance and the losses associated with the inverter are neglected. The system is also assumed to be operating at steady-state. The basic system is shown schematically in Figure 2.10. When viewed from the a.c. system perspective the ASVC appears as a voltage source, coupled to the line voltage through a small reactance (usually the per-phase leakage inductance of a transformer), which produces fundamental and harmonic voltages. For the following analysis, harmonics are neglected and the ASVC is seen as a pure voltage source.

A purely reactive power flow exists if the inverter output voltages are controlled to produce a balanced 3-phase output in phase with the a.c. system voltage. Due to the inherent characteristics of the coupling components used to connect the ASVC to the a.c. system, the line current flowing into or out of the VSI is ideally 90° to the system voltage.

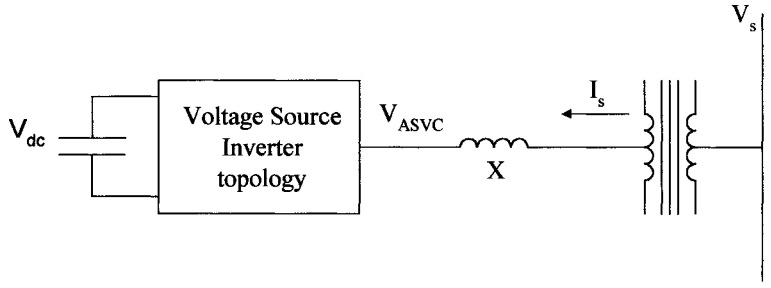
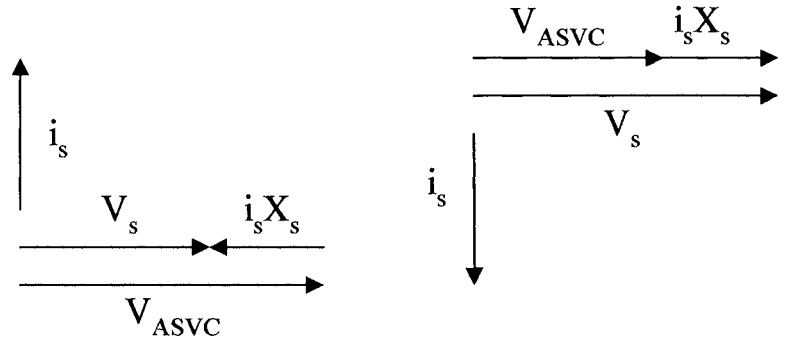


Figure 2.10– Schematic diagram of VSI based ASVC

Under steady-state conditions the ASVC absorbs a leading reactive current if the inverter output voltage amplitude (V_{ASVC}) is larger than the a.c. supply voltage (V_S). This is illustrated with the phasor diagram shown in Figure 2.11(a). This mode of operation is known as the leading reactive compensation mode. If the inverter output voltage is less than the a.c. supply voltage then a lagging reactive current is drawn from the a.c. power system, as illustrated in Figure 2.11(b). This mode of operation is known as the lagging reactive compensation mode. If the amplitude of the inverter output voltage is equal to the a.c. system voltage then, ideally, the reactive power exchange is zero and the ASVC is considered in a floating state.



(a) Leading mode (b) Lagging mode

Figure 2.11 – VSI based ASVC Steady-State Phasor Diagrams

The amount of reactive power exchange between the ASVC and the system, in both modes of operation can therefore be adjusted by controlling the magnitude of the ASVC output voltage. Because there is no real power exchange, I_S is a purely reactive current and the reactive power exchanged by the ASVC can be given by:

$$Q = \frac{1 - \frac{V_{ASVC}}{V_S}}{X} V_S^2$$

The d.c. side voltage, which may be controlled via the phase angle control of the switching strategy applied, determines the magnitude of the VSI output voltage. It can therefore be stated that the d.c. voltage level, V_{dc}, determines the quantity of reactive power generated or absorbed by the ASVC.

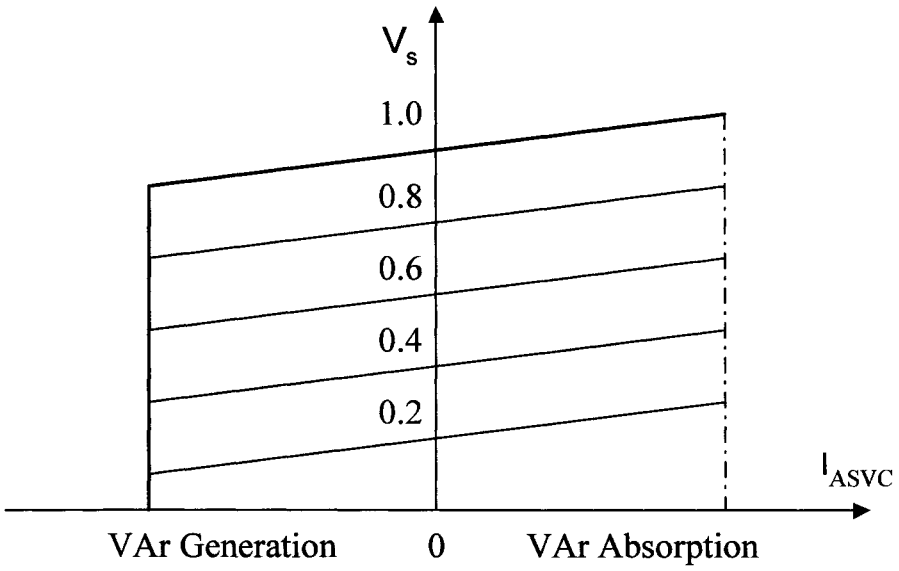
In a practical system, the assumptions of ideal sinusoidal output and no losses are obviously untrue. If the ASVC were to maintain its output voltages exactly in phase with the a.c. system voltages there would be no real power exchange. Therefore, the d.c. capacitors would not only have to maintain a controlled voltage level for the required reactive power compensation, but also supply the real power for the losses. This would result in the d.c. capacitors discharging over a period of time. Due to this fact a small phase difference (δ) is created, through the VSI modulation scheme, between the ASVC output voltage and the system voltage. This is needed to supply the small amount of real power to compensate for the system losses and also to maintain the d.c. capacitor voltage at the required level for compensation. This phase angle control technique is also how the ASVC is controlled during the transient operation. If the angle (δ) is controlled such that the real power delivered is greater than required for the losses then the d.c. capacitor voltage will rise. Hence, moving the system into the leading mode of operation. Whereas, if the phase angle is controlled such that real power is drawn from the capacitor banks, the voltage will drop and the system will move into the lagging mode of operation. The real power exchange between the system and the ASVC is given by:

$$P = \frac{V_{ASVC} V_S}{X} \sin(\delta)$$

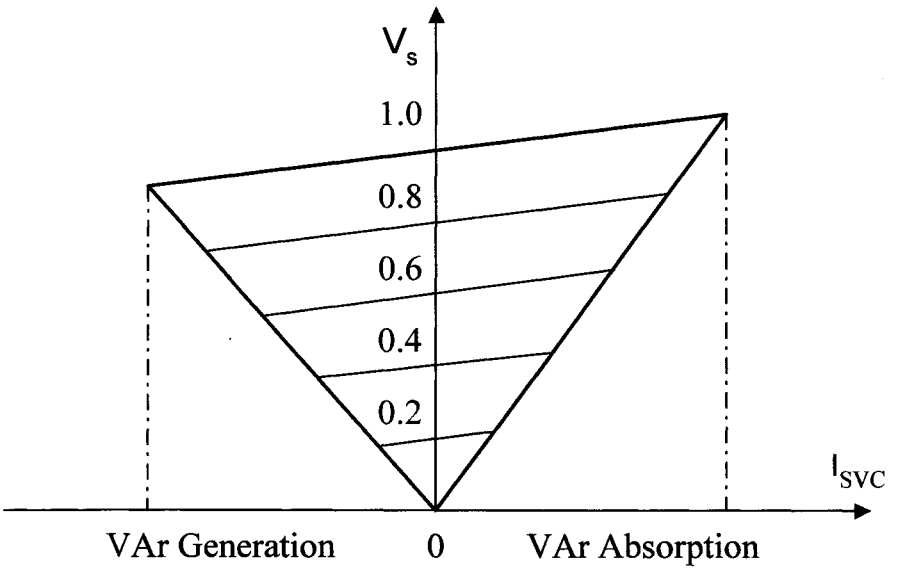
With regards to the ideal sinusoidal output, for a high power ASVC application the implemented switching strategy frequency will be restricted due to power losses. Hence, the output voltage will be a formulation of square waveforms dependant upon the pulse width modulation (PWM) scheme and will therefore contain harmonic components. Resulting from this the total 3-phase instantaneous

power will not equate to zero and in order to maintain this equality the inverter will draw a fluctuating current from the d.c. capacitor. The ripple current waveform is typically a function of the harmonic components of the ASVC output voltage. Investigations into the d.c. ripple waveforms and their overall effect of the harmonic performance of the ASVC system will be presented in Chapter 9. It is apparent that the d.c. capacitors not only perform an important role in the ASVC system performance but also a large part of the total system cost. An investigation into the appropriate sizing of the d.c. capacitors is essential for the practical application of the ASVC system.

To conclude this introduction into the ASVC, it is worth noting that due to the generation or absorption of reactive power being controlled by the inverter a.c. output voltage, the reactive power output can be controlled independent of the a.c. supply voltage. The reactive current values available from the ASVC are only dependant upon the system rating. Comparing the V-I characteristics of the conventional SVC to the ASVC, shown in Figure 2.12, illustrates the superiority of the ASVC in providing voltage support [11]. This results from the reactive current of the conventional SVC being directly proportional to the a.c. system voltage.



(a) Advanced Static VAr Compensator



(b) Static VAr Compensator

Figure 2.12 – V-I Characteristics for the ASVC and SVC

3 SHUNT STATIC VAR SYSTEM (SVS) TOPOLOGIES

3.1 INTRODUCTION

When investigating FACTS shunt compensation technology, it is important to have a general understanding of the options available for the various circuit topologies. Therefore, it is necessary to have an understanding of the past, present and future power semiconductor options together with the 1st and 2nd generation of available power circuit concepts and topologies for FACTS VAr compensators.

This Chapter presents an overview of the available power semiconductor devices and typical topologies implemented in the 1st and 2nd generation shunt FACTS VAr compensators. The SVC and ASVC are presented with characteristics of operation, comparative analysis and reference to industrial application.

3.2 POWER ELECTRONIC DEVICES USED IN SHUNT VAR COMPENSATORS

FACTS technology using thyristor based equipment to improve the utilisation and quality of a.c. networks have been implemented effectively now for many years. More recently equipment requiring fully controllable power electronic devices have emerged at various installations. The advances in power semiconductor devices heavily effect the development of this equipment [19]. In general, power electronic devices can be separated into three groups:

- Uncontrolled – such as a power diode.
- Semi-controlled – also referred to as latching devices, these are turned on via the gate but require circuit commutation in order to extinguish current flow.
- Fully controlled – with these devices the current flow can be both initiated and extinguished by gate control.

Although power diodes are not controllable, they play a very important role in improving the performance of the switching devices used in the power circuitry. They provide a freewheeling element to power devices used in converter applications, such as GTO's and IGBT's. Conventional converter grade diodes have been found to be too slow for these applications and this has resulted in the emergence of fast recovery diodes.

The semi-controlled thyristors are often referred to as the 'workhorse' of the power electronics business. Utilised in series and parallel to increase power ratings, thyristors have been used throughout shunt compensation systems such as the TCR and TSC schemes for many years. The conventional thyristor has been the device of choice for almost all HVDC projects, some FACTS controllers, and a large number of industrial applications [4]. The 2nd generation FACTS VAr compensators require the switching elements to have turn-off capabilities so that the converter can both generate and absorb reactive power. Examples of high power semiconductor devices with a fully controlled capability that are suitable for the FACTS VAr compensators include:

- Gate Turn-Off (GTO) Thyristor – high power (5-8 kV)
- Insulated Gate Bipolar Transistor (IGBT) –low to medium power (3-5 kV)
- Integrated Gate Commutated Thyristor IGCT – high power (state-of-the-art / future)

The phase limbs of a converter are an assembly of valves and each valve is an assembly of power devices. Several schemes have been implemented to generate controllable reactive power by using various power electronic switching converters and there are several reports conducting comparative analysis of the devices [9,11,19,20,21]. The results have indicated that it is favourable to utilise the GTO, IGBT and more recently the IGCT.

The main factors influencing the selection of a power device can be ultimately reduced to a compromise between performance and overall cost. Utilising devices with the highest possible current and voltage ratings should be considered but the

apparent advantage of requiring fewer devices can be outweighed by disproportionately higher device and auxiliary component costs, poorer dynamic performance or higher losses. A cost comparison of power electronic systems using GTO's and IGBT's was carried out by Lorenz [20] and shows a big margin in favour of IGBT's.

The GTO thyristor is still the present choice for industrial high power FACTS equipment requiring fully controllable devices, despite its complicated gate drive and snubber circuits. The device enables high current turn-off capabilities with high voltage blocking ratings and, subject to selection for matched characteristics and attention to equipment design, it can be used in series strings. These factors have recently been improved with the development of the IGCT. The application of the GTO is usually limited to low frequency, typically below 1 kHz, due to the high switching losses associated with the device.

As this project investigates the inherent redundancy of a converter topology in the event of a device fault it is also worth noting that the device selection must consider possible fault scenarios to predict current and voltage margins and the requirement for possible device redundancy. In general, power devices fail short circuit enabling continual operation at a valve if the topology, control scheme and remaining device ratings are suitable.

The IGBT does not yet have ratings comparable with the GTO but it offers much lower switching losses and is therefore better suited to higher switching frequency applications above 1 kHz. Voltage and current ratings of IGBT's are increasing rapidly. IGBT's also have a minimal gate drive and snubbing requirement. For these reasons, and also cost considerations, the IGBT has remained the preferred device for laboratory research implementations and will be utilised in the construction of the power circuit for this project.

3.3 STATIC VAR COMPENSATOR TOPOLOGIES – 1ST GENERATION FACTS

Static VAr Compensators (SVC) installed in power transmission systems serve in various ways to improve the system performance. By rapid control of their reactive power output, improvements in transmission system performance attributable to SVC's may include [22,23]:

- Increased steady-state transmission capacity and enhanced transient stability (resultant from intermediate bus voltage support)
- Improved system dynamic stability by damping of increased system swing
- Reduced voltage flicker from irregular load fluctuations
- Control of steady-state and temporary overvoltages
- Improved transmission system efficiency and load power factor by connection of local VAr supply
- Damping of sub synchronous oscillations
- Correction of phase imbalance or compensation of irregular 1-phase loads

The SVC system is essentially an integrated system of static electrical components and shunt reactive elements that, through control of the variable reactive admittance, makes the SVC inject or absorb reactive power. Thereby maintaining the desired value of voltage at the point of common coupling (PCC). There have been many configurations to construct SVC systems combining the fixed capacitor (FC), thyristor-controlled reactor (TCR) and thyristor-switched capacitor (TSC)[24]. There are several SVC system topologies and control methodologies proposed and developed to meet transmission system requirements. As with most multi-application systems each SVC scheme has specific advantages and disadvantages relative to the other SVC types. The choice of SVC configuration can depend on the required steady-state characteristics, the operating requirements peculiar to the transmission system under small and large system disturbances, limitation on harmonics generated by the SVC, the SVC losses and the overall cost [4]. An overview of the most common configurations and there characteristics is presented here.

3.3.1 TCR TOPOLOGIES

It was presented in section 2.4.2. that, due to the phase control implemented in the TCR scheme, the output current for a standard six-pulse structure would contain low order harmonics (i.e. 5^{th}, 7^{th}, etc.). As this would not be suitable, for a high power SVC application, harmonic reduction techniques are implemented. Two methods suitable for cancelling or reducing the amplitude of the harmonics are shown in Figures 3.1 and 3.2, respectively. The m (m ≥2) parallel-connected (segmented) TCRs, each with 1/m of the total rating required are 'sequentially' controlled (i.e. one is phase controlled whilst the others are on/off), thereby reducing the amplitude of every harmonic by the factor m with respect to the maximum rated fundamental current [4]. With the 12-pulse TCR arrangement, shown in Figure 3.2, the harmonics can be cancelled due to the 30° phase displacement obtained from the star-delta 3-windings transformer arrangement. Generally, the low order harmonic currents 5^{th}, 7^{th}, 17^{th} and 19^{th} cancel resulting in a nearly sinusoidal output current. A twelve-pulse system gives a better a.c. waveform than the six-pulse system and is therefore mainly utilised in high power applications which have more stipulated demands on the harmonic quality of the current waveform.

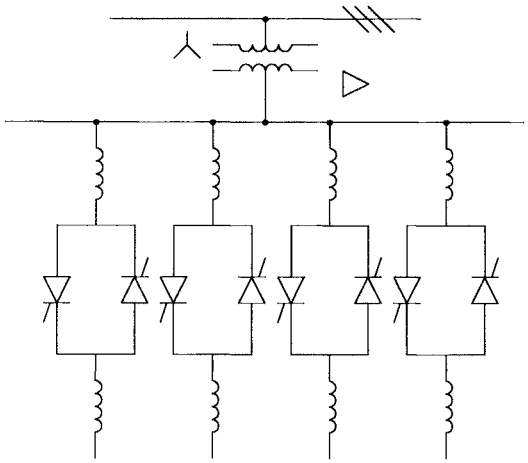


Figure 3.1 – Segmented TCR scheme

Further harmonic cancellation is possible by operating three or more delta connected TCRs from appropriately phase shifted voltage sets. In practice however, 18 and higher pulse circuit arrangements tend to be too complex and

expensive. Also it becomes increasingly difficult to meet the requirements for symmetry, due to possible unbalance in the a.c. system voltages. For these reasons, circuit configurations higher then 12-pulse are seldom used [4].

To further reduce or eliminate the harmonics in the line current shunt passive filters are normally employed in parallel with the TCR system. It should be noted that in many practical applications, due to unbalances or individual phase control of the three TCRs, a tuned filter branch at the 3rd harmonic frequency is also recommended [6].

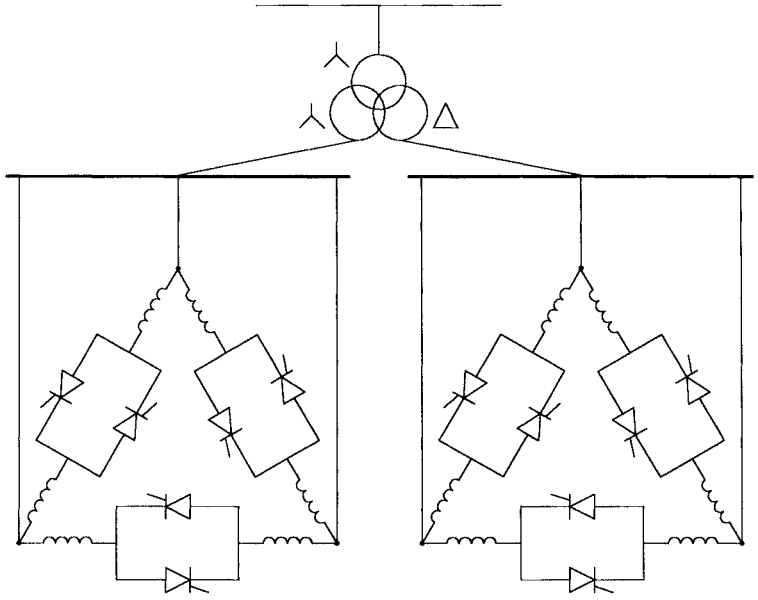


Figure 3.2 – 12-pulse TCR scheme

3.3.2 FIXED CAPACITOR, THYRISTOR CONTROLLED REACTOR (FC/TCR)

The FC/TCR configuration of a SVC system, Figure 3.3, can be controlled to provide continuously variable absorption and generation of reactive power by thyristor control of the reactor current. It is typical to find two or more fixed capacitor banks providing the generation of reactive current. The capacitors deliver reactive power equal to the maximum reactive power consumed by the reactor. The TCR is then rated much larger such that the total fixed capacitance can be effectively cancelled and the system can provide absorption of reactive power. Due to the proportional relationship between the harmonic magnitudes and

the TCR size, the large reactor required in the FC/TCR can be a source of significant harmonics [23]. Therefore configurations of coupling transformers, as presented in section 2.4.2 and utilisation of the harmonic reduction techniques presented in section 3.3.1 is essential for this configuration.

The FC/TCR SVC system is suitable for large power networks in order to improve the dynamic and transient quality of a network [7]. Due to the modular nature of the reactive elements the rating can be increased and with its flexibility in control, the FC/TCR exhibits definite advantages over some alternative schemes. Consequently, it has been thoroughly investigated and implemented for various applications [5,23,25].

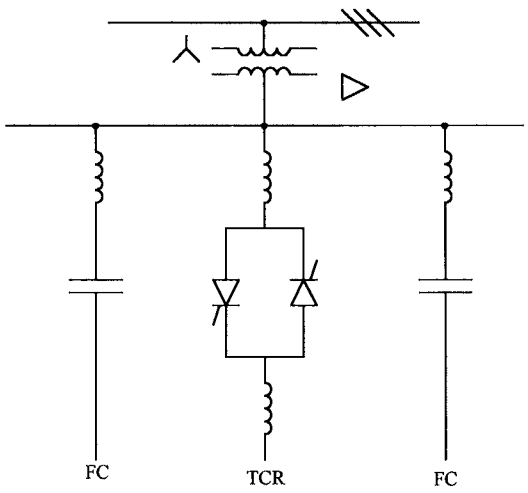


Figure 3.3 – FC/TCR configuration SVC scheme

3.3.3 THYRISTOR CONTROLLED REACTOR / THYRISTOR SWITCHED CAPACITOR (TCR/TSC)

The TCR/TSC type compensator was developed primarily for dynamic compensation of power transmission systems with the intention of minimizing standby losses and providing increased operating flexibility [4]. A typical configuration, shown in Figure 3.4, consists of one TCR and *n* TSC branches with one fixed capacitor (FC) as a tuned filter. Selecting discrete steps of the capacitance with the reactor controlled as usual enables full control of the system. Due to the switching in and out of the capacitor banks there exist conditions when

no harmonic filters are available for attenuation of the TCR output current harmonics. For this reason fixed capacitors used as tuned filters are required. Again to limit harmonics in the output currents multi-pulse or segmented versions of the TCR may be implemented.

When compared to its FC/TCR counterpart, the TCR/TSC has definite advantages in regards to the steady-state losses. When no compensation is required, the reactance and capacitance are disconnected from the power system. However, the overall capital cost of the capacitor switches and increased control complexity are the obvious disadvantages. A premium of 15-20% is typical for the TCR/TSC compared to FC/TCR compensators [23]. The TCR/TSC configuration, before the advent of the 2nd generation of FACTS shunt controllers, was generally considered the fastest, most flexible, low loss static VAr compensator topology.

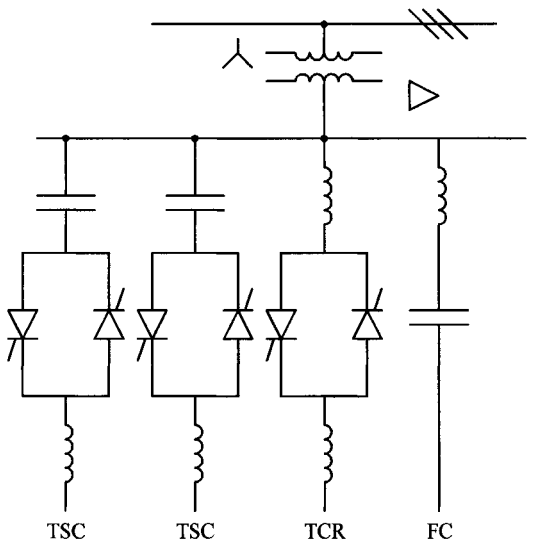


Figure 3.4 – TCR/TSC configuration SVC scheme

3.4 ASVC TOPOLOGIES – 2ND GENERATION FACTS

It is presented in Chapter 2 that a static VAr compensator (SVC) can be realised through a solid-state converter configuration. The most suitable of the three proposed systems being the controlled synchronous voltage source inverter (VSI) usually referred to as the Advanced Static VAr Compensator (ASVC). Together with the improvements in transmission system performance that have been given for the conventional SVC in section 3.3, the use of the VSI based ASVC permits faster control as well as the potential for a reduction in the system footprint.

The initial proposal of the VSI based ASVC demonstrated the principles of operation with a standard six-pulse bridge. However, over the years this has evolved into number of topologies proposed as suitable for the ASVC application. Together with multi-pulse arrangements a various number of multi-level configurations have been presented and investigated. This section summarizes the available VSI topologies suitable for the ASVC application. The basic fundamental frequency modulation (FFM) operation of the inverters is presented. Higher switching frequency PWM strategies and methods of harmonic cancellation are investigated in a later Chapter.

3.4.1 SIX-PULSE VOLTAGE SOURCE INVERTER (VSI)

The six-pulse VSI power circuit consists of switching devices and inverse-parallel diodes, as is shown in Figure 3.5. As illustrated, the standard three-phase topology is similar to its standard single-phase counterpart with the expansion of a third leg, limb or phase. With the advent of the multi-level terminology this topology structure is commonly referred to as the 2-level structure due to its two operational voltage levels, positive or negative. This serves as a good method to bring the topology into the multi-level terminology, but it should be stated that this is not strictly a multi-level system.

With the wide spread use of space vector modulation and digital vector control, the VSI output voltages can be referred to in 'state' form. This terminology relates to the attainable three-phase switching states of the output voltages. Although this 'state' analysis is utilised in the topology redundancy analysis in the following Chapter, for simplicity its full implementation is not required here and only the on/off conditions of the switches are used.

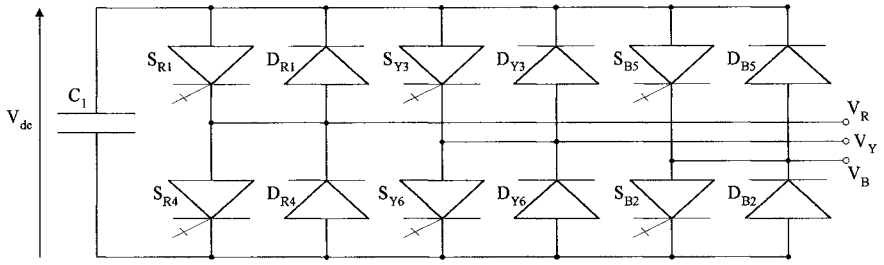


Figure 3.5 – Six-pulse VSI power circuit

The phases to 'zero' and the line-to-line voltages for the six-pulse inverter are shown in Figure 3.6. The standard 180° fundamental frequency modulation (FFM) scheme is applied, as shown in Table 3.1, where the rate of sequencing these patterns specifies the inverter output frequency.

Switching State (1 = on, 0 = off)						Output Voltage Level		
S_{R1}	S_{R4}	S_{Y3}	S_{Y6}	S_{B5}	S_{B2}	V_{R0}	V_{Y0}	V_{B0}
1	0	1	0	0	1	$+V_{dc}$	$+V_{dc}$	$-V_{dc}$
0	1	1	0	0	1	$-V_{dc}$	$+V_{dc}$	$-V_{dc}$
0	1	1	0	1	0	$-V_{dc}$	$+V_{dc}$	$+V_{dc}$
0	1	0	1	1	0	$-V_{dc}$	$-V_{dc}$	$+V_{dc}$
1	0	0	1	1	0	$+V_{dc}$	$-V_{dc}$	$+V_{dc}$
1	0	0	1	0	1	$+V_{dc}$	$-V_{dc}$	$-V_{dc}$

Table 3.1 – FFM switching sequence for the six-pulse inverter

Fourier analysis shows that the phase to 'zero' for the 'red' phase and 'yellow' and hence the 'red-yellow' line-to-line voltage can be obtained as:

$$V_{R0} = \frac{4V_{dc}}{\pi}\left[\sin\omega t + \frac{1}{3}\sin 3\omega t + \frac{1}{5}\sin 5\omega t + \frac{1}{7}\sin 7\omega t + ...\right]$$

$$V_{Y0} = \frac{4V_{dc}}{\pi}\left[\sin\left(\omega t - \frac{2\pi}{3}\right) + \frac{1}{3}\sin 3\left(\omega t - \frac{2\pi}{3}\right) + \frac{1}{5}\sin 5\left(\omega t - \frac{2\pi}{3}\right) + \frac{1}{7}\sin 7\left(\omega t - \frac{2\pi}{3}\right) + ...\right]$$

$$V_{RY} = \frac{4\sqrt{3}V_{dc}}{\pi}\left[\sin\left(\omega t + \frac{\pi}{6}\right) - \frac{1}{5}\sin 5\left(\omega t + \frac{\pi}{6}\right) - \frac{1}{7}\sin 7\left(\omega t + \frac{\pi}{6}\right) + \frac{1}{11}\sin 11\left(\omega t + \frac{\pi}{6}\right) + ...\right]$$

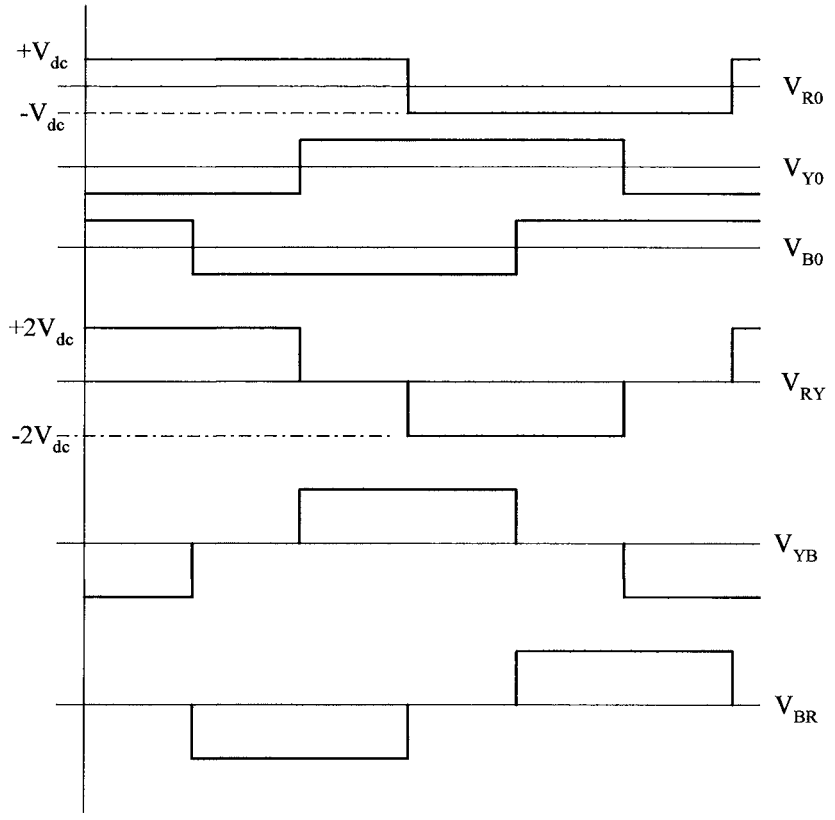


Figure 3.6 – Six-pulse VSI phase and line voltages with 180° FFM

Therefore it can be concluded that with 180° FFM of the six-pulse VSI, harmonics of the order 6k±1, where k=1,2,3... remain in the line output voltage waveform. As with standard square-wave Fourier analysis, for these 'ideal' circuits the k^{th} harmonic component has a 1/k amplitude relative to the fundamental component.

3.4.2 MULTI-LEVEL VSI TOPOLOGIES

The problems associated with series connection of power semiconductor devices and the requirements to limit switching losses have limited the use of a stand-alone six-pulse VSI for high power applications. The multi-level VSI topology has two essential features [26]:

- It enables the possibility of a high voltage at the a.c. side of the inverter without the problems related to the concurrent switching of series connected devices. This is of particular importance when a high d.c. side voltage is typical of the application such as in VAr compensation systems.
- As more levels are available to construct a sinusoidal shape for the a.c. side waveforms, a smaller distortion can be achieved even at low switching frequencies per device.

Throughout the last decade the concept of a 'multi-level converter', proposed as 'a new breed of power converters' [27], has received enormous interest for applications ranging from medium to high power. A variety of multi-level topologies have been proposed, and in some cases implemented into high power applications [27,28]. The three main multi-level converters are the diode clamped multi-level inverter (DCMLI), the flying capacitors topology and the cascaded inverters with separate d.c. sources. This section presents the basic operating principles of these three multi-level topologies together with their respective advantages and disadvantages.

3.4.2.1 DIODE-CLAMPED MULTI-LEVEL INVERTER (DCMLI)

The diode-clamped multi-level inverter has evolved from the Neutral-Point-Clamped (NPC) inverter proposed by Nabae [29]. The 3-level NPC inverter has found uses in various applications and still remains the favoured multi-level topology for high power applications. Since its initial proposal various authors have extended the diode clamping structure into both odd and even topologies [30, 31]. An optimisation study of levels ranging from 3 to 14 indicated that the 6-level topology offers the most suitable characteristics for high power applications [32]. More recently various authors have published variations of the 3-level DCMLI topology and investigations into the neutral point voltage balancing problems proposing improvements in the overall performance [33, 34].

One phase limb of the 5-level DCMLI structure is illustrated in Figure 3.7. As the converter name indicates the inverter uses clamp diodes connecting the sections of the main power circuit to a string of capacitors. Therefore, dividing the d.c. bus voltage into a number of voltage levels. The pattern of the output voltage levels is dictated by the switching strategy implemented by the system controller. A standard 5-level fundamental frequency strategy is illustrated in Table 3.2.

Switching State (1 = on, 0 = off)								**Output Voltage Level**
S_{R1}	S_{R2}	S_{R3}	S_{R4}	S_{R5}	S_{R6}	S_{R7}	S_{R8}	V_{RN}
1	1	1	1	0	0	0	0	$+2V_{dc}$
0	1	1	1	1	0	0	0	$+V_{dc}$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_{dc}$
0	0	0	0	1	1	1	1	$-2V_{dc}$

Table 3.2 – Standard FFM switching scheme for a 5-level DCMLI

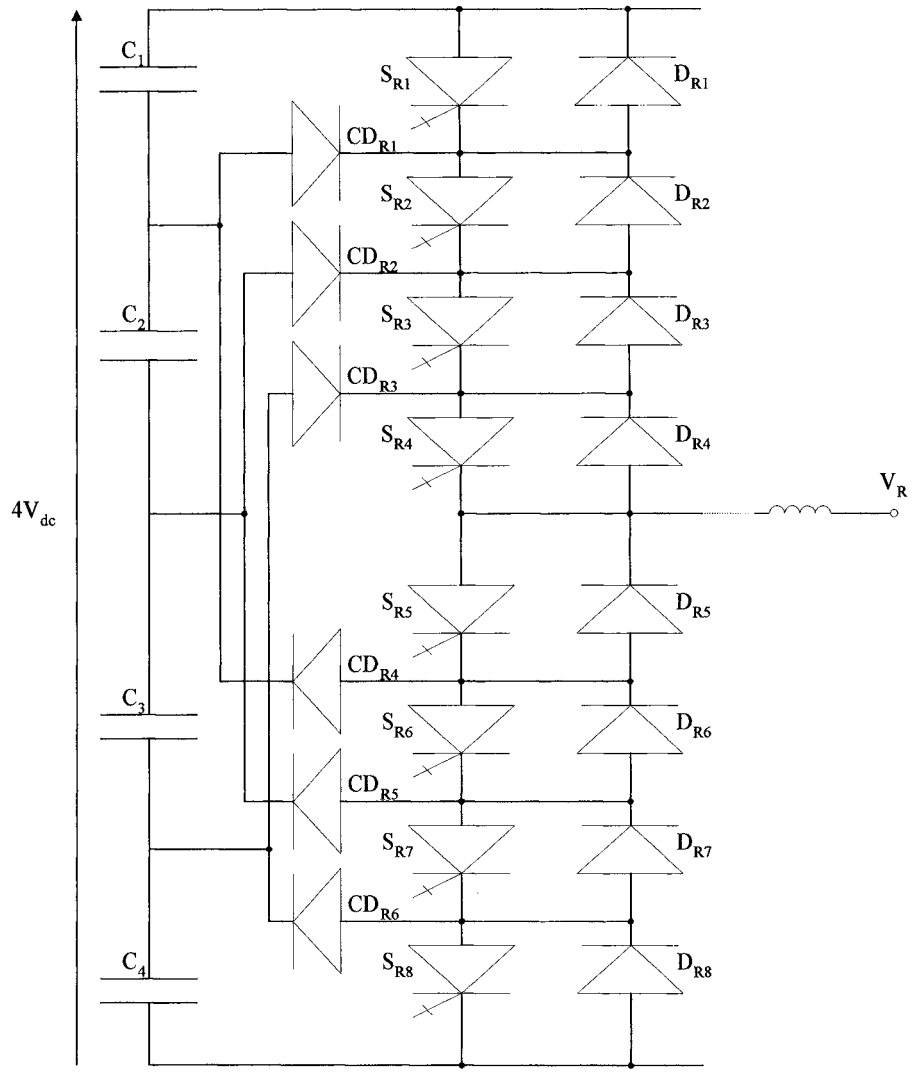


Figure 3.7 – Phase Limb of a 5-level diode-clamped VSI

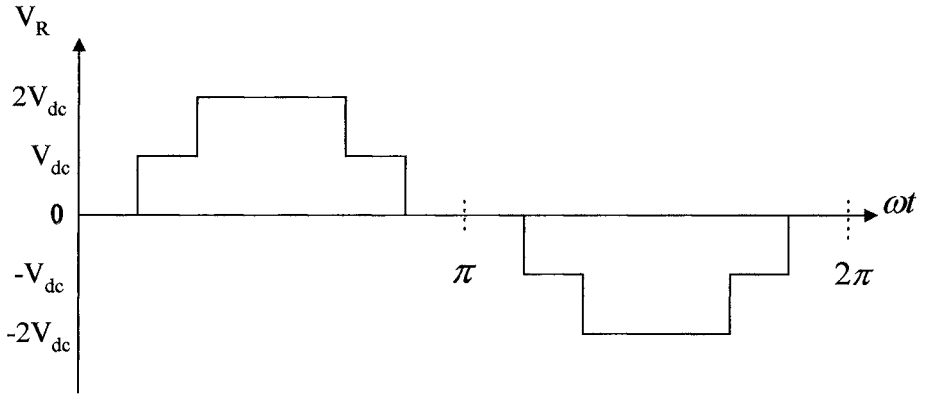


Figure 3.8 – Output Phase Voltage of a five-level inverter

The typical synthesized staircase voltage waveform obtained from a 5-level VSI operated at fundamental frequency is shown in Figure 3.8. The advantages and disadvantages of a diode-clamped multi-level voltage source inverter topology can be summarized as follows [35].

Advantages:

- Low harmonic content in the output due to the possibility of high number of levels, which minimizes filtering requirements, and possibly avoiding transformers.
- As devices are typically switched at low frequency the system exhibits high efficiency – low power losses.
- Control of reactive power (VAr) flow.
- Moderately simple control method.

Disadvantages:

- Number of clamping diodes becomes excessive if number of levels is high.
- Without effective control the capacitor voltage unbalance is seriously detrimental to the performance.
- Real power flow control can be difficult for individual inverters.

3.4.2.2 FLYING CAPACITOR CONVERTER (FCC)

The power circuit of a flying capacitor multi-level inverter utilises separate capacitor banks. For a 5-level topology, illustrated in Figure 3.9, four capacitor banks precharged to V_{dc}, $(3/4)V_{dc}$, $(1/2)V_{dc}$ and $(1/4)V_{dc}$ are used to give voltage increments that define the voltage steps in the output waveform. The outer capacitor bank, V_{dc}, is usually fed from a 3-phase rectifier [36] and is common to all phases. Whereas, the inner-loop balancing capacitors float and are independent to each phase limb. The phase voltage levels can be synthesised through various different strategies such that addition or subtraction of the capacitor voltage takes place.

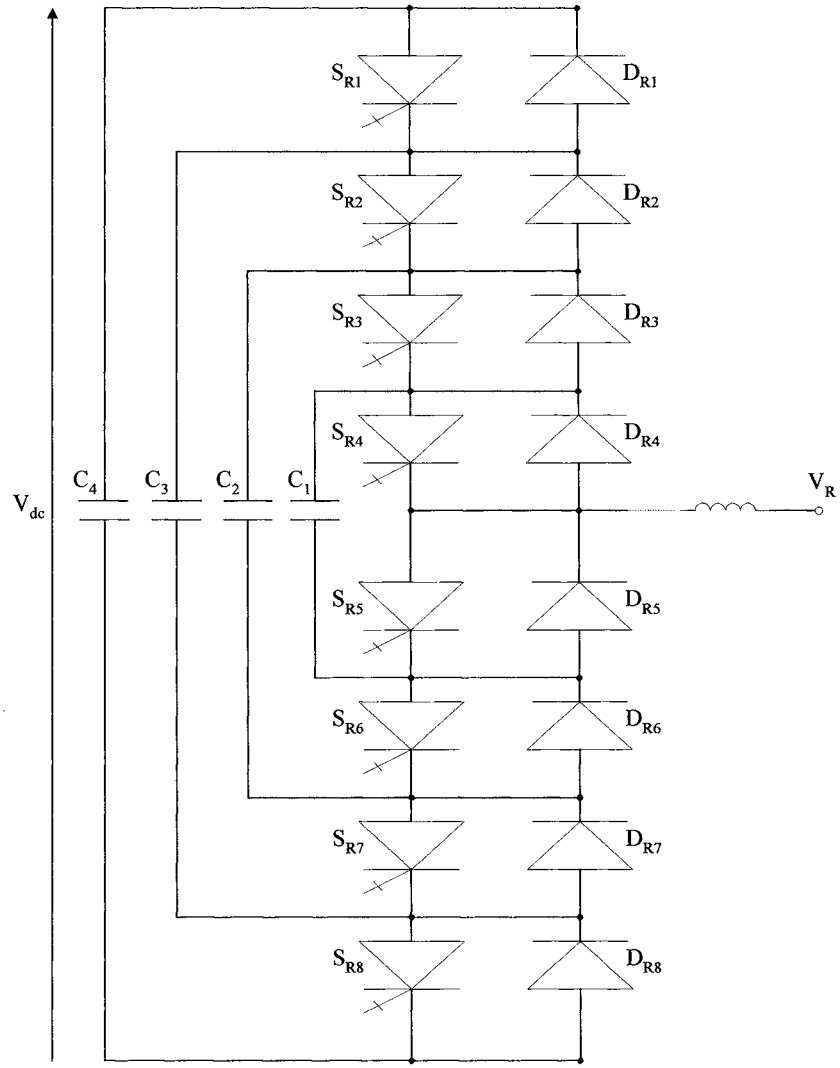


Figure 3.9 – Phase Limb of a 5-level flying capacitor based VSI

A possible switching strategy for the 5-level flying capacitor multi-level circuit is illustrated in Table 3.3. The Red phase output voltage is illustrated with respect to the negative d.c. rail. Switching operations should always be controlled in order to prevent short-circuit paths between the capacitors and to maintain continuous current to the main d.c. bus capacitor [28].

Switching State (1 = on, 0 = off)								Output Voltage Level
S_{R1}	S_{R2}	S_{R3}	S_{R4}	S_{R5}	S_{R6}	S_{R7}	S_{R8}	V_{RN}
1	1	1	1	0	0	0	0	$+V_{dc}$
1	1	1	0	1	0	0	0	$+3V_{dc}/4$
1	1	0	0	1	1	0	0	$+V_{dc}/2$
1	0	0	0	1	1	1	0	$+V_{dc}/4$
0	0	0	0	1	1	1	1	0

Table 3.3 – Possible Switch Combination for the Flying Capacitor 5-level VSI

The advantages and disadvantages of a flying capacitor multi-level voltage source inverter can be summarized as follows [35].

Advantages:

- Large amounts of storage capacitors provides extra ride through capabilities during power outage.
- Switch combination redundancy provides method for balancing different voltage levels.
- With high enough number of levels the harmonic content will be low meaning less filters.

Disadvantages:

- Excessive number of storage capacitors required when the number of converter levels is high. Required bulky capacitors leads to high-level systems being more difficult to package and more expensive.
- Precharging requirements and start-up can be very complex.
- Very complicated inverter control, and high switching losses for real power transmission.

3.4.2.3 CASCADED –INVERTER WITH SEPARATE DC SOURCES

The final multi-level topology to be presented is the cascaded inverter topology. This structure has attracted much interest over the past few years and is referred to under a number of titles: the cascaded-inverter [35, 37], the chain-link inverter [38, 39] and the binary multi-level inverter [40]. An 'M'-level cascaded circuit, where M indicates the number of inverter units (not the number of voltage levels), is constructed from conventional single-phase bridges connected in series. A typical structure is illustrated in Figure 3.10.

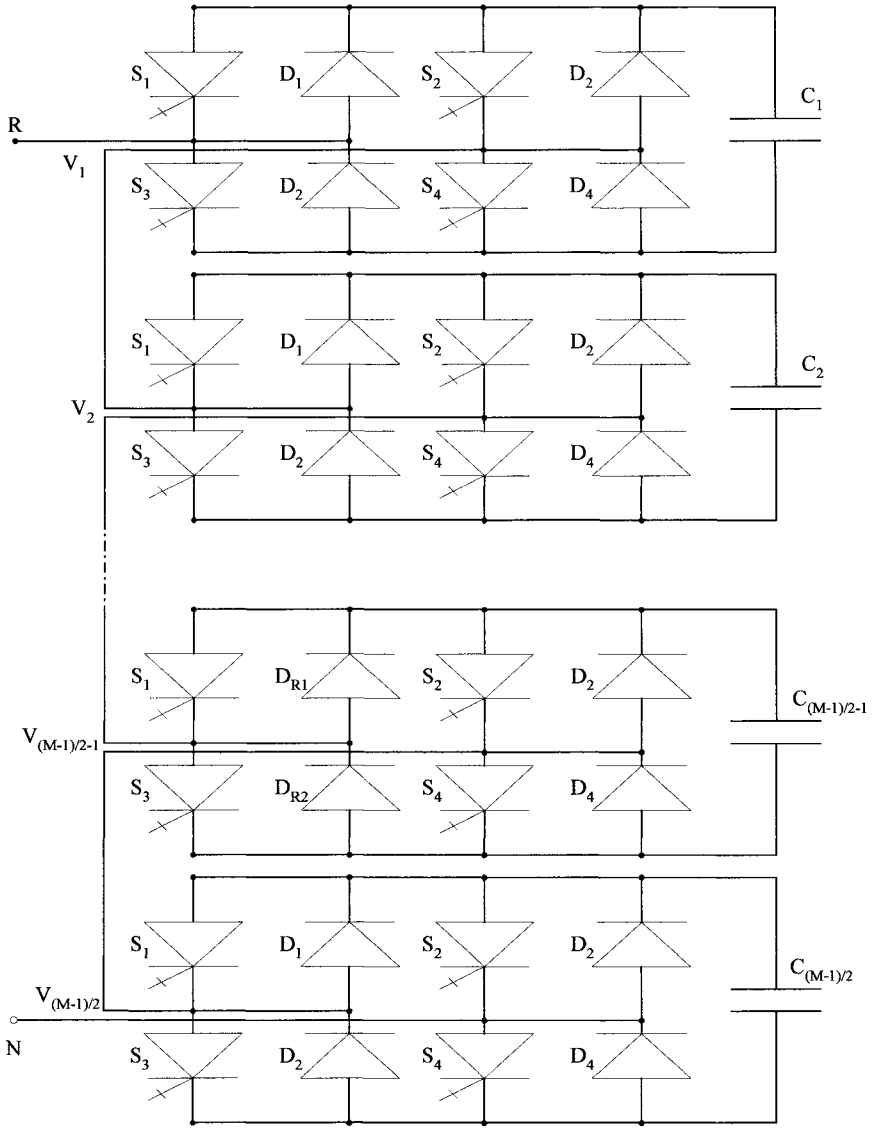


Figure 3.10 - Structure of a 'M'-level cascaded inverter phase limb

The principle of operation of the cascaded inverter is quite simple. Each bridge unit can produce three voltage levels, as with the 3-level DCMLI, which are positive ($+V_{dc}$), negative ($-V_{dc}$) or zero (0V). The 'zero' voltage state is obtained by bypassing the capacitor. Therefore with 'M' links in series the configuration can synthesise a voltage waveform of (2M+1) levels per phase.

This proves extremely beneficial in the elimination of harmonic content. A phase limb configuration with four units can therefore produce a 9-level phase output voltage waveform as illustrated in Figure 3.11. The advantages and disadvantages of the cascaded-inverter based multi-level VSI topology can be summarized as follows [35].

Advantages:

- Requires the least number of components, compared to other multi-level inverters, to achieve the same number of voltage levels.
- As each level has the same structure, modularised circuit layout and packaging is possible. Also, there are no extra clamping diodes or voltage balancing capacitors.
- Soft switching techniques can be used in this structure to avoid bulky and lossy resistor-capacitor-diode snubbers.

Disadvantages:

- For real power conversions the topology needs separate d.c. sources. Its applications are therefore limited.

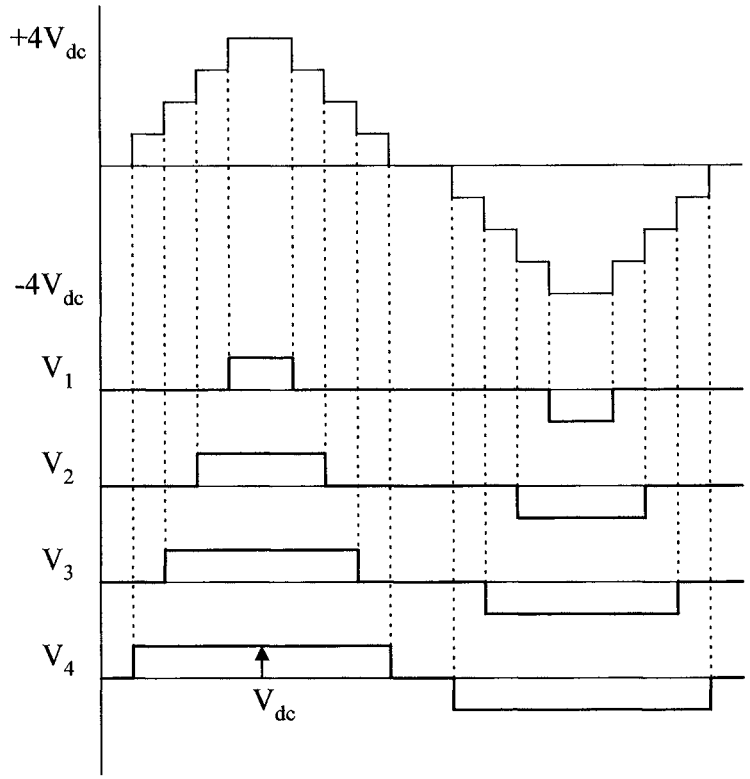


Figure 3.11 – Waveform showing a 9-level cascaded converter phase voltage

3.4.3 MULTI-PHASE / PULSE VSI TOPOLOGIES

High power applications of the VSI topologies restrict the maximum switching frequency in order to minimize the losses. The harmonic performance of the stand-alone six-pulse and the lower-level multi-level topologies are not suitable due to high low order harmonic amplitudes. The quasi-square waveforms obtained from the 2-level (six-pulse) and the 3-level DCMLI would produce unacceptable current harmonics if connected directly to the line. It is therefore usual for industrial applications of the VSI based ASVC to obtain high power and acceptable harmonic cancellation by connecting multiple inverter bridges using complex transformer arrays [11, 41].

These multiple inverter bridge arrangements are known as multi-phase converter topologies. By using a concept of keeping the fundamental in phase and

introducing a pre-defined phase shift in the remaining harmonics of the output voltage of the multiple inverters, which is obtained by connection of a complex electromagnetic interface, a suitable harmonic cancellation/minimisation can be obtained. The pulse number of such an arrangement is generally quoted as six times the number of basic inverters, for multiple six-pulse inverters, and provides an indication of the level of harmonic neutralisation achieved [41]. It is presented in [11] that for transmission line applications a pulse number of 24 or higher is required to achieve adequate waveform quality without passive filters.

For simplicity, only 12-pulse arrangements or dual 3-level VSI configurations are presented here. There have been many investigations published comparing the series and parallel transformer configurations suitable for the dual VSI configurations of the ASVC [42, 43]. With others also comparing not only the transformer configurations but also the series and parallel connection of the d.c. capacitor banks [44]. Due to the problems of low frequency harmonic ripples in the d.c. link voltage, parallel connection of the inverter capacitor banks has been favoured as demonstrated in [12]. As the d.c. link currents meet at two common nodes, their harmonic components are cancelled so the capacitor banks are relatively smaller. Also, the risk of DC-AC harmonic remodulation is apparent if the harmonic components are not cancelled or the capacitor is not large enough, which is further discussed in Chapter 9. However, analysis in [42] has shown that voltage THD requirements can be achieved with series connection of reasonably sized components. Series and parallel connections of the 12-pulse and dual 3-level configurations are illustrated in Figure 3.12.

It is typical through both series and parallel transformer connections for the converter output voltage to be phase shifted by 30°. This is resultant of the star-delta transformer arrangement. Fourier harmonic analysis shows that on the primary side of the transformer the currents only have harmonics of the order $12k\pm1$, where k is any positive integer.

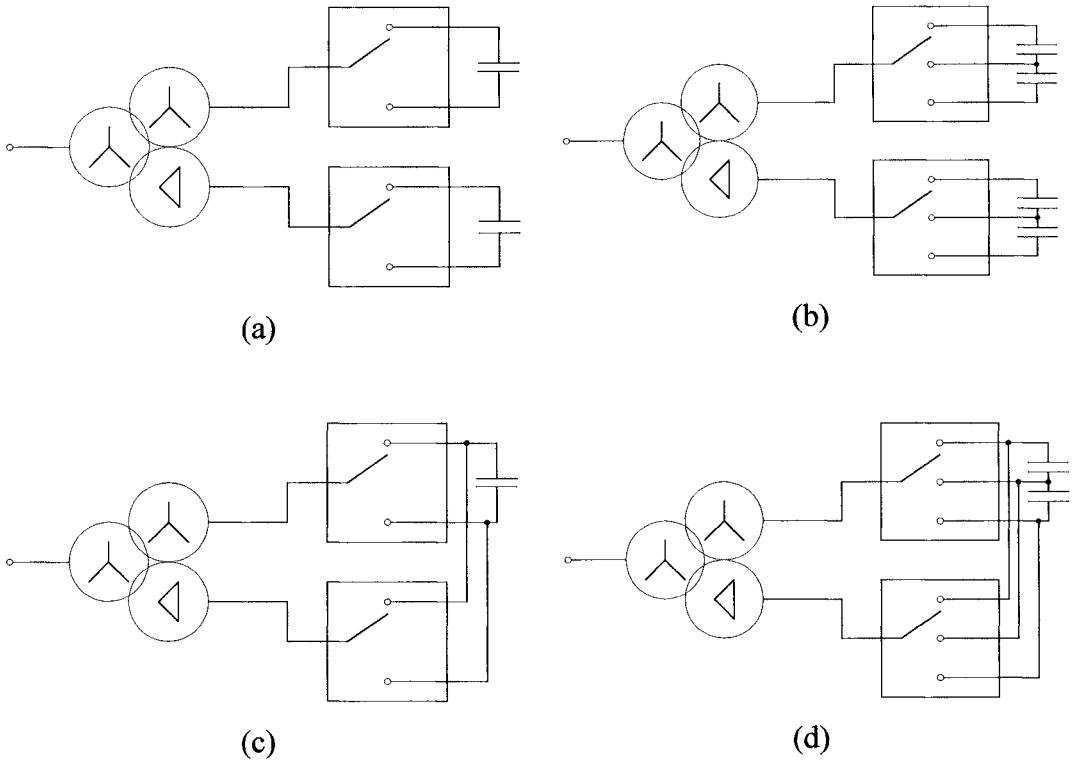


Figure 3.12 – Multi-phase configurations of two and three-level inverter structures (a) 12-pulse series connected capacitor, (b) Dual 3-level series connected capacitor, (c) 12-pulse parallel connected capacitor and (d) Dual 3-level parallel connected capacitor.

3.4.4 COMPARISON OF SUITABLE VSI TOPOLOGIES

As illustrated throughout this Chapter, there are many variations and possible configurations of voltage source inverter topologies that are suitable for the ASVC application.

As described in section 3.4.3, the stand-alone six-pulse or the stand-alone 3-level multi-level structure would not provide acceptable harmonic performance for high power applications. For this reason multi-phase structures have been widely used in industrial applications. The multiple bridge arrangement offers a high voltage

rating, without the problem of numerous series connected devices in each valve, and also a simple control scheme and low switching frequency.

The main disadvantage is that the transformer array required is usually very expensive, complicated and large. Also, continual operation of the configuration in the event of a power circuit fault is not possible, unless suitable device redundancy is provided. A fault will result in the loss of an inverter unit, hence severely affecting the harmonic performance of the system. This will be further discussed in Chapter 4.

The higher-level multi-level configurations are proving a viable option for the ASVC applications. The arrangement of the phase limbs offers a substantial advantage in that as the overall d.c. voltage is distributed across the devices the necessity to connect series devices in independent valves, and therefore the problems associated with this, are avoided. It should be noted however that the multi-level ASVC structures do have there own problems. The switching control scheme is usually more complicated than the multi-pulse arrangements and the problem of d.c. link capacitor balancing in the DCMLI structure is an ongoing investigation.

Comparison of voltage level redundancy between the topologies shows that the two-level (six-pulse) phase voltage levels can only be obtained by one combination of switch selection. For the flying capacitor circuit, each voltage level can be synthesised through various patterns that obviously results in voltage level redundancy. Due to the different voltage constraints of the individual devices in the diode-clamped structure the configuration doesn't offer phase voltage redundancy between the voltage levels. However, this doesn't infer that the DCMLI structure offers no inherent redundancy in the event of a device fault, as will be investigated in Chapter 4.

4 DCMLI INHERENT REDUNDANCY INVESTIGATIONS

4.1 INTRODUCTION

Since the initial proposal of the diode-clamped or Neutral-Point-Clamped (NPC) voltage source inverter (VSI), various multi-level inverter topologies and associated control strategies have been proposed. To date, the highly researched and industrially favoured topology level has been the 3-level diode-clamped multi-level inverter. Although investigations have been presented on DCMLI structures of higher levels [45, 46], they have as yet to appear in industrial applications due to the complexities of control strategies, the inherent difficulties associated with d.c. voltage balancing control and the number of associated semiconductor power devices within the structure.

With the exception of Sinha's investigation into fault protection for the 5-level diode-clamped multi-level structure [47], published work so far has concentrated on the normal operation of the power circuit within the multi-level structure. In 1999 Tolbert presented the possibility of exploiting the redundant switching-states within a multi-level inverter, but this was focused upon redundancy for multi-level PWM at low amplitude modulation indices [48]. It has been an accepted practice that the inverter, comprising of many semiconductor devices, shuts down in the event of any device failure. Shutdown incidents are minimised by providing back-up (redundant) devices incorporated in each valve in the inverter.

A single-phase leg of the 3-level diode-clamped multi-level inverter (DCMLI) structure is illustrated in Figure 4.1. Utilisation of the 3-level diode-clamped VSI topology has proved very effective under normal operating conditions. However, in the event of a device fault the presently applied back-up protection contradicts, and eliminates, some of the advantages of utilising the multi-level topology. The series connection of switching devices, required in the low-level inverter bridges to operate at high voltage rating, leads to voltage sharing problems among devices during switching and hence poor utilisation of device voltage ratings. As a result, the number of devices that can be placed in series is limited. Another

disadvantage of series connection of the devices is that all devices could be subjected to a common mode fault, for example due to a system side transient. The desired series redundancy is thus not achieved. An expected advantage of the multi-level topology is the reduced requirement for series connection as, for an 'N'-level inverter, each device has a nominal blocking voltage of $V_{dc\ (total)}$ / (N-1). This minimizes the voltage-sharing problem, as the voltage stress on each device is well controlled and far less than the full bus voltage [49]. However, redundant switching devices to be utilised in the event of a device failure are still connected in series within each valve comprising the DCMLI leg. Another disadvantage, in addition to the series limitations, is the increased hardware requirements and overall losses. It is also recognised that voltage sharing between series connected devices can be more easily implemented in a multi-level inverter. In the multi-level structure each valve needs to withstand only one level of the d.c. link voltage. Therefore fewer devices need to be series connected. Also as the number of level increases, the required additional voltage at each level during abnormal operation becomes relatively small.

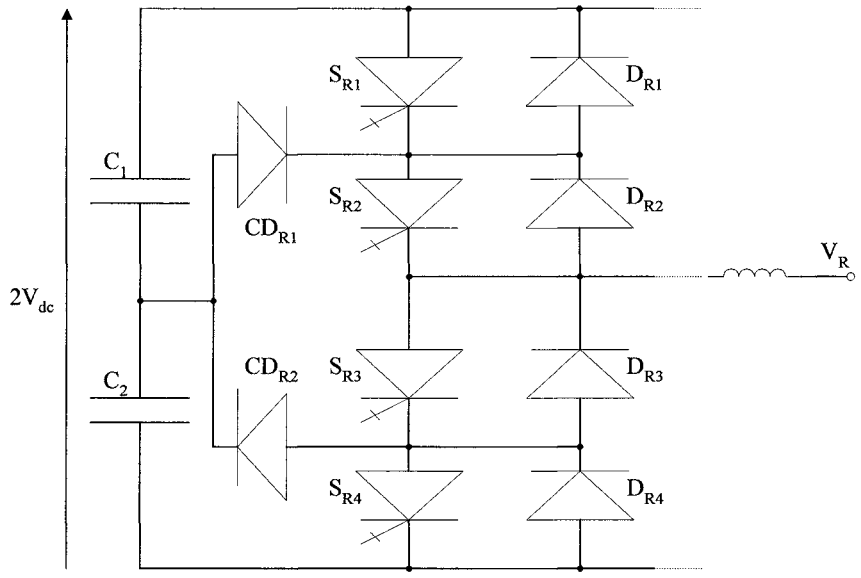


Figure 4.1 – Phase limb of conventional 3-level DCMLI

This Chapter investigates the abnormal operating conditions with regards to a power circuit device failure. Analysis is presented that investigates the robustness of the conventional diode-clamped multi-level VSI topology and the inherent redundancy of the inverter to device failure. The inherent redundancy analysis of voltage source inverter 'levels' ranging from 2 to 6 is summarised in the final section of this Chapter; with recommendations of possible redundancy operation if any is available within the inverter structure.

4.2 Representation of the 3-Level VSI in Space Vector Nodal Plane

The status of the output voltages of a conventional six-pulse (2-level) voltage source inverter (VSI) may be represented by transformation from three-phase into a two-dimensional plane. Used conventionally in the analysis of electric machine drives, the terminology of this technique has been found suitable for both the standard six-pulse bridge and also the diode-clamped multi-level topologies. By illustrating the three-phase line voltages in a two-dimensional plane, voltage space vectors can be used to represent the status of the output voltages of any level diode-clamped voltage source inverter. A 3-level DCMLI topology is presented here for illustration of the transformation into a bi-dimensional plane and then into a space-vector nodal plane.

The voltage space vectors can be represented by 'switching-state vectors' as shown for a 3-level DCMLI structure in Figure 4.2(a). Each vector, termed a 'switching-state vector', represents the inverter three-phase output line voltages in a two-dimensional plane. The inverter output line voltage can be realised at any given time by one (or more) 'switching-states' of the inverter bridge phase limbs. Therefore, a line voltage output is produced by a combination of the phase voltage switching states.

As illustrated by the switch representation diagram of the 3-level VSI structure in Figure 4.3(a), each phase output terminal of the bridge (R, Y, B) may be connected to either the positive (P), negative (N) or neutral point (0) of the d.c. link. Therefore, each switching-state vector and its resultant output line voltage is

represented in the diagram by a vector sum of the phase output voltages $V_{R0} + V_{Y0} + V_{B0}$ (assuming P or N has a 1 p.u. value). Using the space vector representation, the switching-state vector components are represented as phase voltage levels, with respect to the d.c. bus, in the form positive = 1, neutral point = 0, and negative = -1; thus the switching-state vector P0N represents R, Y, B = 1, 0, -1, respectively.

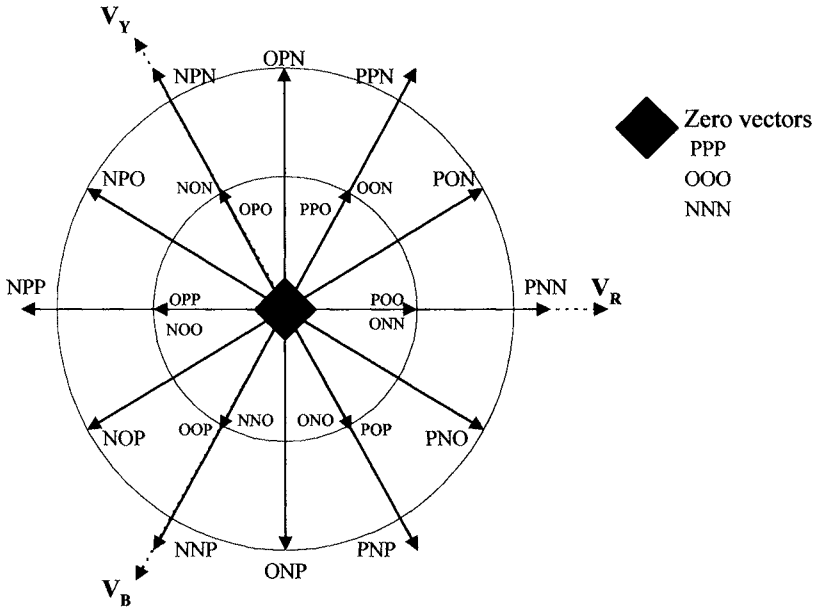
A 3-phase multi-level inverter, with N levels, has N^3 switching-state vectors, which may be selected through the applied control scheme to generate the required active voltage vectors. Therefore, for a 3-level VSI the control scheme would have a maximum of 27 available switching-state vectors. Observation of the vectors in Figure 4.2(a) shows duplication of certain switching-states per desired vector. Which implies the same line-to-line voltages on the output side. All the states, except those on the outer space circle, are duplicated. This results in the possibility of system redundancy if a switching-state is 'lost' through a fault occurrence. It can be shown that for all multi-level topologies:

Switching-state vectors = N^3, Active voltage vectors = $N^3 - (N-1)^3$

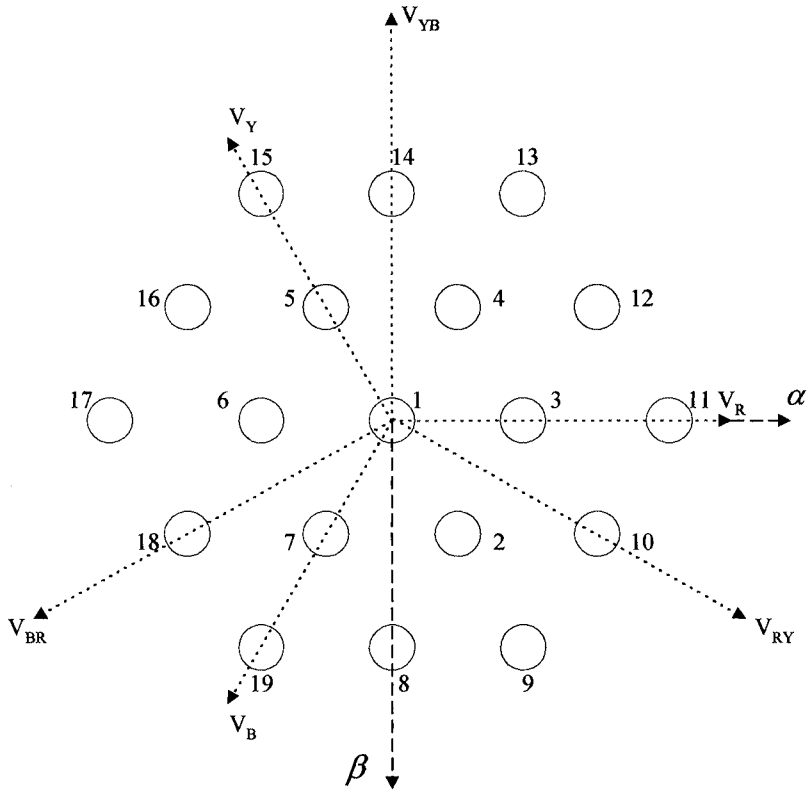
Redundant states = $(N-1)^3$, Zero voltage vectors = N

For illustration of the inverter redundancy analysis the vector representation is transformed into nodal representation, as shown in Figure 4.2(b). The obtainable output line voltages represented in Figure 4.2(a) by voltage space vectors are now shown as numbered nodes, where PNN is replaced by node 11. This minimises the complexity of the space vector representations and offers a simplistic method of illustrating 'lost' voltage vectors in the event of device faults.

To illustrate the phase voltage and line voltage outputs of individual vectors, and the coupling of the nodal plane to the voltage vector plane, a switching diagram is provided in Figure 4.3(b). Observing this possible switching sequence illustrates the connection between the output voltage level and the resultant 'lost' voltage vector, which must be averted from the space vector nodal plane for the 3-level inverter structure, in the event of a device failure.

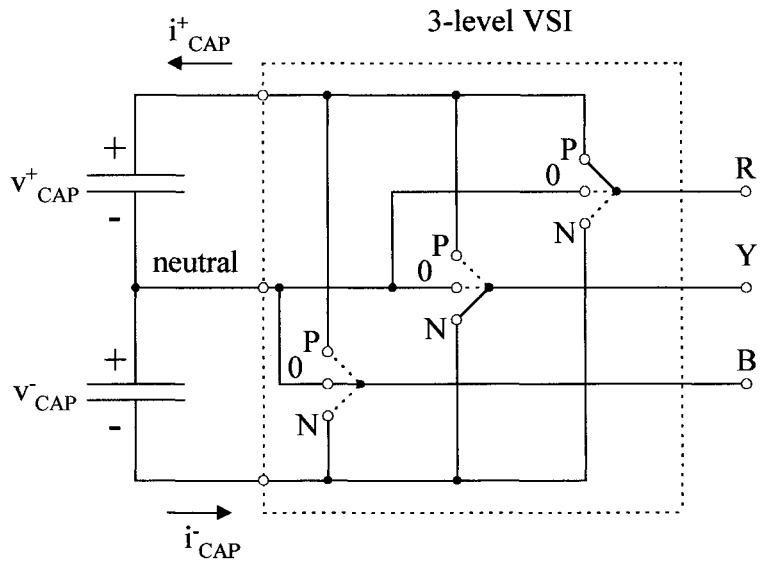


(a) – Switching state voltage vectors of the 3-level DCMLI structure

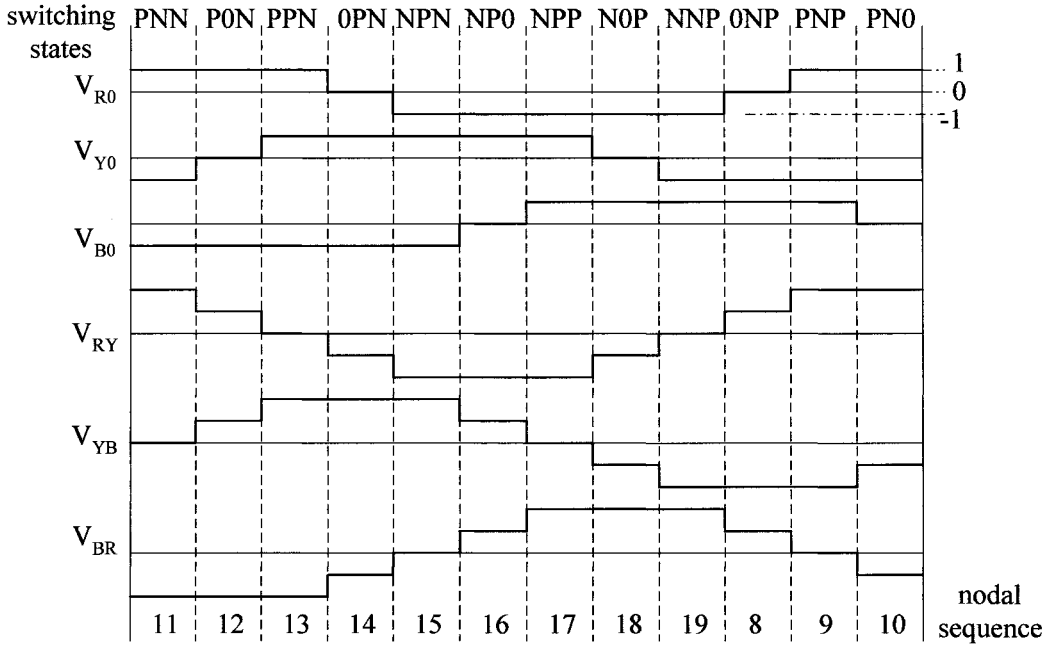


(b) – Three-level voltage vectors in space vector nodal plane

Figure 4.2 – Voltage vector and space vector nodal planes for the 3-level VSI



(a) – PON switch representation of the 3-level DCMLI structure



(b) – Switching state sequence and output voltage waveforms

Figure 4.3 – Three-level DCMLI switch representation diagram and possible switching state sequence in a three-phase voltage-source inverter

4.3 Robustness and Inherent Redundancy Investigation

The continual performance of the DCMLI topology in the event of short-circuit or open-circuit device faults is investigated. Hence, the inherent redundancy and operational robustness of the DCMLI topology is investigated for various levels. Analysis is carried out on a single limb of the inverter using the space vector nodal technique. The notation (1XX) for the switching-state is applied for the analysis of the inverter structures where 1 indicates a positive output voltage level from the first phase (R) and 'X' identifies indifference to the states of the remaining phases (Y and B).

It will be shown that the impact of a single device failure on the continual operation of the inverter is dependent upon the location of the failed device in the phase limb and on the number of levels of the multi-level inverter. This indicates the occurrence of different levels of inherent redundancy with respect to different device failures of the same inverter type. Normally, when a semiconductor device fails it becomes short-circuit rather than open-circuit. Thus, a short-circuit device failure is the most common fault event in a multi-level topology. It will be presented that when a switching device fails short-circuit, the d.c. bus voltage will be shorted if the normal control switching modulation scheme is continued under fault conditions. Therefore, in order to continue operation in the event of a fault, certain switching-states will be sacrificed or 'lost' as the switching sequence must be altered to avert the short-circuit path. For device open-circuit fault analysis, depending upon the polarity of the load current, switching states are lost with respect to diode biasing and positioning of the switching device within the inverter phase leg. However, this form of analysis is only suitable if the apparent fault is not due to an actual device failure. Such a situation could occur if a switching device driver signal is delayed for a period of time and the controller rectifies the problem before the current direction changes. Therefore, as the work presented in this thesis is investigating a complete device failure where the device is permanently short-circuit or open-circuit the diode biasing analysis, as performed in [47] is not suitable.

4.4 TWO-LEVEL VSI INVESTIGATIONS

Although the inherent redundancy investigations are particularly focussed upon the diode-clamped multi-level inverter topology the conventional six-pulse (or 2-level) topology is analysed and presented first. This is simply for completeness and comparison of the investigation as the 2-level topology, used as a building block for the multi-pulse configurations, is still presently the most utilised structure in high power industrial applications. Using the same three-two transformations applied to the 3-level topology in section 4.2 the attainable output line voltages of a 2-level inverter can be realised through switching-state voltage vectors. Representing the voltage vectors, for the 2-level inverter topology, in a space-vector nodal plane results in the bi-dimensional switching-state nodal plane given in Figure 4.4. The switching-states available from each phase of the 2-level topology are positive (1XX) and negative (-1XX). Utilising this representation the inherent redundancy of the 2-level structure in response to a device fault is analysed, as presented in the following sections.

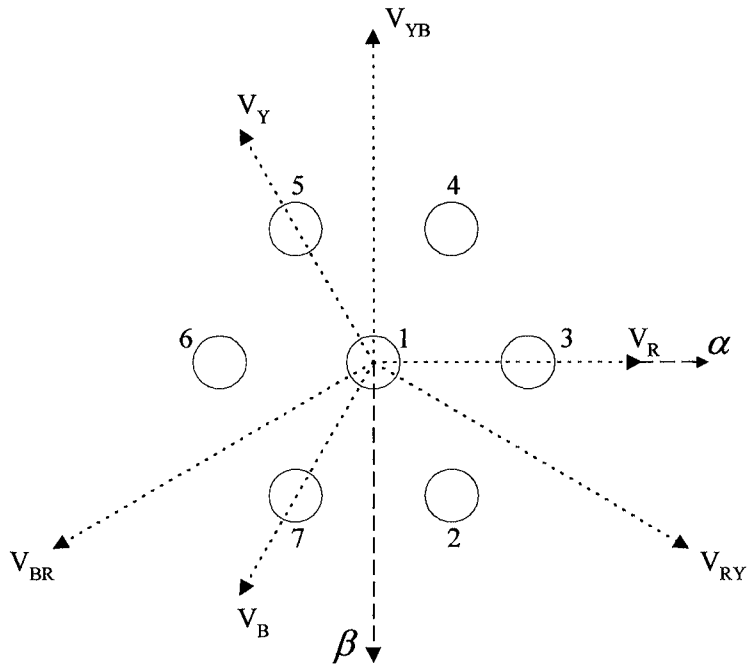


Figure 4.4 – Two-level VSI represented in the space-vector nodal plane

4.4.1 SHORT-CIRCUIT DEVICE FAULTS

The short-circuit fault of a main switching device is examined in the red (R) phase of the inverter structure. Figure 4.5 illustrates a short-circuit fault to device S_{R1}. As shown, if S_{R4} is activated through the controller this will provide a capacitor discharge path. To prevent this, switching states of the form (-1XX) must be avoided. This results in 4 switching states out of a possible 7 being 'lost'. The distribution of the unobtainable states, across the negative α axis in the nodal plane, is given in Figure 4.6. The red nodes represent voltage vectors completely lost (nodes 5-7) and the cyan nodes illustrate voltage vectors that have lost switching states but can still be realised through system redundancy (node 1).

The effect of a short-circuit failure to device S_{R4} is comparable to its complementary positioned device in the upper half of the phase leg, as illustrated in Figure 4.7. The distribution of 'lost' states, in the event of S_{R4} failing short, is across the positive α-axis as states (1XX) would be unobtainable due to the prevention of a capacitor discharge path. This is shown in Figure 4.8. As with the upper device, 3 vectors are completely 'lost' (nodes 2-4) and 1 vector has 'lost' switching states but can still be realised through system redundancy (node 1). The results of this device short-circuit fault analysis are given in Table 4.1.

Device	Number of states lost	Number of active vectors lost	Lost states of form
S_{R1}	4	3	(-1XX)
S_{R4}	4	3	(1XX)

Table 4.1 - States lost due to short-circuit device faults in the 2-level topology

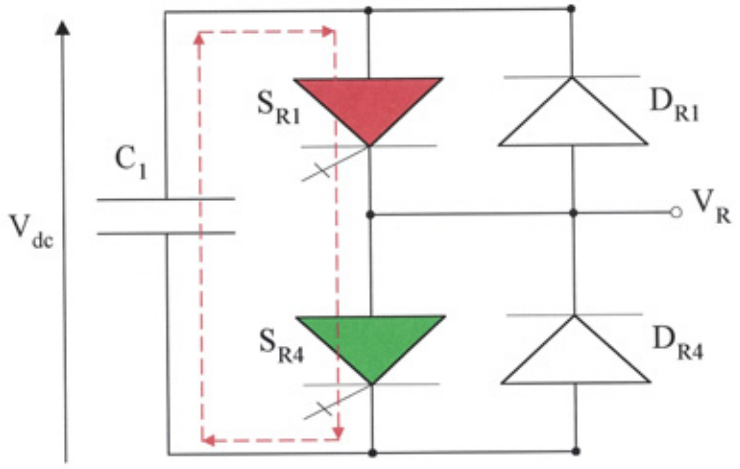


Figure 4.5 – Capacitor Discharge Path - S_{R1} short-circuit: S_{R4} activated

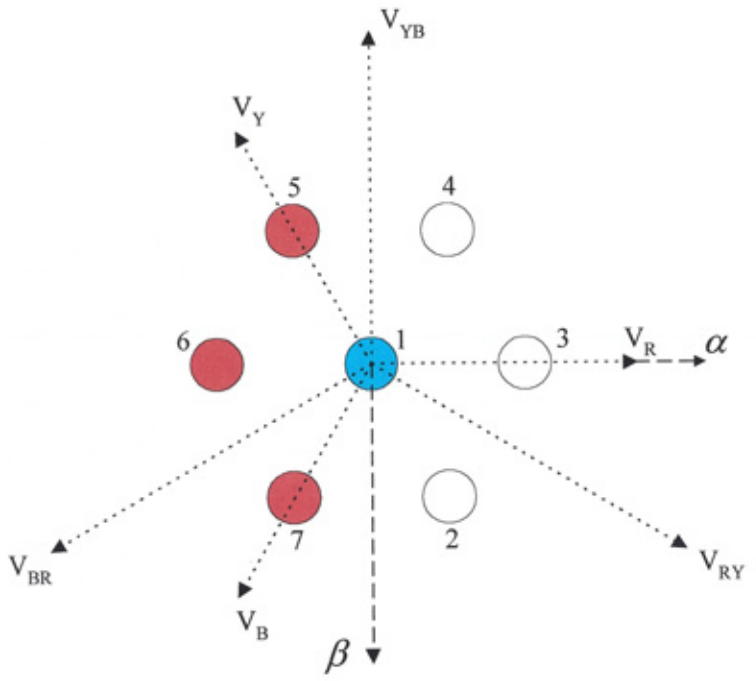


Figure 4.6 – Distribution of 'lost' switching-states due to a S_{R1} short-circuit

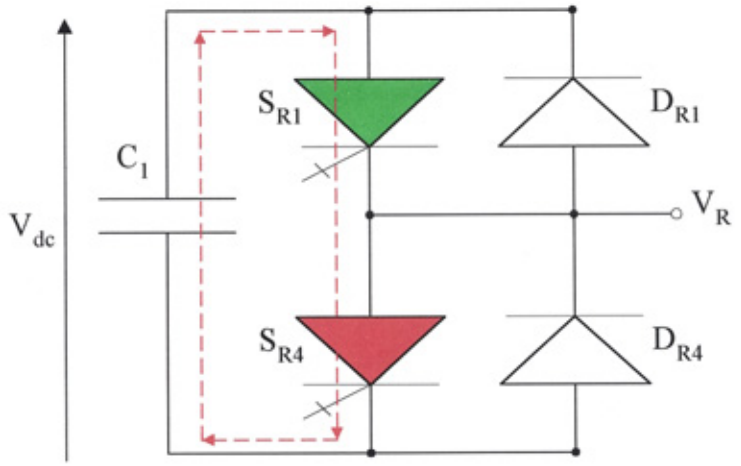


Figure 4.7 – Capacitor Discharge Path - S_{R4} short-circuit: S_{R1} activated

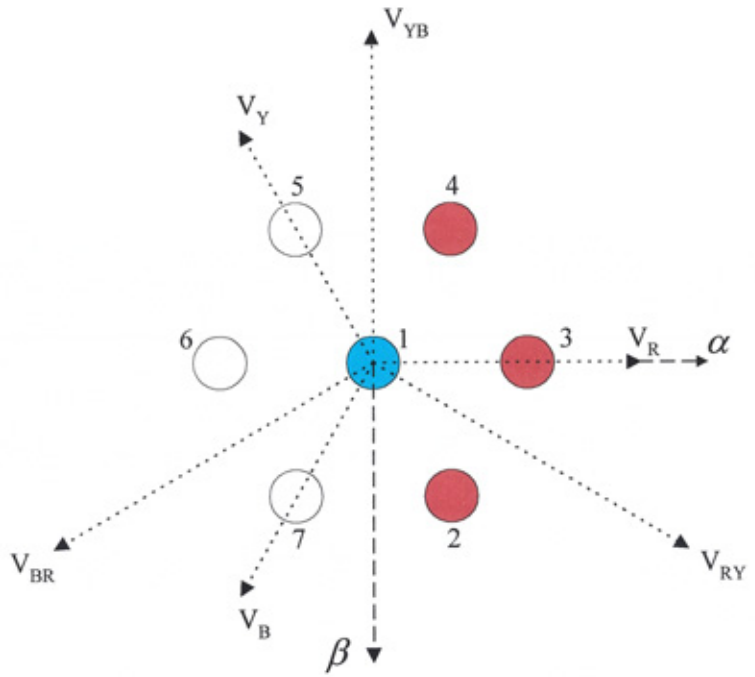


Figure 4.8 – Distribution of 'lost' switching-states due to a S_{R4} short-circuit

4.4.2 Open-Circuit Device Faults

The 2-level topology is then investigated with respect to open-circuit device faults. Open-circuit switching device failure investigations show equivalent results for an upper phase leg device failing open-circuit and the short-circuit failure of its complementary device in the lower phase leg. The distribution of 'lost' states for S_{R1} failing open-circuit is, as expected, across the positive α axis as illustrated in Figure 4.9. This is due to switching-states (1XX) being 'lost' from the modulation scheme as any voltage level that requires the device S_{R1} will now be unobtainable.

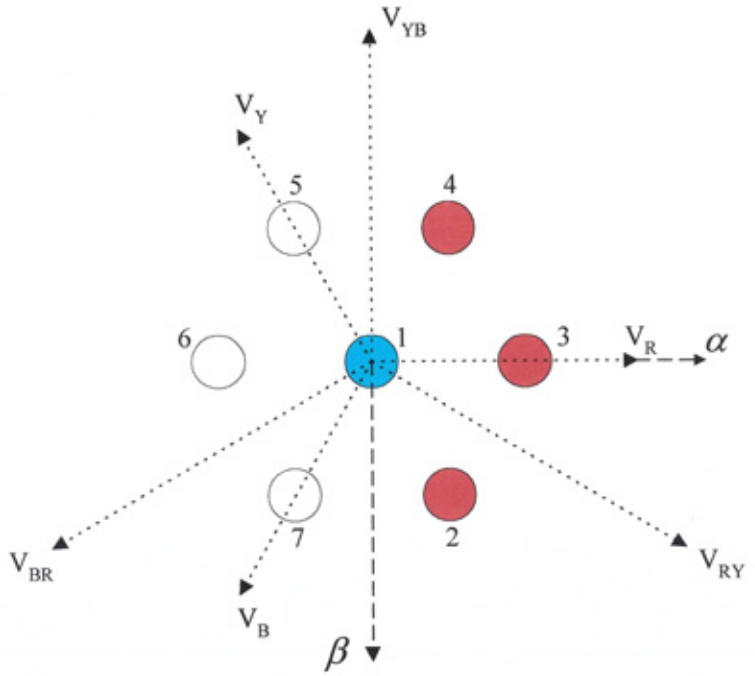


Figure 4.9 – Distribution of 'lost' switching-states due to a S_{R1} open-circuit

Figure 4.10 illustrates the 'lost' switching-states in the event of device S_{R4} failing open-circuit. Again any voltage levels requiring the activation of S_{R4} will be 'lost' from the modulation scheme and therefore switching-states (-1XX) are unobtainable. The complete results of the 2-level open-circuit device investigations are presented in Table 4.2.

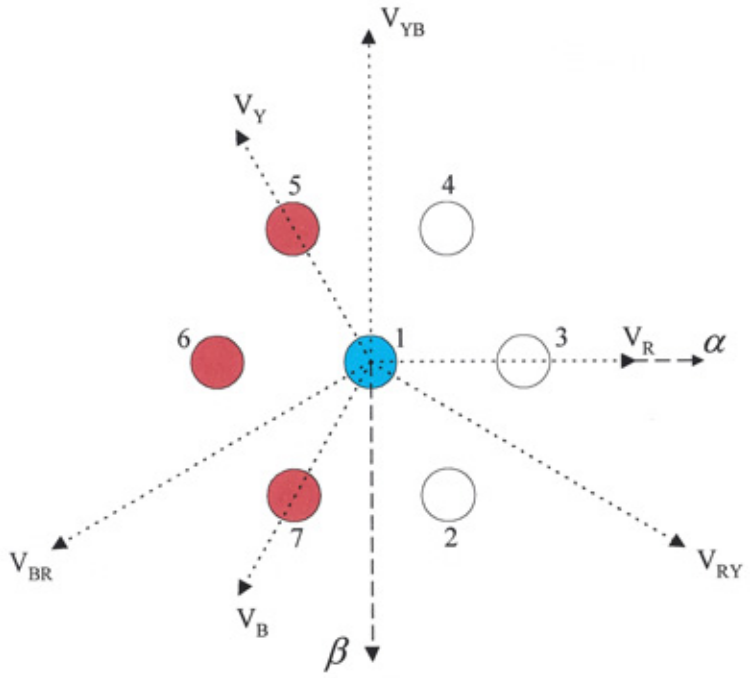


Figure 4.10 – Distribution of 'lost' switching-states due to a S_{R4} open-circuit

Device	Number of states lost	Number of active vectors lost	Lost states of form
S_{R1}	4	3	(1XX)
S_{R4}	4	3	(-1XX)

Table 4.2 - States lost due to open-circuit device faults in the 2-level topology

4.5 THREE-LEVEL VSI INVESTIGATIONS

It can be predicted from the previous analysis for a 2-level inverter that a switching device short-circuit failure would result in the possibility of a capacitor discharge path, if the normal switching scheme were continued under fault conditions. The multi-level structure differs in the fact that there are more available voltage levels, attainable through switching-states of the phase limbs. For the phase output voltage in the 3-level topology, there are three switching-states, positive (1XX), negative (-1XX) and neutral (0XX) as compared to the limited two switching-states, (1XX) and (-1XX), of the 2-level inverter. This is illustrated in the 3-level fundamental frequency output phase voltage shown in Figure 4.11. A standard fundamental frequency modulation control strategy for the three-level DCMLI structure is also presented in Table 4.3.

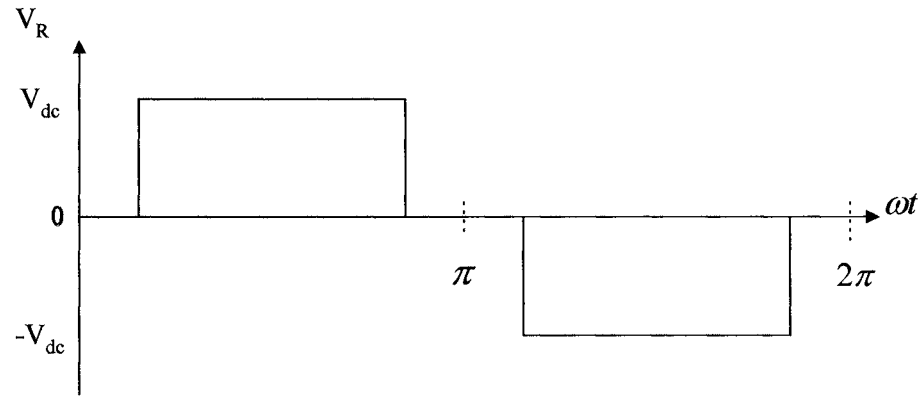


Figure 4.11 – Three-level output phase voltage

Voltage levels are produced through the use of more phase limb switching devices and also auxiliary clamp diodes used for the 'zero', neutral or clamping path to the d.c. link. Therefore, as well as investigating the main d.c. rail devices, as with the 2-level topology, the 3-level topology investigations also require analysis of the additional switching devices and clamp diodes.

Switching State (1 = on, 0 = off)				Output Voltage Level
S_{R1}	S_{R2}	S_{R3}	S_{R4}	V_{RN}
1	1	0	0	+Vdc
0	1	1	0	0
0	0	1	1	-Vdc

Table 4.3 – Standard switching scheme for the three-level VSI

4.5.1 SHORT-CIRCUIT DEVICE FAULTS

Short-circuit failure of switching devices and clamp-diodes are considered in the red (R) phase of the 3-level inverter structure. If device S_{R1} fails short-circuit, as illustrated in Figure 4.12, when the controller sequentially activates $S_{R2} \rightarrow S_{R3}$ a discharge path occurs for capacitor C_1. Therefore to prevent this, the controller must evade the switching-state (0XX).

Observation of the nodal plane (Figure 4.13) shows that lost states are concentrated in the inner nodal hexagon, where there exist redundant switching states. Therefore, although short-circuit faults to device S_{R1} result in 9 unobtainable (zero clamp) switching-states, only 2 voltage vectors are completely lost. The nodal plane illustrates how full voltage vectors 8 and 14 are lost whereas intermediate voltage vectors 1-7 are still obtainable through inherent system redundancy. The inverter can therefore keep operating with the phase voltage level reduced from three to two.

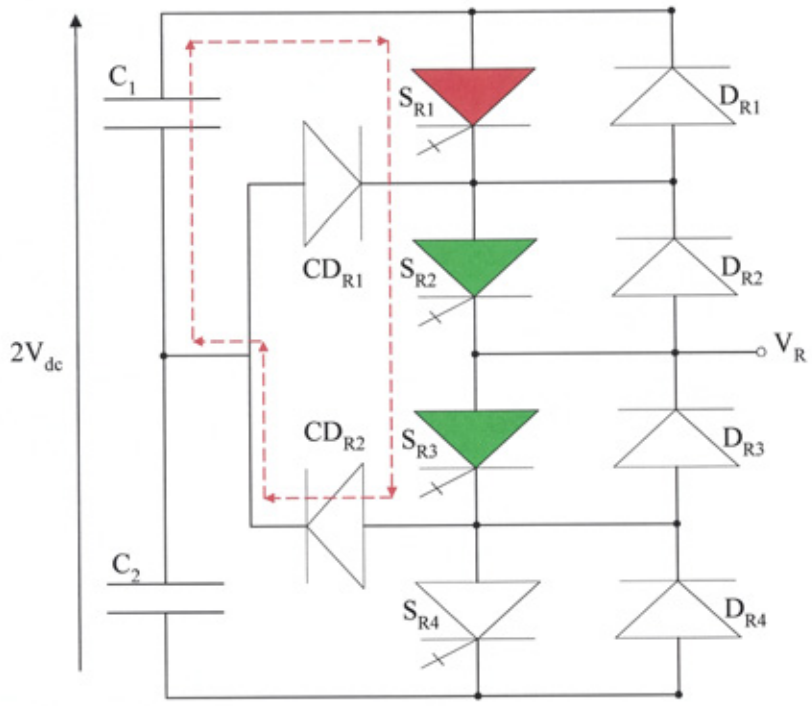


Figure 4.12 – Capacitor Discharge Path
- S_{R1} short-circuit: S_{R2} and S_{R3} activated

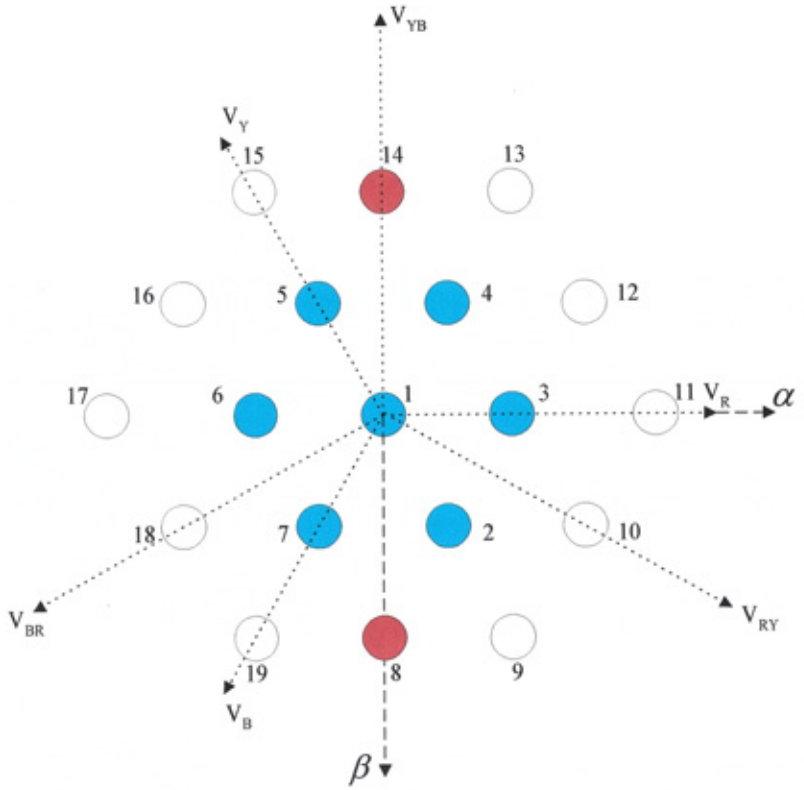


Figure 4.13 – Distribution of 'lost' switching-states due to either S_{R1} or S_{R4} short-circuit

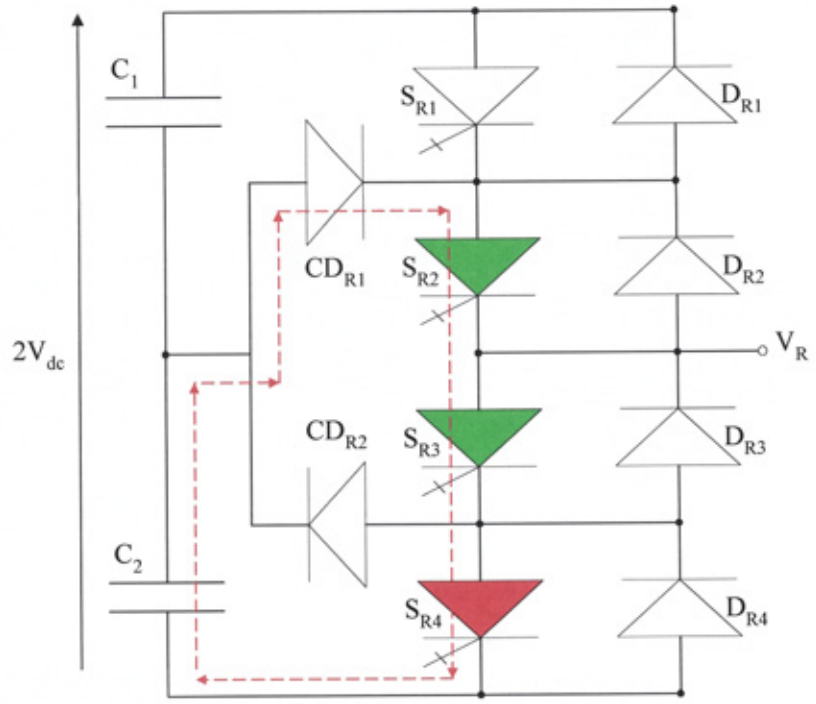


Figure 4.14 – Capacitor Discharge Path
- S_{R4} short-circuit: S_{R2} and S_{R3} activated

Similarly, for a short-circuit fault to device S_{R4} a capacitor discharge path is presented to C_2 if the controller activates $S_{R2} \rightarrow S_{R3}$, as shown in Figure 4.14. Resulting in the loss of zero clamp states (0XX) for the red phase. As with S_{R1} failing short-circuit, the distribution of the 'lost' switching states due to the aforementioned device faults is given in Figure 4.13.

The short-circuit failure of a central switching device (S_{R2} or S_{R3}) and an auxiliary clamp diode (CD_{R1} or CD_{R2}) have a more detrimental effect on the continual performance of the inverter. When S_{R2} or CD_{R2} fails short, a discharge path for capacitor C_2 results if devices $S_{R3} \rightarrow S_{R4}$ are activated by the control scheme, as shown in Figures 4.15 and 4.16. Therefore, the controller must sacrifice the switching-state (-1XX) to prevent the capacitor discharge.

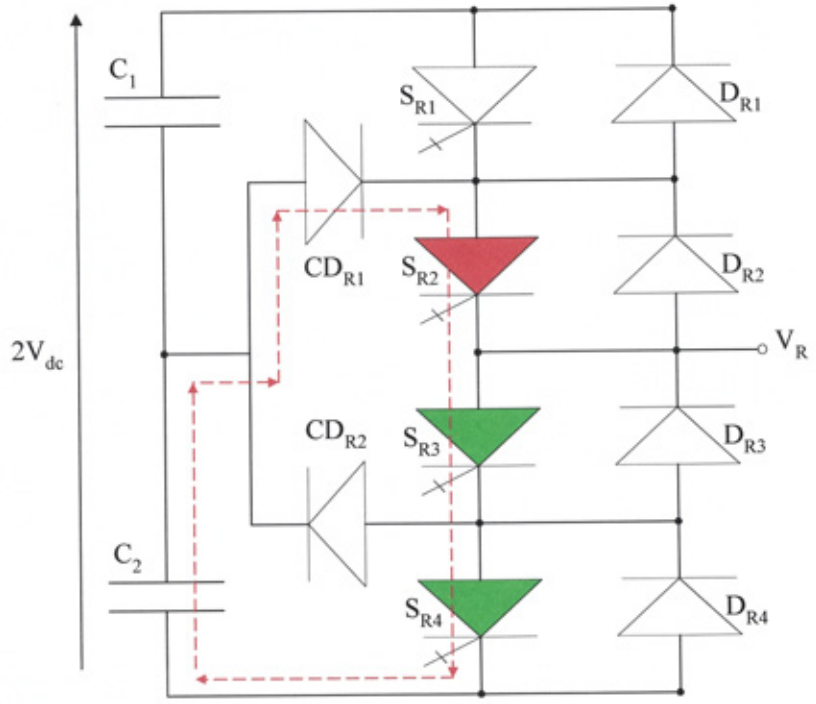


Figure 4.15 – Capacitor Discharge Path

- S_{R2} short-circuit: S_{R3} and S_{R4} activated

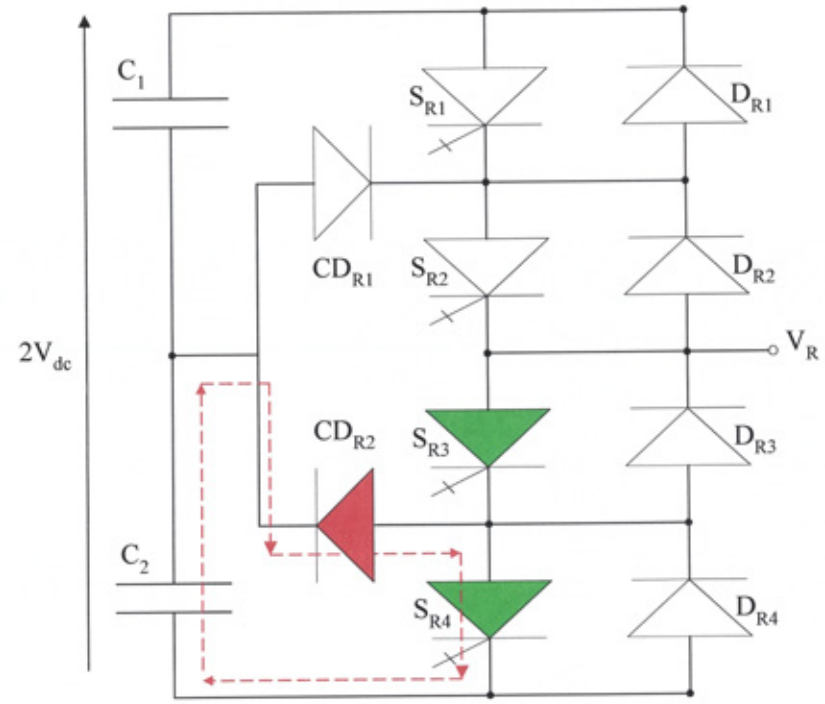


Figure 4.16 – Capacitor Discharge Path

- CD_{R2} short-circuit: S_{R3} and S_{R4} activated

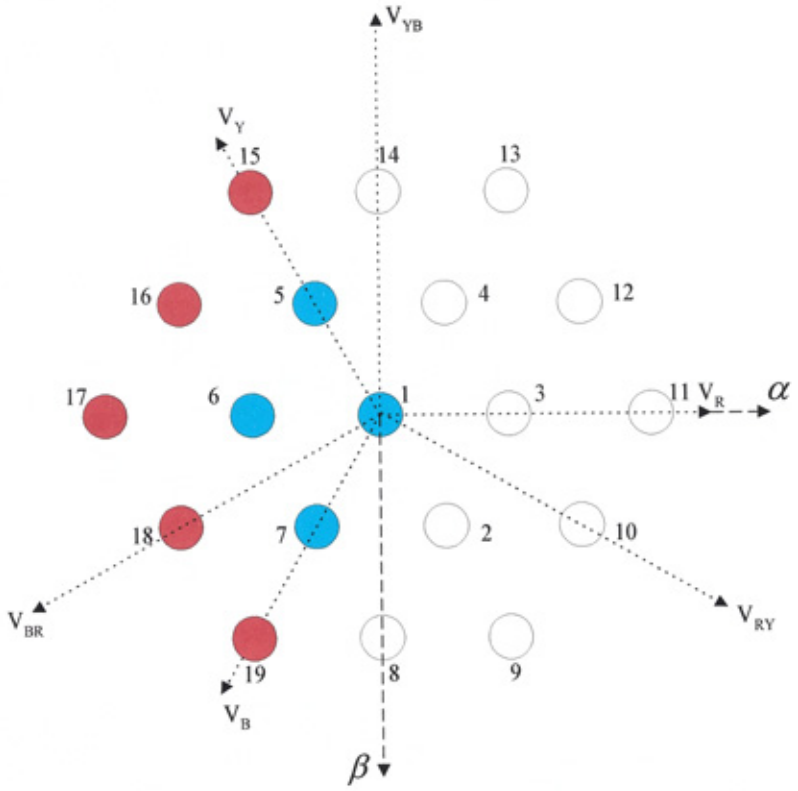


Figure 4.17 – Distribution of 'lost' switching-states due to either S_{R2} or CD_{R2} short-circuit

In the event of these faults, the distribution of unobtainable switching states across the nodal plane (Figure 4.17) shows that of the 9 unobtainable states, 5 result in completely lost full voltage vectors. As the outer nodal hexagon (representing full voltage vectors) offers no switching-state redundancy, the inverter would be inoperable. Similarly, for a short-circuit fault to device S_{R3} or CD_{R1} a capacitor discharge path is presented to C_1 if the controller activates $S_{R1} \rightarrow S_{R2}$, as shown in Figures 4.18 and 4.19. Resulting in the loss of switching states (1XX) from the controller for the Red phase. The distribution of the 'lost' switching states due to these device faults is given in Figure 4.20.

Observation of the nodal plane shows that the distribution of states is the mirror image across the β axis of the 'lost' states due to S_{R2} or CD_{R2} failing short. Therefore, as 5 voltage vectors out of 9 are completely unobtainable, the nodal plane again illustrates inoperability of the inverter and its limited inherent robustness for continual operation.

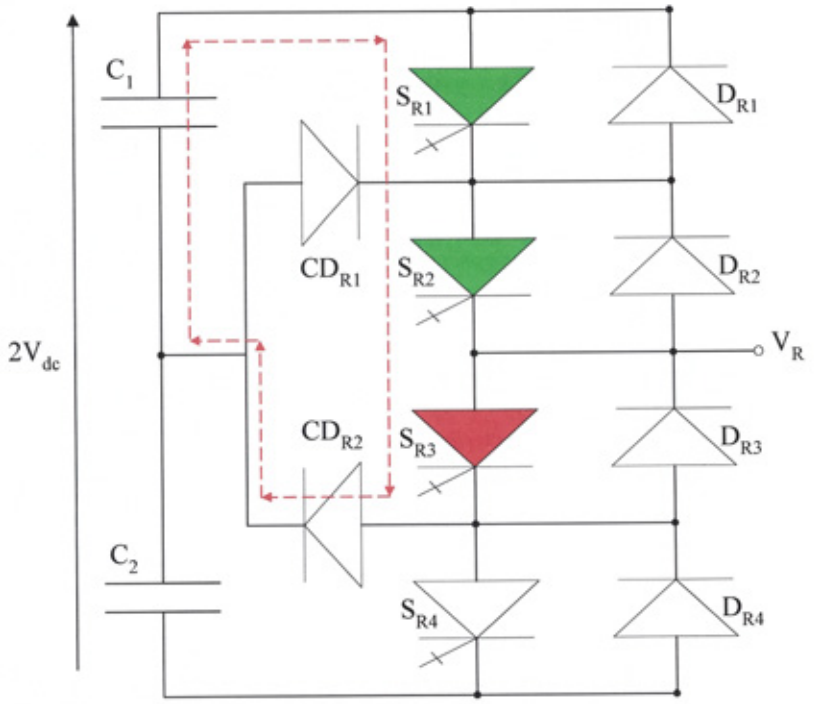


Figure 4.18 – Capacitor Discharge Path

- S_{R3} short-circuit: S_{R1} and S_{R2} activated

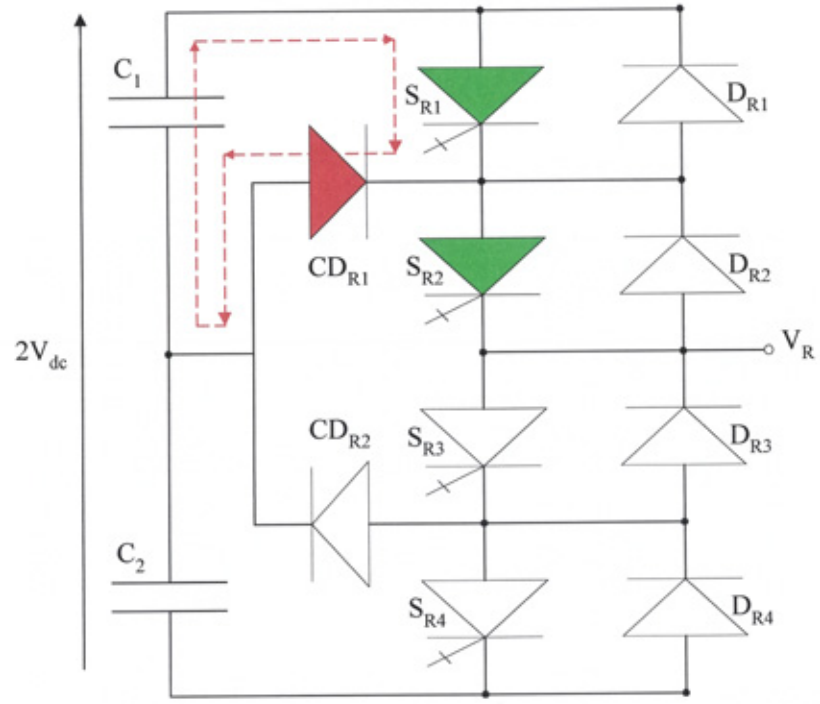


Figure 4.19 – Capacitor Discharge Path

- CD_{R1} short-circuit: S_{R1} and S_{R2} activated

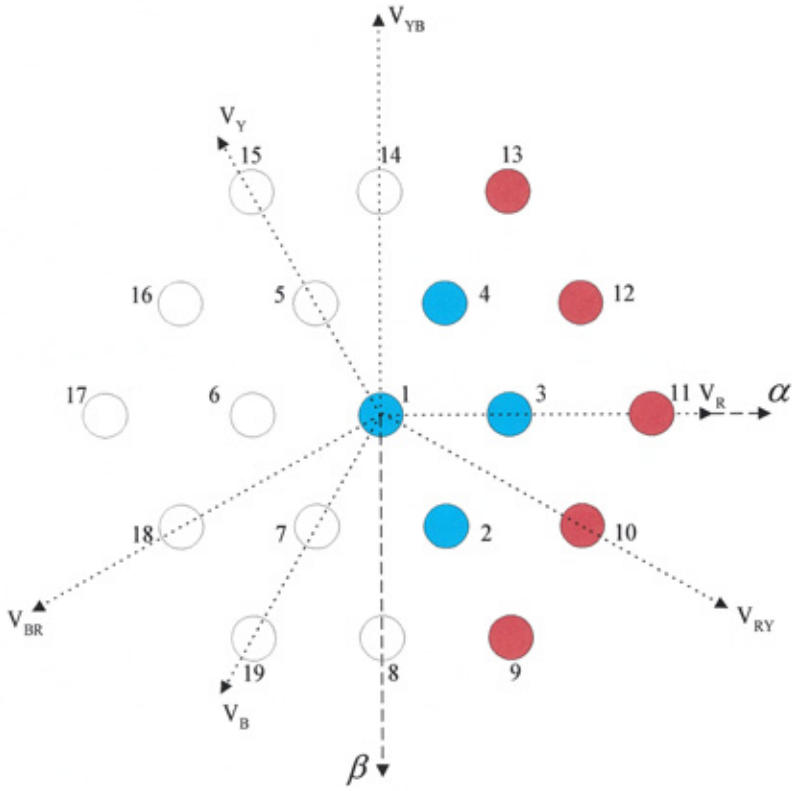


Figure 4.20 – Distribution of 'lost' switching-states due to either S_{R3} or CD_{R1} short-circuit

The results of the short-circuit device faults for the 3-level inverter are summarized in Table 4.4. Observation of Table 4.4, and the distribution of the 'lost' states across the nodal planes, shows that the 3-level inverter offers some inherent operational redundancy and adaptability, albeit extremely restricted

Device	Number of states lost	Number of active vectors lost	Lost states of form
S_{R1} or S_{R4}	9	2	(0XX)
S_{R2} or CD_{R2}	9	5	(-1XX)
S_{R3} or CD_{R1}	9	5	(1XX)

Table 4.4 - States lost due to short-circuit devices

4.5.2 OPEN-CIRCUIT DEVICE FAULTS

The fact that there is less probability of an open-circuit device failure is beneficial for the inherent robustness and continual operation of the voltage source inverter, as was illustrated partially with the 2-level investigation given in section 4.4. In the investigation of the 3-level inverter structure, the severity of an open-circuit failure, due to a device fault or malfunction of the drive circuit, is illustrated with the number of switching-states and resultant active vectors 'lost'. The results of the open-circuit fault analysis are given in Table 4.5.

Device	**Number of states lost**	**Number of active vectors lost**	**Lost states of form**
S_{R1}	9	5	(1XX)
S_{R2}	18	10	(1XX), (0XX)
S_{R3}	18	10	(0XX), (-1XX)
S_{R4}	9	5	(-1XX)
CD_{R1} or CD_{R2}	9	2	(0XX)

Table 4.5 - States lost due to open circuit device failures

Observation of these results illustrates the severity of failure of the central switching devices, which is a common observation across all the multi-level structures. Obviously all states requiring the operation of devices in conjunction with the faulty device will be unobtainable. For example, an open-circuit failure restricting the operation of device S_{R2} results in the distribution of 'lost' states shown in Figure 4.21. Of the 18 switching states unobtainable through the control scheme 14 of them result in the loss of 10 voltage vectors out of a possible 19. Nodes 1, 5, 6 and 7 have each lost two switching states accounting for the 4 that appear missing. An open-circuit failure of S_{R3} results in an identical restriction of voltage vectors for continual operation as with the S_{R2} open-circuit case, with the distribution of 'lost' states being a mirror image across the β axis as shown in Figure 4.22.

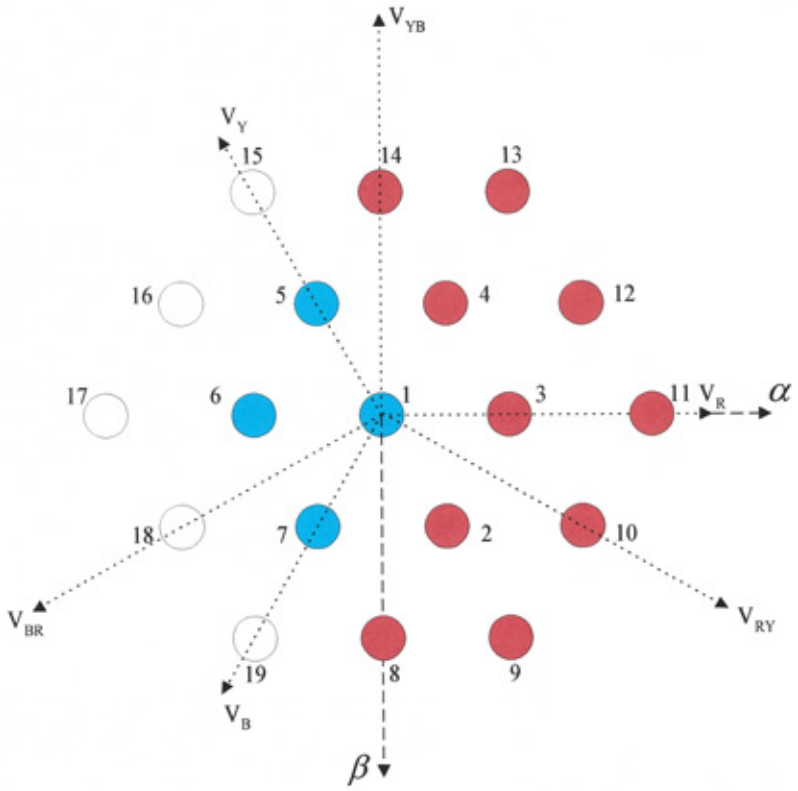


Figure 4.21 – Distribution of 'lost' switching-states due to a S_{R2} open-circuit

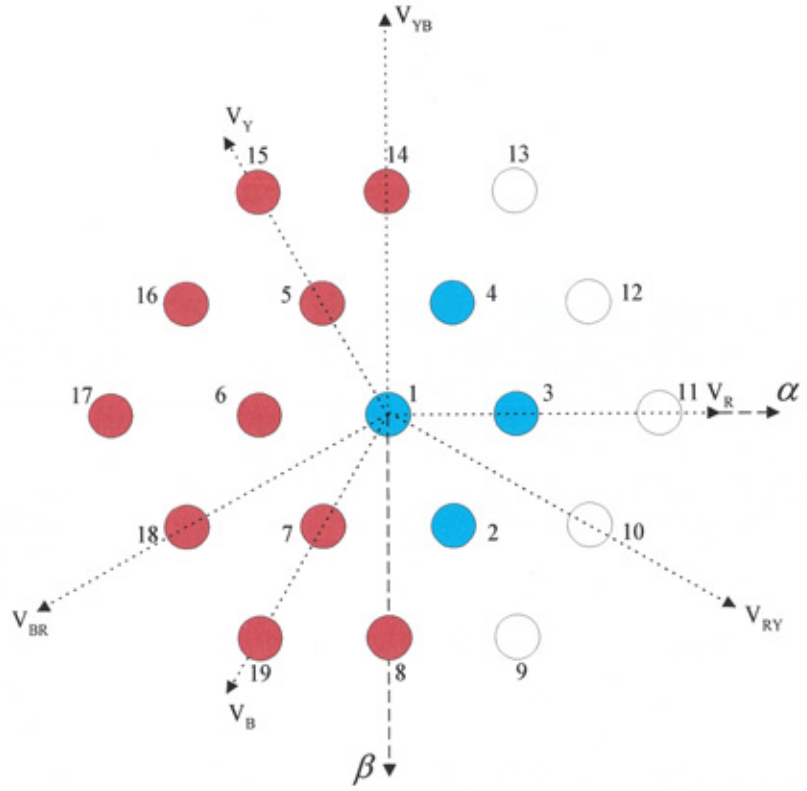


Figure 4.22 – Distribution of 'lost' switching-states due to a S_{R3} open-circuit

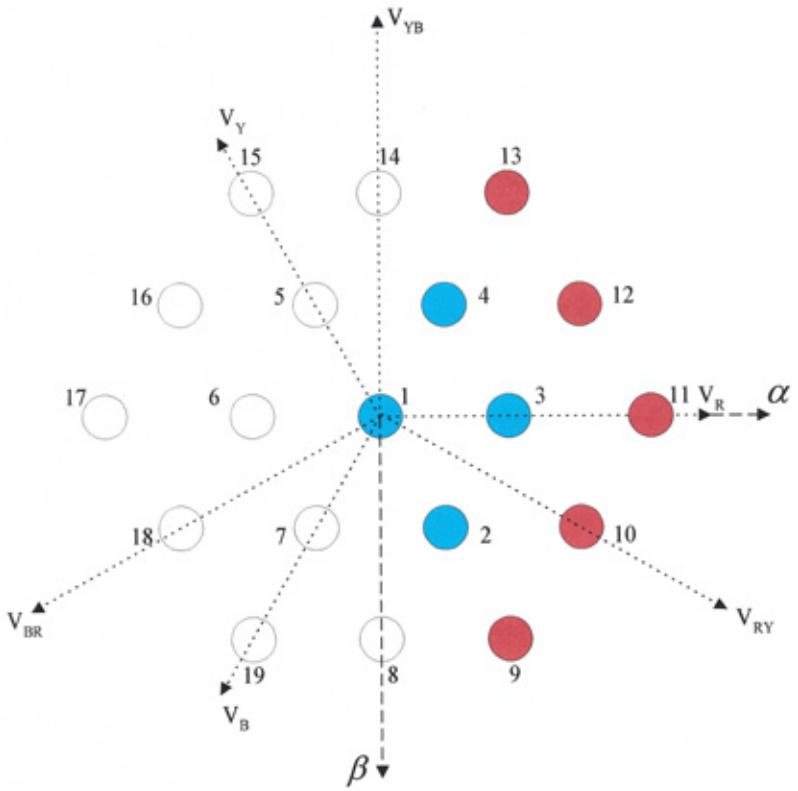


Figure 4.23 – Distribution of 'lost' switching-states due to a S_{R1} open-circuit

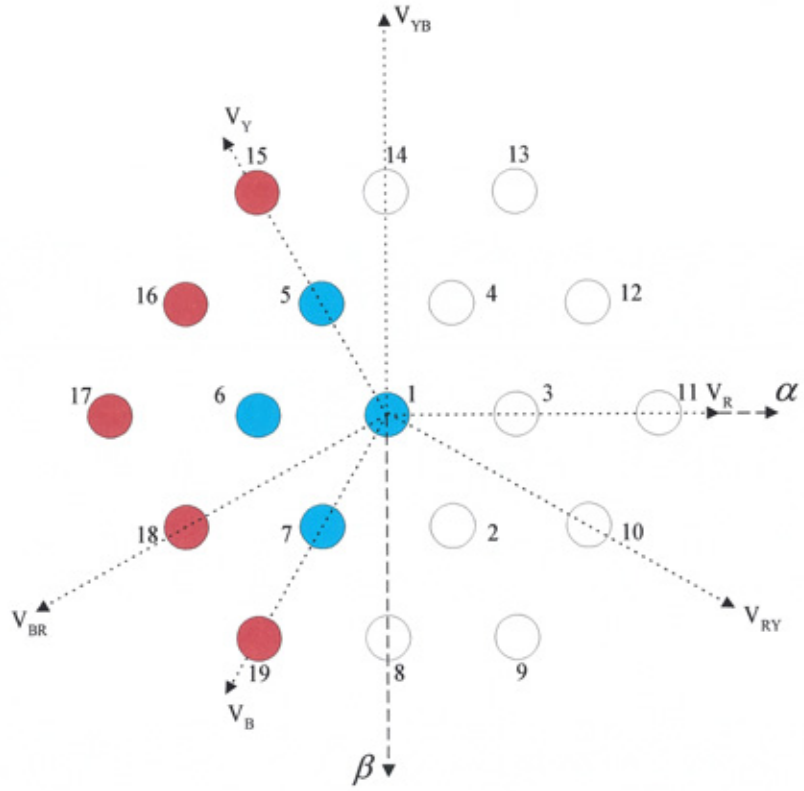


Figure 4.24 – Distribution of 'lost' switching-states due to a S_{R4} open-circuit

Open-circuit failure of devices S_{R1} and S_{R4}, although appearing less destructive with respect to the number of lost vectors, still results in an inoperable system as the full voltage vectors (1XX) and (-1XX) will be lost respective of the faulty device. The distribution of 'lost' states, illustrated in Figures 4.23 and 4.24, are therefore identical to the short circuit failures of devices S_{R3} and S_{R2} respectively.

Analysis of the open circuit failure of an auxiliary clamp diode shows more promising results with regard to continual operation. Observation of Table 4.5 and the distribution of unobtainable states given in Figure 4.25 show that, as with the short-circuit failure of devices S_{R1} and S_{R4}, the zero clamp state (0XX) is lost. Exemplifying that in the event of these types of faults the inverter could be operated as a 2-level inverter utilising states (1XX) and (-1XX).

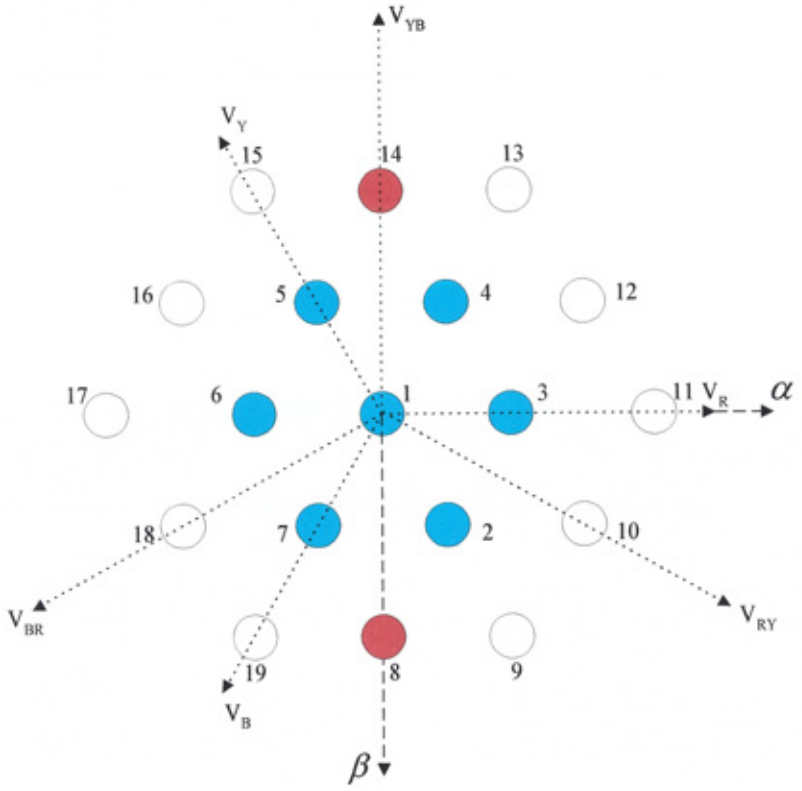


Figure 4.25 – Distribution of 'lost' switching-states due to either CD_{R1} or CD_{R2} open-circuit

4.6 SIX-LEVEL VSI INVESTIGATIONS

As presented in Chapter 3, the diode-clamped multi-level inverter topology can be structured in both odd and even forms. The even-level topology offers similar operational characteristics and advantages to their odd-level counterparts, differing only due to the removal of the zero voltage level resultant from the zero switching- state (0XX).

The 6-level DCMLI structure, proposed as the optimal 'level' of the available DCMLI topologies [32], is presented in this section to illustrate the increased inherent redundancy as the multi-level number 'N' increases. The 6-level inverter output phase voltage exhibits six voltage levels as illustrated in Figure 4.26. The phase switching states that must be realisable through the controller for full operation of the inverter are therefore (3XX), (2XX), (1XX), (-1XX), (-2XX) and (-3XX). Figure 4.27 shows one phase limb of the 6-level DCMLI structure. The standard fundamental frequency-switching scheme for the 6-level VSI topology is given in Table 4.6.

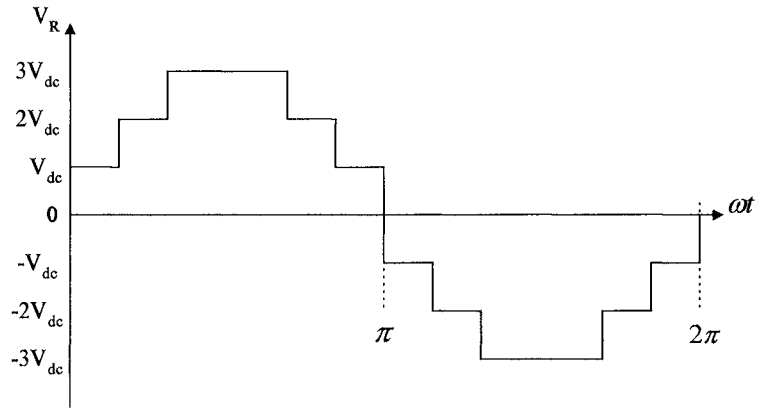


Figure 4.26 – Six-level output phase voltage

In the previous sections, the routes of the capacitor discharge paths have been fully illustrated for the 2-level and the 3-level DCMLI topologies. Therefore, they will not be repeated in the following analysis. Only the distribution of the 'lost'

switching-states due to a device fault is presented. The 6-level DCMLI topology represented in the space-vector nodal plane is given in Figure 4.28.

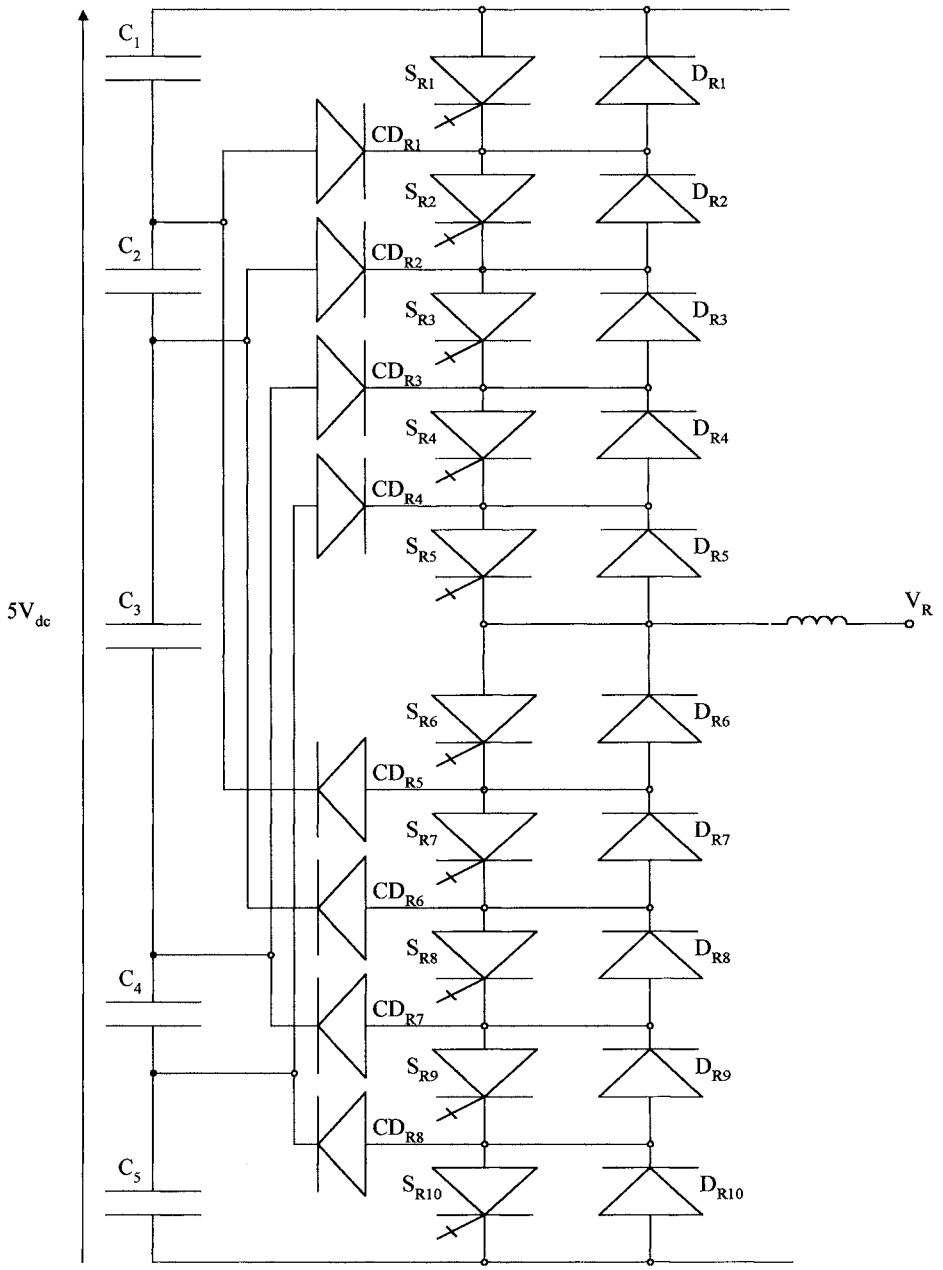


Figure 4.27 – Phase limb of a six-level DCMLI structure

Switching State (1 = on, 0 = off)										Output Voltage Level
S_{R1}	S_{R2}	S_{R3}	S_{R4}	S_{R5}	S_{R6}	S_{R7}	S_{R8}	S_{R9}	S_{R10}	V_{RN}
1	1	1	1	1	0	0	0	0	0	$+3\ V_{dc}$
0	1	1	1	1	1	0	0	0	0	$+2\ V_{dc}$
0	0	1	1	1	1	1	0	0	0	$+\ V_{dc}$
0	0	0	1	1	1	1	1	0	0	$-\ V_{dc}$
0	0	0	0	1	1	1	1	1	0	$-2\ V_{dc}$
0	0	0	0	0	1	1	1	1	1	$-3\ V_{dc}$

Table 4.6 – Standard switching scheme for 6-level DCMLI

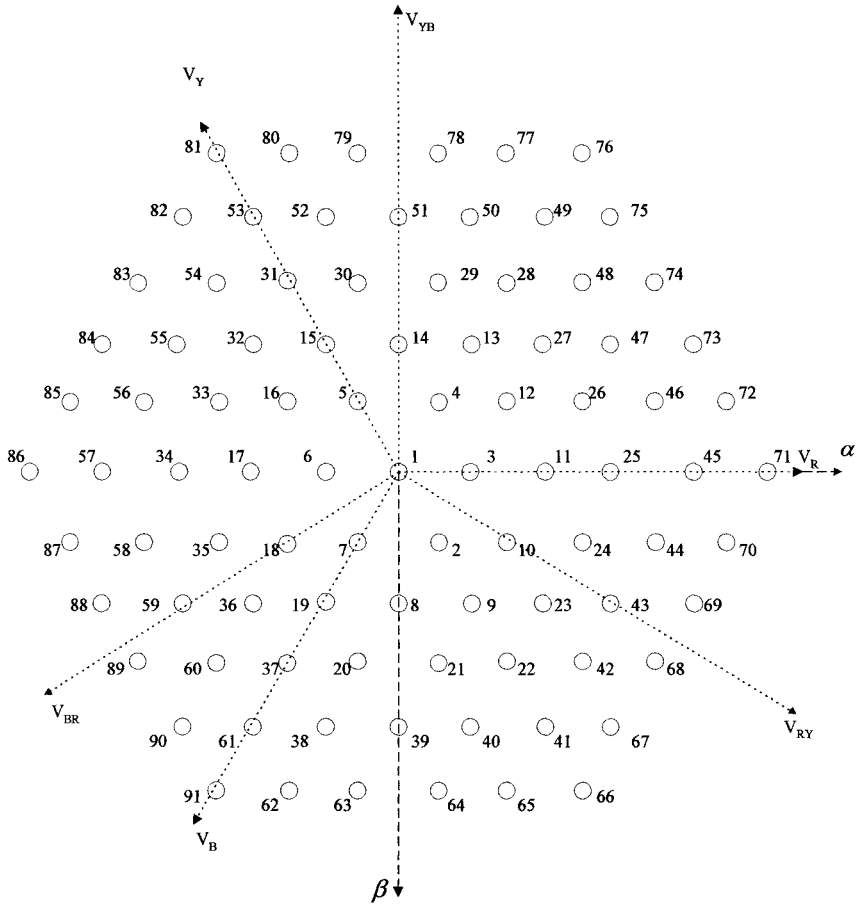


Figure 4.28 – Six-level DCMLI represented in the space-vector nodal plane

4.6.1 SHORT-CIRCUIT DEVICE FAULTS

The redundancy analysis of the 3-level structure has indicated that the most critical devices to the continual performance of the inverter under short-circuit fault conditions are the central switching devices. Also, short-circuit failure of the d.c. rail devices leaves some operational redundancy. Therefore, the 6-level analysis will begin with a comparison of short-circuit faults to the d.c. rail and central switching devices. As with the 3-level structure, short-circuit failure of switching devices and auxiliary clamp-diodes are considered in the red (R) phase of the inverter structure.

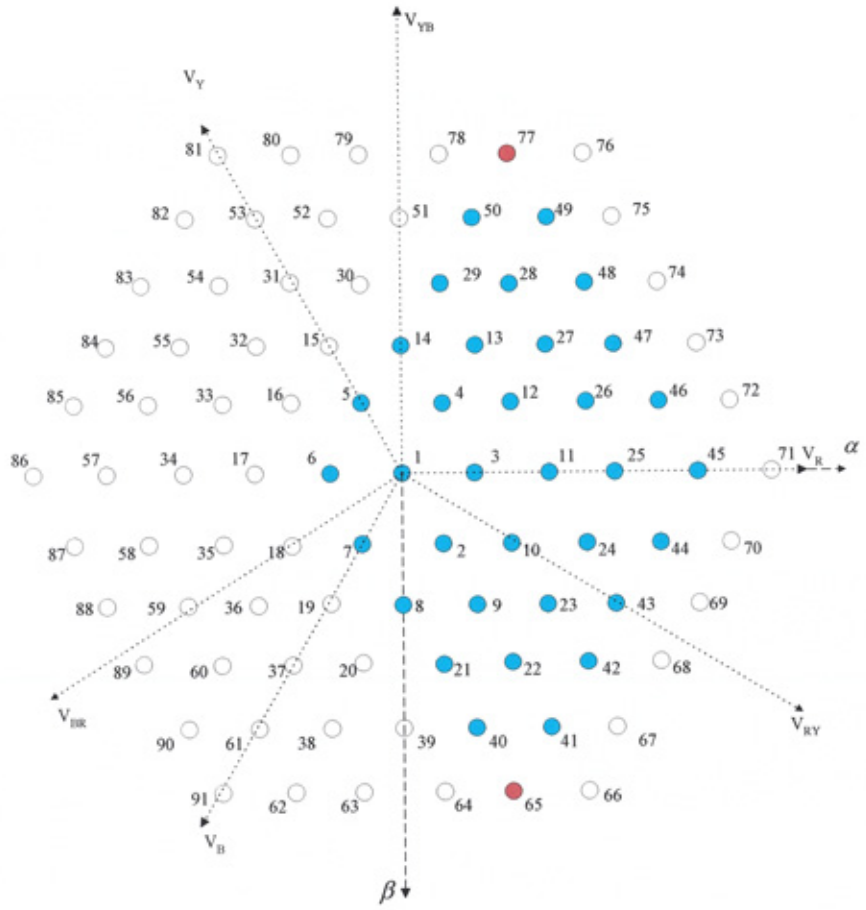


Figure 4.29 – Distribution of 'lost' states due to either S_{R1} or S_{R7} short-circuit

If device S_{R1} or S_{R6} fails short-circuit, when the controller sequentially activates devices $S_{R2}\rightarrow S_{R6}$ to obtain switching-state (2XX), or $S_{R1}\rightarrow S_{R5}$ to obtain

switching-state (3XX), under the standard switching scheme shown in Table 4.6 then a capacitor discharge path occurs for capacitor C_1. Although the effect to the capacitor, and the route of the discharge path are identical, the distribution of 'lost' switching-states and resultant inherent operational robustness is very different.

Observation of the nodal state plane for the 6-level structure in the event of S_{R1} failing short, Figure 4.29, shows the distribution of a large number (36) of unobtainable switching-states but only two of these reflect the complete loss of voltage vectors from the control scheme (nodes 65 and 77). The fact that the distribution is gathered towards the inner hexagonal of nodes due to the 'loss' of states (2XX) indicates that there exists an inherent robustness to this device fault, as the structure exhibits state redundancy in this region of its operating plane. Of the nodes affected by the fault the cyan shaded nodes retain voltage vector operational redundancy by a total of 85 possible switching-states. For a short-circuit fault to device S_{R6}, although the discharge path and capacitor are identical the overall effect on the continual operation is very different. The distribution of the 'lost' full voltage vector states (3XX) in the event of S_{R6} failing short-circuit is illustrated in Figure 4.30. As with the previous device failure, a total of 36 switching-states are 'lost'. Unfortunately, as 11 of the 36 states are on the outer hexagon of nodes, representing full voltage vectors, the system is inoperable and offers no level of inherent redundancy.

The analysis of short-circuit device faults to S_{R10} and S_{R5} shows an identical mirror image, across the β axis of the nodal plane, of 'lost' switching states due to short-circuit faults as their positional mirror image devices across the upper and lower phase limb, S_{R1} and S_{R6} respectively. Again identical discharging paths are provided to one capacitor, in this case C_5. Also, as with the previous analysis the central device S_{R5} failing short-circuit has a greater severity on the possibility of continual operation. The distribution of 'lost' switching-states, of the form (-2XX), for the short-circuit failure of S_{R10} is illustrated in Figure 4.31. For S_{R5} failing short, switching-states of the form (-3XX) are 'lost', as illustrated in Figure 4.32.

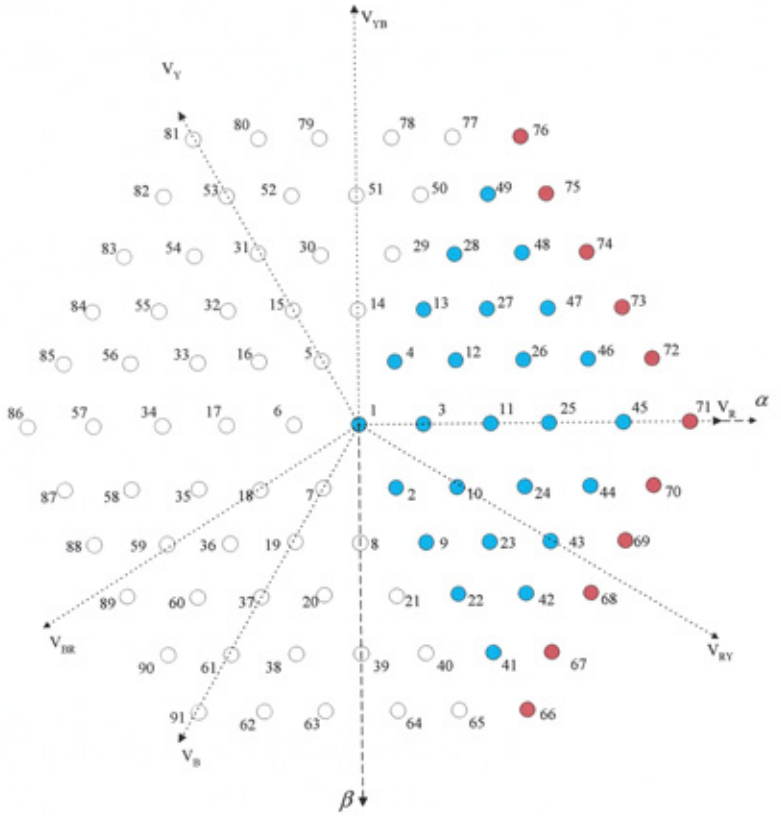


Figure 4.30 – Distribution of 'lost' states due to S_{R6} or CD_{R1} short-circuit

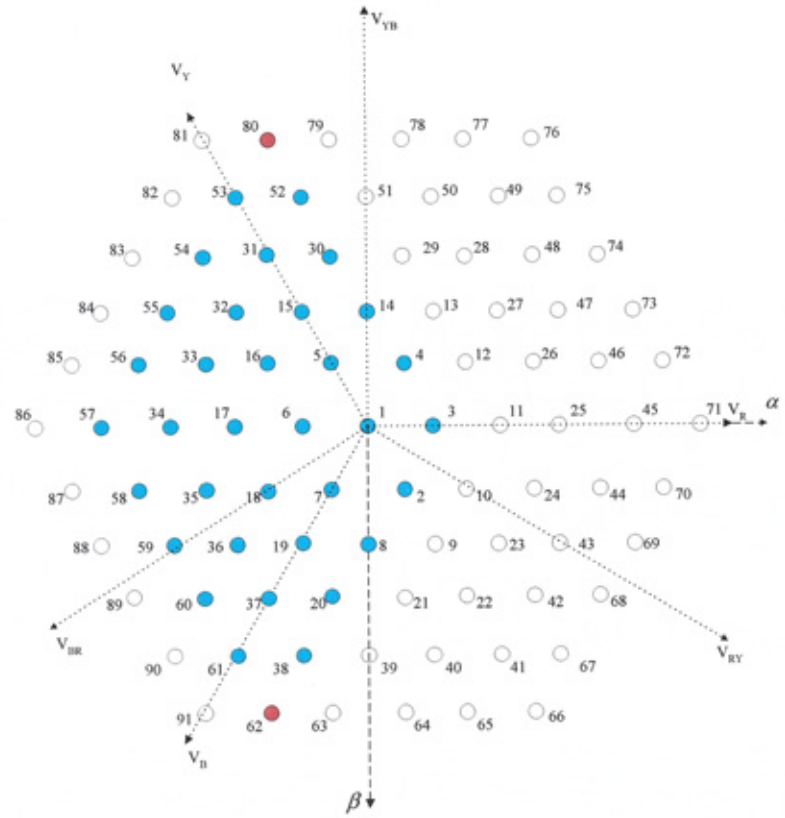


Figure 4.31 – Distribution of 'lost' states due to either S_{R10} or S_{R4} short-circuit

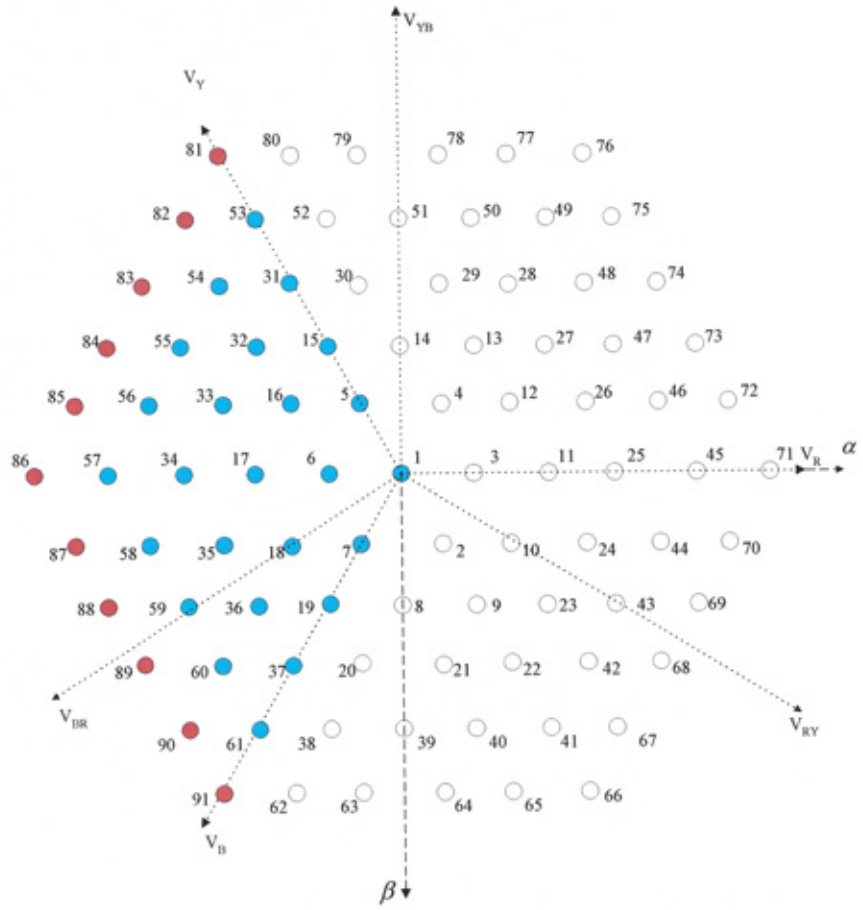


Figure 4.32 – Distribution of 'lost' states due to S_{R5} or CD_{R8} short-circuit

By analogy, device faults in the upper and lower halves of the phase limb will produce similar results. Hence, analysis of S_{R2} failing short-circuit is comparable with a short-circuit fault on S_{R9}. If under fault conditions the controller maintains a standard modulation pattern and activates $S_{R3} \rightarrow S_{R7}$ with S_{R2} short-circuit (or $S_{R4} \rightarrow S_{R8}$ with a short-circuit fault on device S_{R9}) a discharge path for capacitor C_2 or C_4 is created. The distribution of 'lost' switching-states is also similar in state redundancy and of resultant inherent operational robustness. In the event of S_{R2} failing short, states (1XX) are lost, as shown in Figure 4.33. Whereas, a failure to S_{R9} results in the 'loss' of states (-1XX), as shown in Figure 4.34. Comparison of the distribution of 'lost' switching-states across the nodal plane shows a mirror image distribution of the states across the inner nodal hexagon of the β axis, which exhibits an abundance of redundant switching-states obtainable through the control strategy.

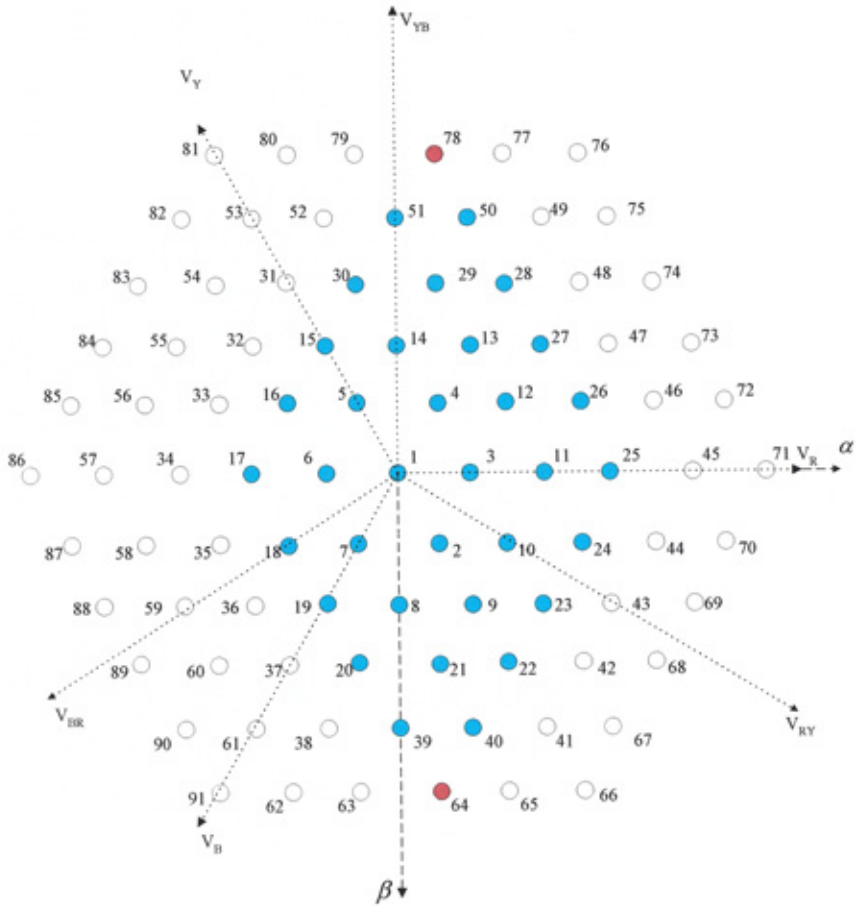


Figure 4.33 – Distribution of 'lost' states due to either S_{R2} or S_{R8} short-circuit

In the event of a short-circuit failure of devices S_{R3} or S_{R8} the analysis shows identical 'lost' states and distribution to the short-circuit failure investigations of S_{R9} and S_{R2}, respectively. The analysis only differs in the fact that it is now capacitor C_3 that is presented with a discharge path if the standard control scheme is maintained. With S_{R3} failing short-circuit the states (-1XX) are 'lost', as illustrated in Figure 4.34. Whereas, states (1XX) are 'lost' in the event of S_{R8} failing short-circuit, as shown in Figure 4.33. It is therefore acknowledged that a pattern of possible system redundancy is beginning to emerge throughout the phase limb switching devices not positioned as a central device.

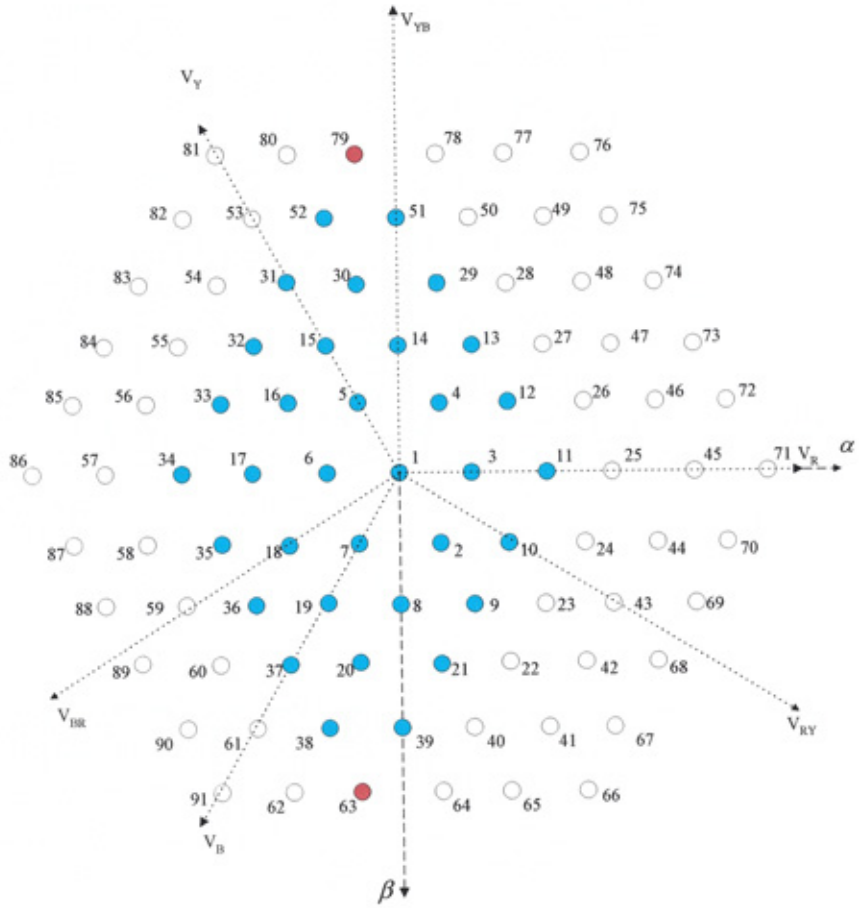


Figure 4.34 – Distribution of 'lost' states due to either S_{R9} or S_{R3} short-circuit

By analogy, short-circuit failure of devices S_{R4} and S_{R7} will produce similar results as failure of devices S_{R10} and S_{R1}, respectively. Therefore, a short-circuit fault to device S_{R4} will result in that switching-states (-2XX) are 'lost', as illustrated in Figure 4.31. In the case of S_{R7} failing short, switching-states (2XX) are 'lost', as illustrated in Figure 4.29.

Observation of the 6-level DCMLI topology shows that, as with the 3-level structure, a failure due to short-circuit of any auxiliary clamp-diode will have severe effects upon the continual operation. It can be deduced that if the outer clamp-diodes CD_{R1} or CD_{R8} fail short then states (3XX) and (-3XX) are 'lost', respectively. The results will be similar to failure of the central switching devices S_{R6} and S_{R5}, as illustrated in Figures 4.30 and 4.32. The distribution of 'lost' states

results in an inoperable system. The nodal distributions indicate that, as with the central device failure conditions, 11 full voltage vectors are completely lost.

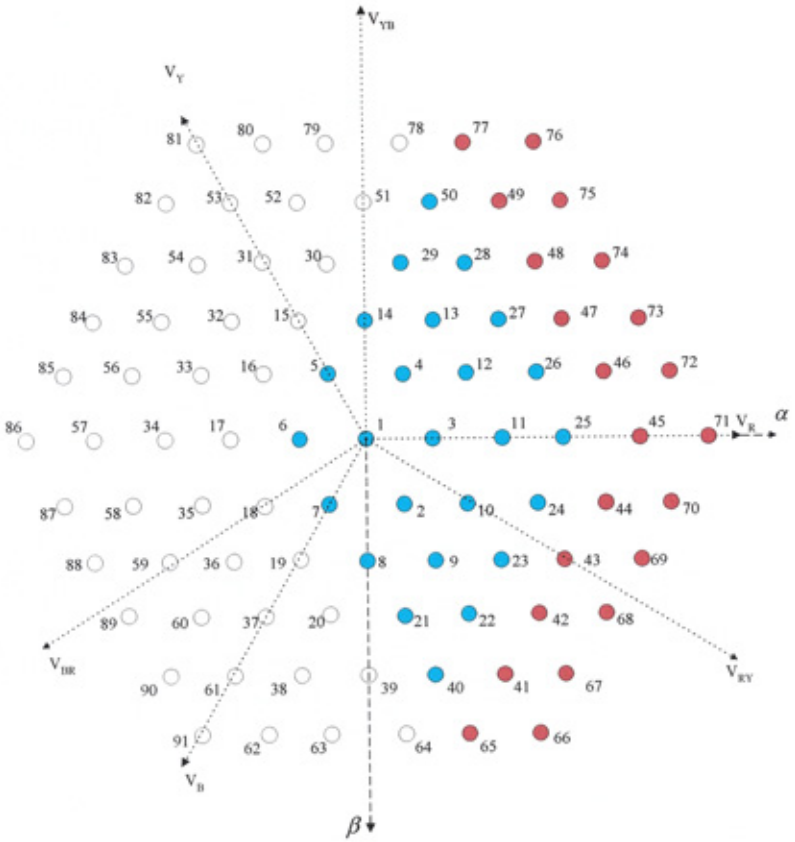


Figure 4.35 – Distribution of 'lost' states due to CD_{R2} short-circuit

As the positioning of the clamp-diodes moves towards the central point the impact of a short-circuit failure has more detrimental effect upon the system operation. In the event of devices CD_{R2} or CD_{R7} failing short then states (3XX) plus (2XX) or (-3XX) plus (-2XX) will be 'lost', respectively. The distribution of 'lost' states is illustrated for CD_{R2} failing short in Figure 4.35. The 'lost' state distribution for CD_{R7} failing short is not presented, as it is simply the mirror image of Figure 4.35 across the β axis.

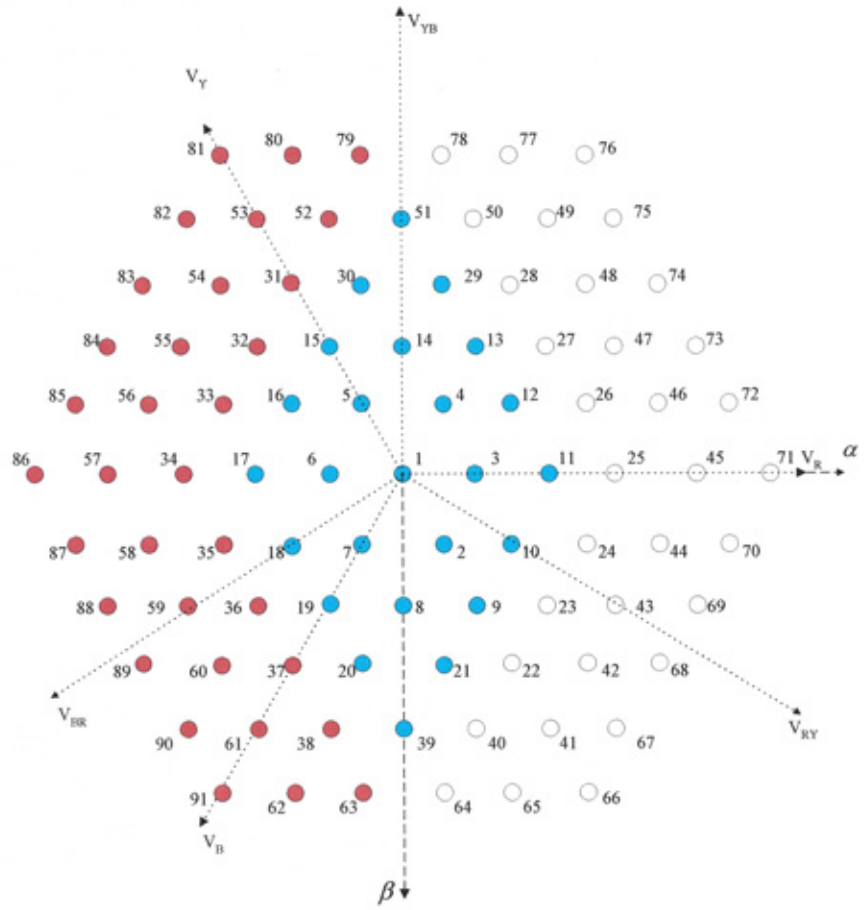


Figure 4.36 – Distribution of 'lost' states due to CD_{R6} short-circuit

When the device positioning moves further central the number of total voltage vectors 'lost' increases. If devices CD_{R3} or CD_{R6} fail short then another total switching-state is 'lost' in this case (1XX) and (-1XX), respectively. These together with the higher voltage state levels that are already lost due to the positioning of the clamp-diode result in three switching-states completely 'lost'. This is illustrated for CD_{R6}, where states (-3XX), (-2XX) and (-1XX) are 'lost', in Figure 4.36. The 'lost' state distribution for CD_{R3} failing short is simply the mirror image of Figure 4.36 across the β axis.

To finalise the short-circuit device investigations, the central clamp-diode devices CD_{R4} and CD_{R5} are considered. As can be predicted through the previous analysis, a short-circuit failure to either of these devices has a devastating effect on the continual performance as four switching-states are 'lost'. In the case of CD_{R4} states (3XX), (2XX), (1XX) and (-1XX) must be evaded by the controller to

prevent discharge paths to capacitors C_1, C_2, C_3, and C_4, respectively. The distribution of 'lost' states resulting from a short-circuit of CD_{R4} are illustrated in Figure 4.37. The 'lost' state distribution for CD_{R5} failing short is simply the mirror image of Figure 4.37 across the β axis.

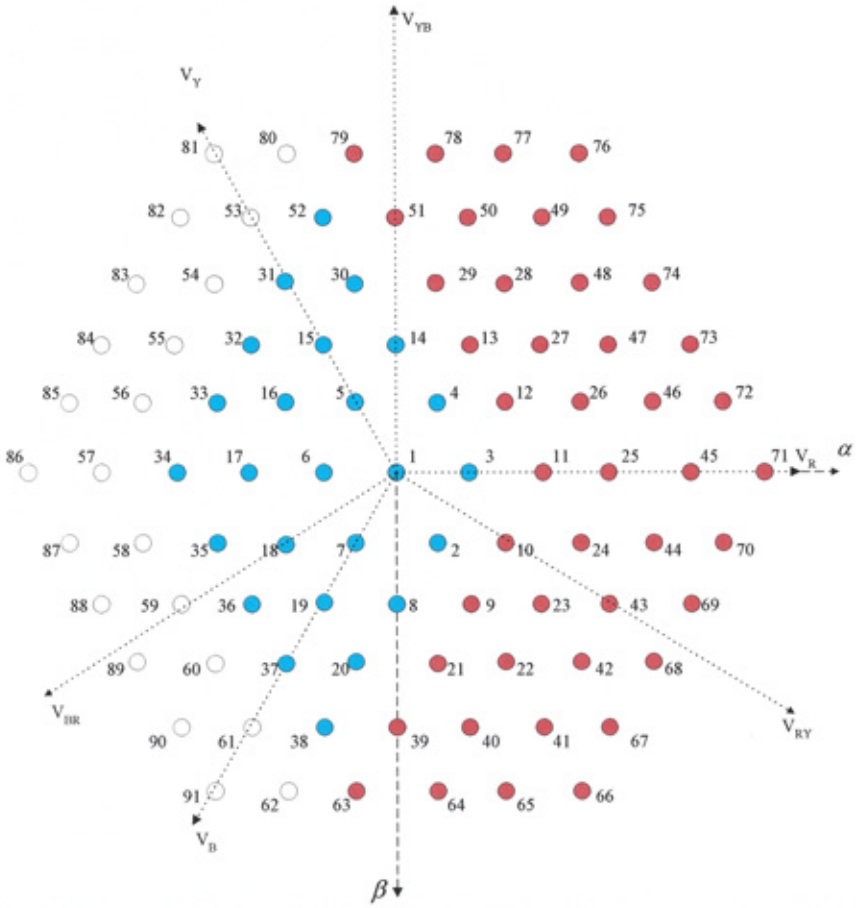


Figure 4.37 – Distribution of 'lost' states due to CD_{R4} short-circuit

The complete results for the short-circuit device faults for the 6-level DCMLI topology are given in Table 4.7. Observation of these results and the analysis presented shows that the even-level structure offers some apparent improvement, with respect to inherent operational robustness, over the odd-level inverter structure. This will be further discussed when the inherent redundancy investigations are summarised at the end of the Chapter.

Device	Number of states lost	Number of active vectors lost	Lost states of form
S_{R1}, S_{R7}	36	2	(2XX)
S_{R2}, S_{R8}	36	2	(1XX)
S_{R3}, S_{R9}	36	2	(-1XX)
S_{R4}, S_{R10}	36	2	(-2XX)
S_{R5}, CD_{R8}	36	11	(-3XX)
S_{R6}, CD_{R1}	36	11	(3XX)
CD_{R2}	72	22	(3XX), (2XX)
CD_{R3}	108	33	(3XX), (2XX), (1XX)
CD_{R4}	144	44	(3XX), (2XX), (1XX), (-1XX)
CD_{R5}	144	44	(-3XX), (-2XX), (-1XX), (1XX)
CD_{R6}	108	33	(-3XX), (-2XX), (-1XX)
CD_{R7}	72	22	(-3XX), (-2XX)

Table 4.7 - States lost due to short-circuit device failures

4.6.2 Open-Circuit Device Faults

As presented in the 3-level open-circuit investigations, analysis of the 6-level DCMLI structure shows that the number of 'lost' states and resultant voltage vectors increases as the faulty device position moves closer to the central device. The results of the 6-level open-circuit device failure investigations are given in Table 4.8. Observation of any of the nodal plane 'lost' state distributions, resulting from open-circuit switching device faults, would illustrate the limitations of the continual operation. As any switching device failing open-circuit would result in the system shutdown, only the worst-case scenario is presented. If device S_{R5} fails open-circuit then all switching-state sequences requiring this device to be closed would be inoperable. Therefore, states (3XX), (2XX), (1XX), (-1XX) and (-2XX) would all be 'lost' resulting in the loss of 55 voltage vectors as illustrated in Figure 4.38.

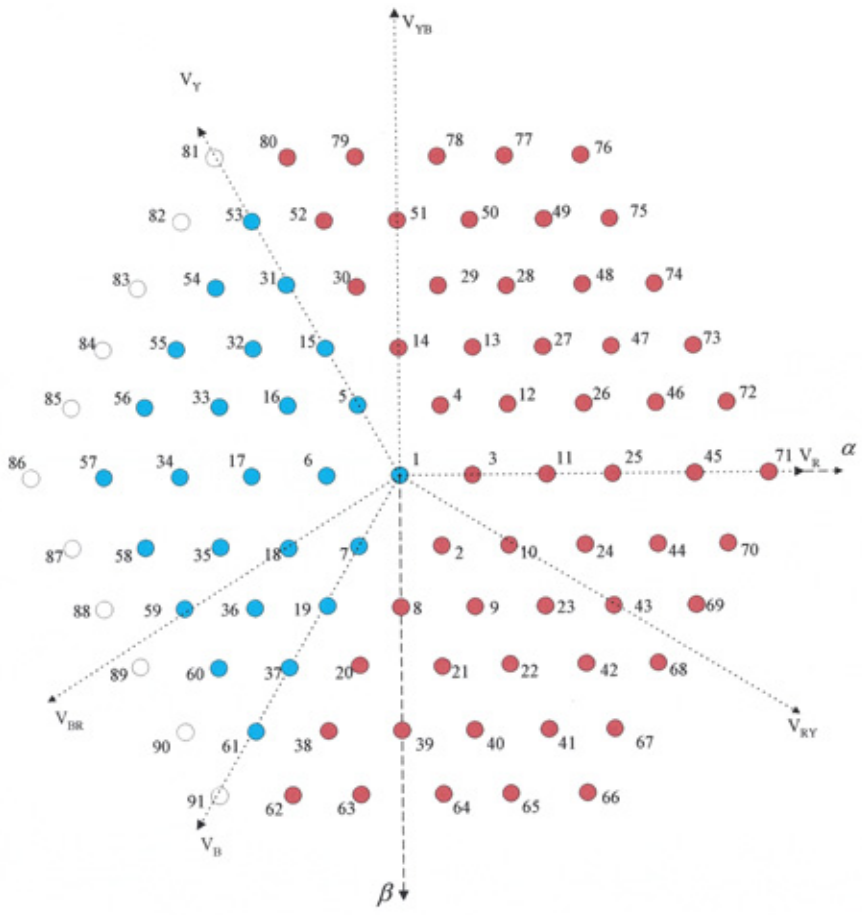


Figure 4.38 – Distribution of 'lost' states due to S_{R5} open-circuit

Observation of the clamp-diode open-circuit analysis results given in Table 4.8 shows that there is minimal effect to the system continual operation as only 2 full voltage vectors are 'lost'. Also, there are no conditions when the d.c. rail switching-states (3XX) or (-3XX) are 'lost'. Therefore, it is possible to obtain full d.c. voltage levels, hence maintaining the output power rating performance of the 6-level VSI. However, although the loss of switching-states (2XX) and (-2XX) or (1XX) and (-1XX) will not cause an inoperable system it will result in a drop of operational level to a 4-level system. This presents a possibility of inherent operational redundancy in the topology. To illustrate the effect of a clamp-diode failing open-circuit, the distribution of 'lost' states resulting from failure of devices CD_{R1}or CD_{R5} is given in Figure 4.39.

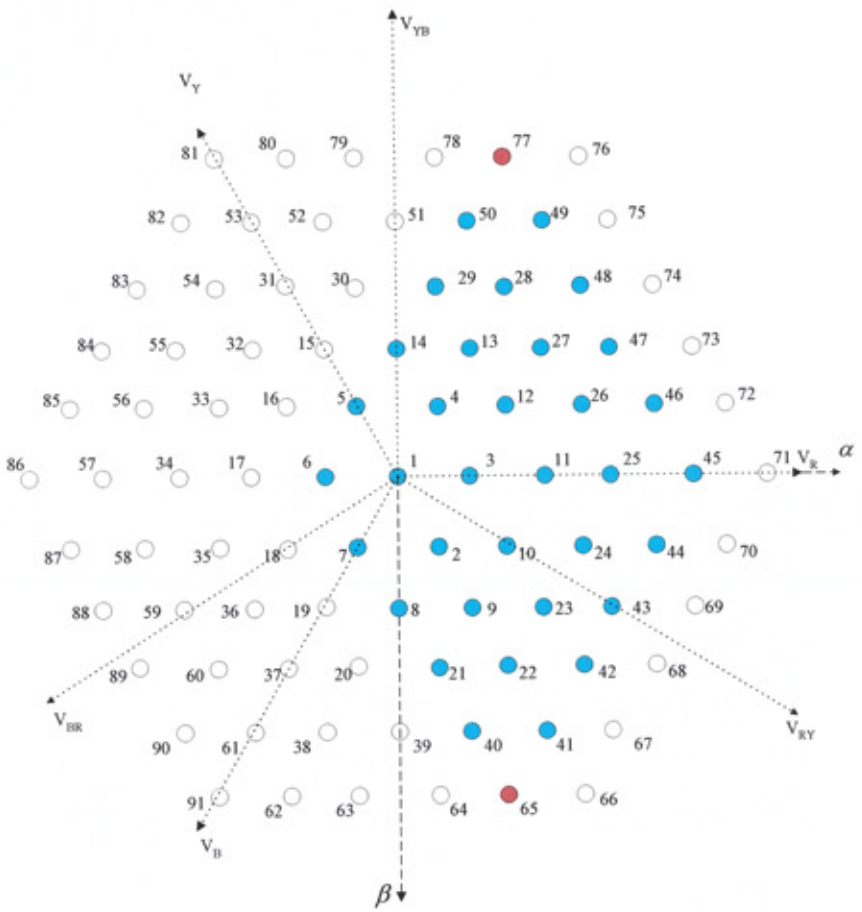


Figure 4.39 – Distribution of 'lost' states due to CD_{R1} or CD_{R5} open-circuit

Device	Number of states lost	Number of active vectors lost	Lost states of form
S_{R1}	36	11	(3XX)
S_{R2}	72	22	(3XX), (2XX)
S_{R3}	108	33	(3XX), (2XX), (1XX)
S_{R4}	144	44	(3XX), (2XX), (1XX), (-1XX)
$S_{R5,}$	180	55	(3XX), (2XX), (1XX), (-1XX), (-2XX)
$S_{R6,}$	180	55	(-3XX), (-2XX), (-1XX), (1XX), (2XX)
S_{R7}	144	44	(-3XX), (-2XX), (-1XX), (1XX)
S_{R8}	108	33	(-3XX), (-2XX), (-1XX)
S_{R9}	72	22	(-3XX), (-2XX)
S_{R10}	36	11	(-3XX)
CD_{R1}or CD_{R5}	36	2	(2XX)
CD_{R2} or CD_{R6}	36	2	(1XX)
CD_{R3} or CD_{R7}	36	2	(-1XX)
CD_{R4} or CD_{R8}	36	2	(-2XX)

Table 4.8 - States lost due to open-circuit device failures

4.7 SUMMARY OF INHERENT REDUNDANCY INVESTIGATION

An investigation into the inherent operational redundancy of the conventional six-pulse (2-level) and the diode-clamped multi-level inverter (DCMLI) topologies of levels 3 to 6 has been performed. Throughout this Chapter the analysis for the 2, 3 and 6-level inverter structures has been presented. The phase limbs and space-vector nodal planes for the 4 and 5-level VSI topologies are given in Appendix B. A summarized table of results for the redundancy investigations, applied to these topologies, is also presented. The topologies have been investigated in response to short or open-circuit switching and clamp-diode device faults.

In all topologies investigated an open-circuit switching device fault would result in an inoperable system, hence no inherent redundancy. This is largely to do with the structural arrangement of the phase limbs. As the limbs are a series connection of valves, if a device fails open-circuit it is impossible to achieve a voltage level of which the switching controller would need to activate the faulty device. Therefore, in the case of a high multi-level structure, not only would it prevent the clamping voltage level of its positioning within the phase limb but also any voltage levels that included the device in the switching sequence. A structural arrangement to improve the redundancy in the event of an open-circuit would be the connection of parallel devices, or limbs, to be activated if necessary. Unfortunately, this arrangement may prove very expensive to implement and would therefore only be possible if the inverter's continual operation was unquestionably necessary, for example an aircraft's fuelling system.

Analysis of the open-circuit failure of clamp-diodes in the multi-level structures indicated a stronger possibility of inherent redundancy. Due to only 2 full voltage vectors being 'lost' for any 'level' topology or any positioning of clamp-diode within the structure, the DCMLI topology shows an inherent operational redundancy and robustness to this type of fault. The analysis illustrates that in the event of clamp-diodes failing open-circuit the multi-level under investigation can revert to a 'lower' level operation. It is therefore possible for the multi-level structure, applied for the ASVC application, to maintain reactive compensation

requirements, albeit at a reduced operational harmonic performance. This 'drop' of operational 'level' to maintain operation will be further discussed for individual topologies later.

The short-circuit device failure investigations demonstrated that the six-pulse (2-level) VSI topology offers no inherent redundancy in the event of a switching device fault. Therefore, as is presently applied in industrial applications, the connection of redundant series devices within each valve appears the only option for reducing the possibility of shutdown due to device short-circuits.

However, the diode-clamped multi-level topology short-circuit fault analysis illustrates mixed results. The analysis demonstrated that for all 'levels' of the VSI topology if a central positioned switching device fails short-circuit the structure offers no inherent redundancy and the system is inoperable. This would result in either shutdown of the inverter system, or the necessity to reduce the possibility of shutdown by redundant (back-up) devices. This case is also observed from the clamp diode analysis. In the event of a short-circuit fault, the DCMLI structure and positioning of the clamp-diodes resulted in severe effects on the continual operation of the system. The number of full voltage vectors 'lost' illustrated that the DCMLI structure offered no inherent redundancy or robustness to a clamp-diode short-circuit fault.

Although the results of the redundancy analysis of the standard DCMLI structure are by now looking very disillusioning, some inherent redundancy is observed throughout the investigation. Considering the 6-level structure, results obtained show that for short-circuit faults to switching devices, other than the centrally positioned, the topology offers a possibility of reducing the operational 'level', as explained in the following.

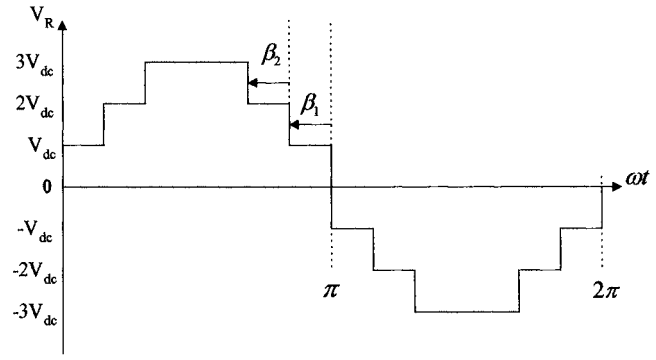


Figure 4.40 – Six-level output phase voltage

The stepped waveform of the 6-level output phase voltage, shown in Figure 4.40, exhibits two step angles, β_1 and β_2, for control of the waveform. If in the event of S_{R1} or S_{R7} and S_{R4} or S_{R10} failing short-circuit, then switching states (2XX) or (-2XX) respectively would be 'lost'. To prevent the generation of even harmonics in the output waveform, if either state (2XX) or (-2XX) were 'lost' then the corresponding inverse state would have to be sacrificed. Therefore, as shown in Figure 4.41, the obtainable output waveform would be reduced to four-levels.

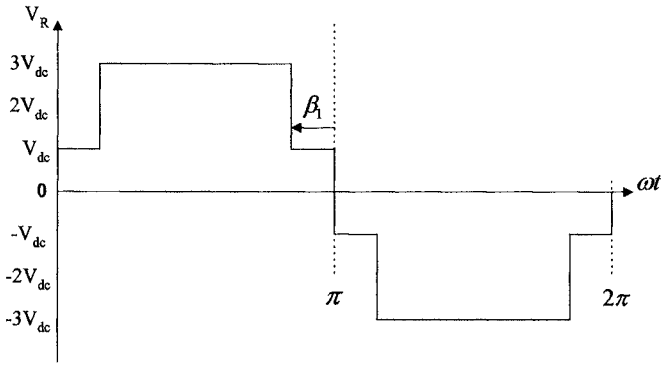


Figure 4.41 – Output phase voltage, state (2xx) or (-2XX) 'lost'

A short-circuit failure to devices S_{R2} or S_{R8} and S_{R3} or S_{R9} results in 'loss' of states (1XX) and (-1XX), respectively. Again for harmonic symmetry within the phase voltage waveform the corresponding inverse state would also have to be

sacrificed. So as with the previous case a 4-level waveform, as shown in Figure 4.42, with one modulation control angle is the only obtainable waveform.

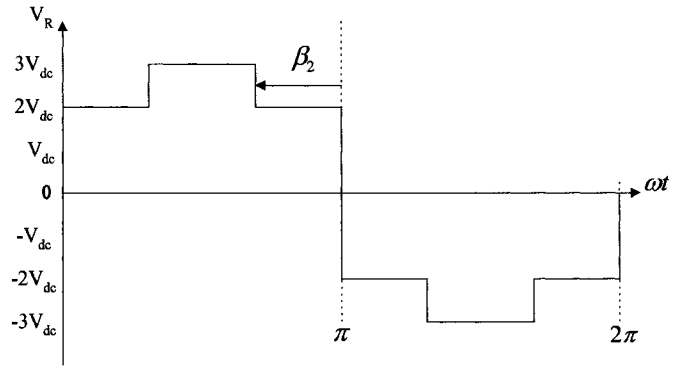


Figure 4.42 – Output phase voltage, state (1xx) or (-1XX) 'lost'

This illustrates some, albeit very limited, inherent redundancy and robustness to a device short-circuit fault. As only an intermediate voltage level is 'lost' from the 6-level phase waveform the system can revert to a 4-level operation. Although this may result in an increase in harmonic content of the output waveforms, control of the remaining modulation angles in either case offers suitable redundancy of maintaining output power levels. The analysis of 3 to 6-level DCMLI structures demonstrated this limited inherent redundancy to revert to 'lower' level operation under some short-circuit switching device or clamp-diode open-circuit faults. The possible 'level' redundancy for the investigated levels is given in Table 4.9.

DCMLI level in normal operating conditions	**Possible redundancy 'level' in abnormal operating conditions**
Three	Two
Four	Two
Five	Three
Six	Four

Table 4.9 – Operation 'level' in normal and abnormal device fault conditions

Obviously to maintain a balanced three-phase output, the reduction of output phase voltage 'level' has to be across all three-phases of the voltage source inverter. To illustrate the resultant limitations of modulation control, and reduction of operational 'level' across the three-phases, the 3-level DCMLI structure space-vector nodal plane is used. As the three-phase output voltage waveforms exhibit the conventional 120° phase shifts between phases, the nodal plane exhibits identical node shifts. Therefore, in the event of S_{R1} or S_{R4} failing short-circuit, or CD_{R1} or CD_{R2} failing open-circuit, the (0XX) states are 'lost', as shown in Figure 4.43. As the (0XX) states are 'lost' in the red (R) phase, they must also be sacrificed in the yellow (Y) and blue (B) phases to maintain a balanced three-phase output. The distribution of 'lost' (0XX) states is illustrated for the yellow and blue phases in Figures 4.44 and 4.45, respectively.

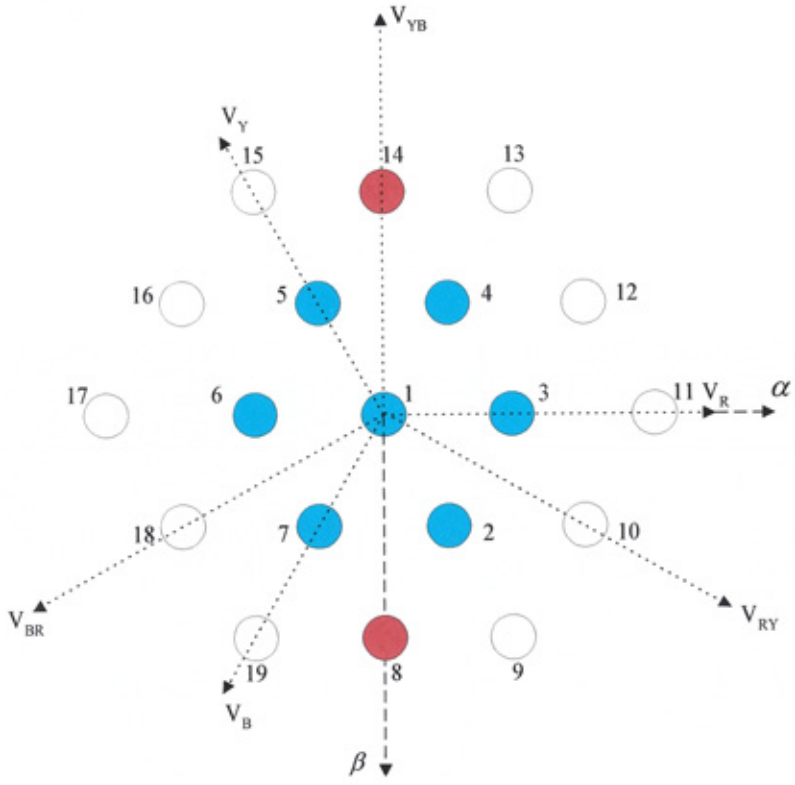


Figure 4.43 – Distributions of 'lost' (0XX) states for phase R.

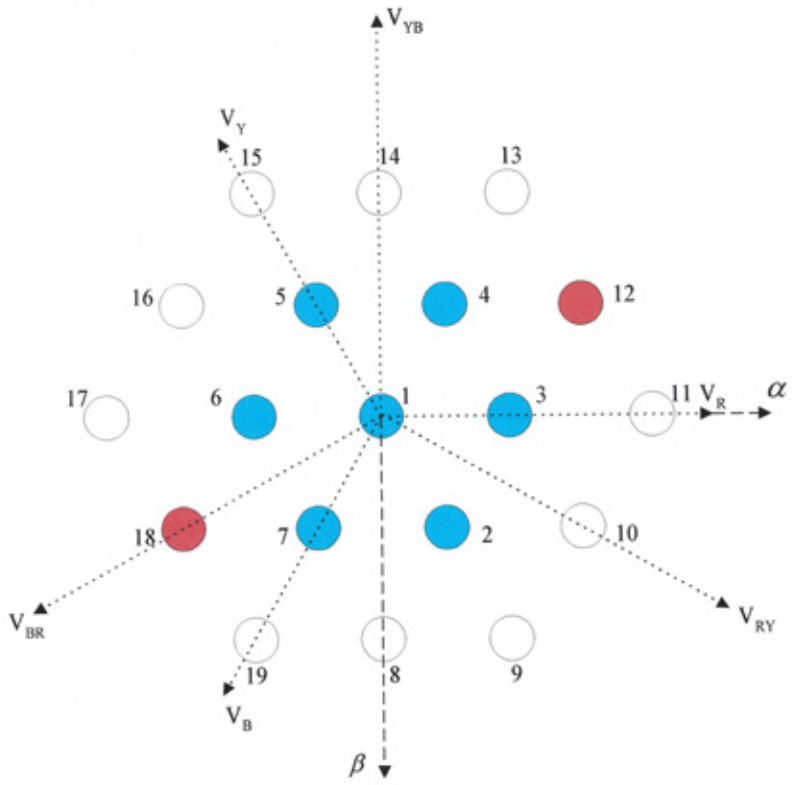


Figure 4.44 – Distributions of 'lost' (0XX) states for phase Y

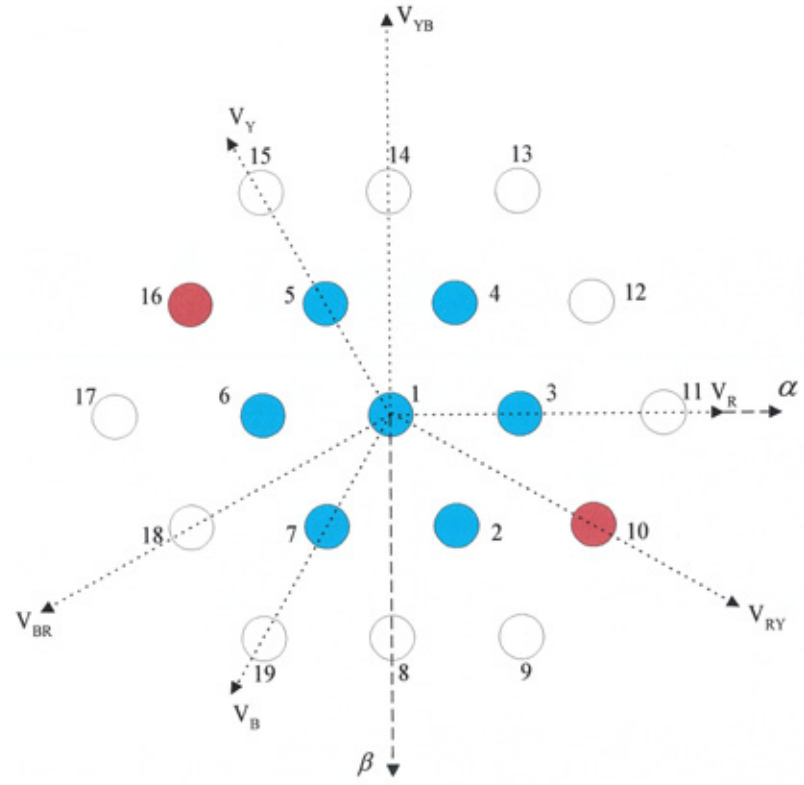


Figure 4.45 – Distributions of 'lost' (0XX) states for phase B

Therefore, if all the (0XX) states are removed from the space-vector nodal plane the resultant system is a 2-level inverter, as illustrated in Figure 4.46. With correctly sequenced bi-polar switching-state control of these resultant nodes it is possible to produce the required three-phase 2-level VSI output line voltages.

As the three-phase 3-level DCMLI structure is to be the particular focus of the remaining Chapters of this thesis, the results of the full inherent redundancy investigations showing possible redundancy and shutdown is illustrated as a flow diagram in Figure 4.47. At the end of the 3-level device fault flow diagram it is illustrated that in the event of the system reverting to a bi-polar switching scheme, the harmonic performance may be recovered by increasing the switching frequency. This will be further discussed in the following Chapter.

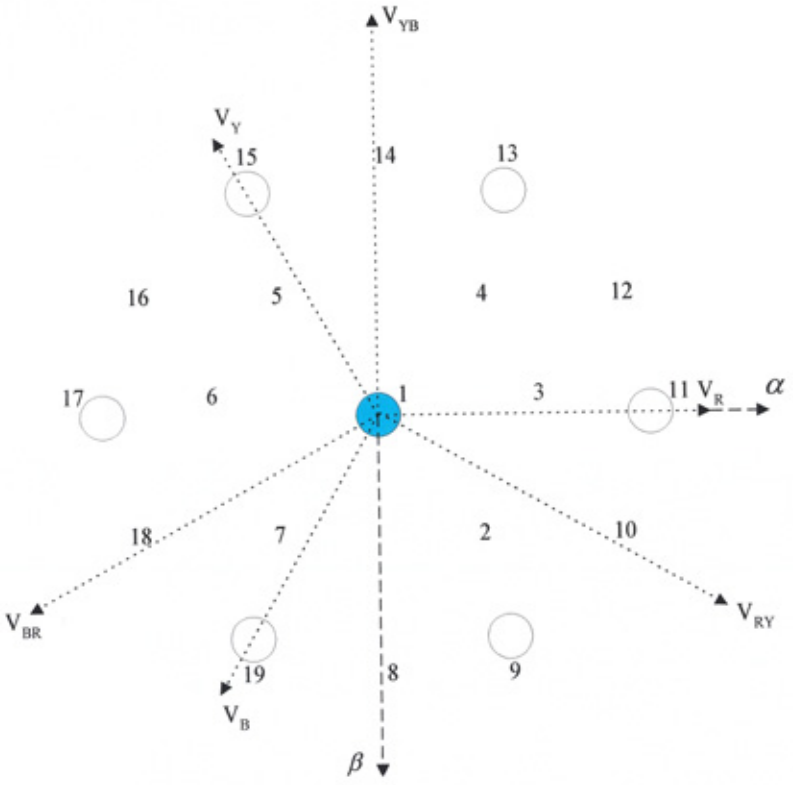


Figure 4.46 – Remaining Voltage Vector nodes for VSI operation

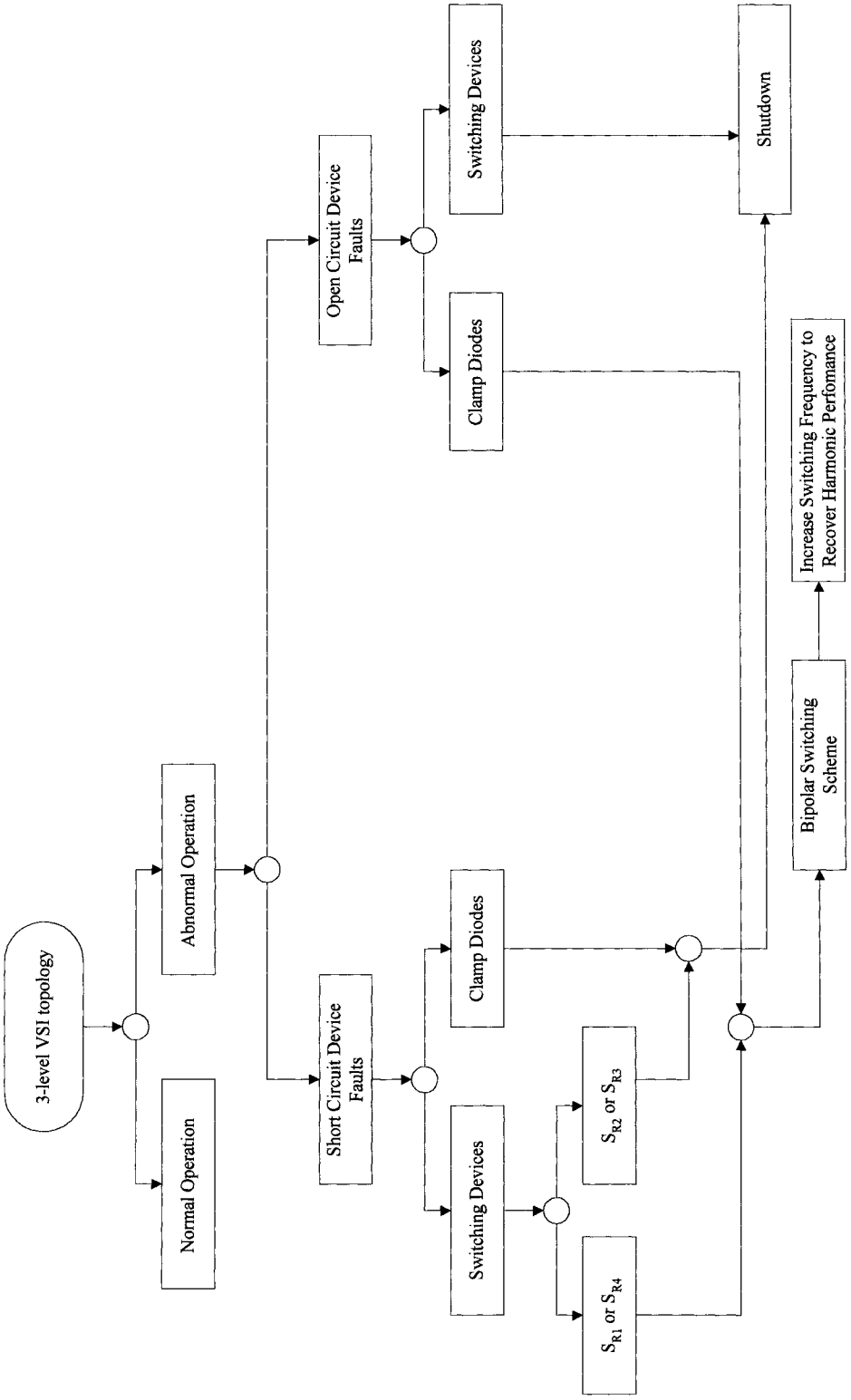


Figure 4.47 – Three-level Device Fault Flow Diagram

5 HARMONIC ANALYSIS & PERFORMANCE RECOVERY DURING ABNORMAL OPERATING CONDITIONS

5.1 INTRODUCTION

The redundancy analysis presented in the last Chapter has illustrated that, for certain device fault events, the diode-clamped multi-level VSI can maintain operation through reduction in the operating 'level' of the inverter. The limitation of this inherent redundancy is that it would also result in degradation in harmonic performance. Therefore, for continual harmonic performance through abnormal device fault conditions, the multi-level VSI controller must provide adaptive switching control schemes, which can 'recover' the harmonic spectrum of the normal operation.

This Chapter presents harmonic analysis of the 3-level DCMLI structure under normal operating conditions. The possibilities of utilising 'lower' level modulation strategies to recover the harmonic performance under abnormal conditions are also investigated.

5.2 HARMONIC ANALYSIS OF THE 3-LEVEL VSI

In normal operating conditions, modulation of the 3-level output voltage is dependant upon the application, the inverter rating and the utilised topology e.g. multi-bridge transformer array topology or stand-alone bridge. The former topology arrangement would typically utilise the fundamental frequency modulation (FFM) implementing minimum switching frequency.

Minimising the harmonic distortion to meet the appropriate standards (e.g. G5/3 [50]) is achieved by using an appropriate multiple transformer arrangement. The stand-alone topology would not have this freedom of elimination through phase cancellation and would therefore require an increase in switching frequency to obtain the required harmonic spectrum. The most suitable low frequency PWM

scheme for high power systems is the optimised Selective Harmonic Elimination Modulation (SHEM) scheme. Typical methods of harmonic optimisation used are improvement of the entire spectra or elimination of certain low order harmonic components. The following sections demonstrate the harmonic optimisation procedures for the stand-alone 3-level VSI, operated with either FFM or SHEM, and the methodologies of harmonic recovery under abnormal conditions.

5.3 FUNDAMENTAL FREQUENCY MODULATION (FFM)

5.3.1 THREE-LEVEL VSI

The phase and line voltages of a 3-level inverter operated with a FFM switching control strategy are shown in Figure 5.1. As indicated above, the harmonic optimisation can be implemented in two forms, elimination of certain low order harmonics, or improvement of the entire spectra.

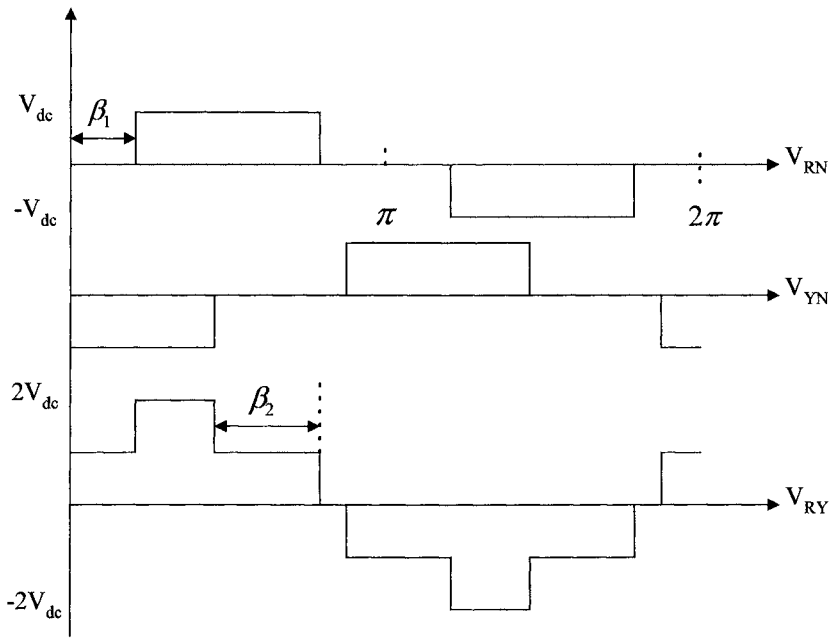


Figure 5.1 – FFM phase and line voltages of the 3-level VSI

For the 3-level VSI output phase R voltage, shown in Figure 5.1, the Fourier expression with FFM and the respective Fourier coefficient can be shown (Appendix C) as:

$$V_{RN}(\omega t) = \sum_{n=1}^{\infty} b_n \sin(n\omega t) \qquad (5.1)$$

where

$$|bn| = 0 \qquad \text{for even n}$$

$$|b_n| = \frac{4.V_{dc}}{\pi.n}\left(\cos(n\beta_1)\right) \qquad \text{for odd n} \qquad (5.2)$$

V_{dc} = d.c. bus voltage, n = harmonic component and β_1 = Modulation angle.

That is,

$$V_{RN}(\omega t) = \frac{4.V_{dc}}{\pi}.\sum_{n=1}^{\infty}\frac{1}{n}\left[\cos(n\beta_1)\right].\sin(n\omega t) \qquad (5.3)$$

Considering the elimination of individual harmonics, observation of equations (5.1)-(5.3) shows that by controlling the modulation-switching angle β_1, one specific harmonic may be eliminated. Hence, for elimination of individual harmonics the Fourier coefficient is equated to zero. Elimination of the low-order harmonics is of particular importance as they are more difficult to filter. The modulation switching angles required to eliminate, individually, the 5^{th}, 7^{th} or 11^{th} harmonics from the 3-level output phase voltage are found from equation 5.2 as:

$$\cos(5.\beta_1) = 0 \qquad (5.4)$$

Hence, to eliminate the 5^{th} harmonic $\beta_1 = 18°$.

For elimination of the 7^{th} harmonic:

$$\cos(7.\beta_1) = 0 \qquad (5.5)$$

Hence, $\beta_1 = 12.86°$.

For elimination of the 11^{th} harmonic:

$$\cos(11.\beta_1) = 0 \tag{5.6}$$

or $\beta_1 = 8.18°$.

Implementing any of these modulation angles into the 3-level control strategy will remove the unwanted harmonic component from the spectrum. However, if only one harmonic quantity was removed from the overall spectrum the remaining low-order harmonics would remain at almost full amplitude and large filters would be required. In this work the spectrum of the 3-level waveform is used as a performance indicator. To do this, the line voltage total harmonic distortion is minimised [30].

From Fourier analysis the yellow (Y) phase of the 3-level output waveforms, given in Figure 5.1, can be written as:

$$V_{YN}(\omega t) = \sum_{n=1}^{\infty} b_n \sin\left(n\left(\omega t - \frac{2\pi}{3}\right)\right) \tag{5.7}$$

Therefore, the line voltage, V_{RY}, can be written (Appendix C) as:

$$V_{RY}(\omega t) = \sum_{n=1}^{\infty} b_n \left[\sin n(\omega t) - \sin n\left(\omega t - \frac{2\pi}{3}\right)\right]$$

Where $$\left[\sin n(\omega t) - \sin n\left(\omega t - \frac{2\pi}{3}\right)\right] = 2.\cos n\left(\frac{\pi}{6}\right).\sin n\left(\omega t + \frac{\pi}{6}\right)$$

$$2\cos n\left(\frac{\pi}{6}\right) = 0 \qquad \text{for n = 3, 9, 15, 21...}$$

$$2\cos n\left(\frac{\pi}{6}\right) = \sqrt{3} \qquad \text{for n = 1, 5, 7, 11, 13...}$$

Substitution into the Fourier series:

$$V_{RY}(\omega t) = \frac{4.\sqrt{3}.V_{dc}}{\pi}.[\cos\beta_1.\sin\left(\omega t + \frac{\pi}{6}\right) - \frac{1}{5}\cos 5\beta_1.\sin 5\left(\omega t + \frac{\pi}{6}\right) - \frac{1}{7}\cos 7\beta_1.\sin 7\left(\omega t + \frac{\pi}{6}\right)$$

$$+ \frac{1}{11}\cos 11\beta_1.\sin 11\left(\omega t + \frac{\pi}{6}\right) + \frac{1}{13}\cos 13\beta_1.\sin 13\left(\omega t + \frac{\pi}{6}\right).....] \quad (5.8)$$

However, observation of the line voltage in Figure 5.1 shows a 5-level output waveform. Therefore, as with the 3-level phase waveform, the Fourier expression for the line waveform can be expressed as:

$$V(\omega t) = \frac{4.V_{dc}}{\pi}.\sum_{n=1}^{\infty}\frac{1}{n}[\cos(n\beta_1) + \cos(n\beta_2)].\sin(n\omega t) \quad (5.9)$$

As the waveform is the resultant difference between the red (R) and yellow (Y) phases, β_1 for a balanced 3-phase system will be equal to $((\pi/3)- \beta_2)$. Substituting into equation (5.9) gives:

$$V(\omega t) = \frac{4.V_{dc}}{\pi}.\sum_{n=1}^{\infty}\frac{1}{n}\left[\cos\left(n\left(\frac{\pi}{3} - \beta_2\right)\right) + \cos(n\beta_2)\right].\sin(n\omega t) \quad (5.10)$$

The total harmonic distortion (THD) of the line voltage can then be minimised by selection of the modulation angle β_2. The total harmonic voltage distortion of a waveform can be defined as:

$$THD_v = \sqrt{\frac{V_t^2}{V_f^2} - 1} \quad (5.11)$$

Where V_t = the rms value of the waveform

V_f = the rms value of the fundamental component waveform

The square of the fundamental component of the line voltage is given as:

$$V_f^2(1) = \frac{8 \cdot V_{dc}^2}{\pi^2} \cdot \left\{ \cos\left(\frac{\pi}{3} - \beta_2\right) + \cos(\beta_2) \right\}^2 \tag{5.12}$$

Whereas, the square of the rms value of the line waveform is:

$$V_t^2 = \frac{V_{dc}^2}{\pi} \cdot \left\{ \frac{10 \cdot \pi}{3} - 4 \cdot \beta_2 \right\} \tag{5.13}$$

Substituting (5.12) and (5.13) into equation (5.11) and minimising by differentiating with respect to β_2 gives:

$$\frac{d\left(\frac{V_t^2}{V_f^2}\right)}{d(\beta_2)} = -\frac{1}{2} \cdot \frac{1}{\left(\sin\left(\frac{1}{6} \cdot \pi + \beta_2\right) + \cos(\beta_2)\right)^2} - \frac{1}{4} \cdot \pi \cdot \frac{\left(\frac{10}{3} \cdot \pi - 4 \cdot \beta_2\right)}{\left(\sin\left(\frac{1}{6} \cdot \pi \cdot \beta_2\right) + \cos(\beta_2)\right)^3} \cdot \left(\cos\left(\frac{1}{6} \cdot \pi + \beta_2\right) - \sin(\beta_2)\right) \tag{5.14}$$

This equation was plotted to observe the angular value when the plot crosses zero, as illustrated in Figure 5.2. This indicates that the minimum value of total harmonic voltage distortion occurs with $\beta_2 = 0.785$ radians.

Converting into degrees and substituting due to $\beta_1 = ((\pi/3) - \beta_2)$, gives the minimum THD% over the entire spectrum with $\beta_1 = 15°$. By re-substitution of this modulation switching angle into the line voltage equation (5.8) the amplitudes of the individual harmonic components can be determined. Calculated as percentage magnitude, with respect to the fundamental, the harmonic table (Table 5.1)

illustrates the benefits of optimising the entire spectra as appose to elimination of individual harmonic components.

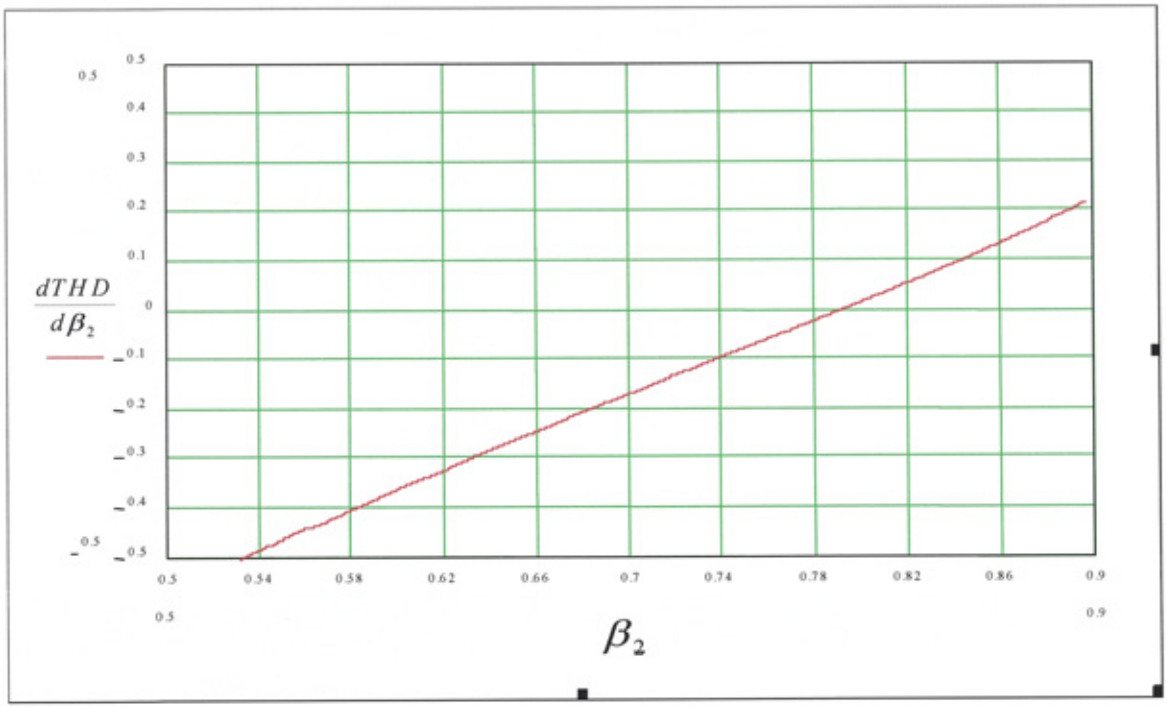


Figure 5.2 – Minimisation plot of THD_V from modulation angle β_2

Considering the percentage THD for each case in Table 5.1 shows similar levels of harmonic energy when components, below and including the 49th, are calculated as a performance indicator of the quality of the voltage spectra to the fundamental component. Column 1 shows a favourable result for the high power optimised spectra modulation angle criteria. The amplitudes of the 5th and 7th low order harmonic components, resulting from the optimised modulation angle, are greatly reduced from the worst-case scenario of 20% and 14.2% possible from a non-optimised waveform, β_1=0°. Observation of the remaining three columns, which show the resultant amplitudes when an individual component is targeted, illustrates that the harmonic energy from the eliminated component is dispersed across the remaining spectra. Therefore, the low order harmonic elimination is obtained at the expense of the higher frequency component amplitudes. For high power applications this is still considered preferential as the filtering requirements of the spectra become cheaper as the harmonic component frequency increases.

Harmonic Number	(b_n/b_1)% β_1=15°	(b_n/b_1)% β_1=18°	(b_n/b_1)% β_1=12.86°	(b_n/b_1)% β_1=8.18°
b_1	100	100	100	100
b_3	0	0	0	0
b_5	5.35	0	8.896	15.275
b_7	3.829	8.829	0	7.807
b_9	0	0	0	0
b_{11}	9.09	9.091	7.29	0
b_{13}	7.69	4.754	7.69	2.186
b_{15}	0	0	0	0
b_{17}	1.576	3.635	4.714	4.49
b_{19}	1.41	5.263	2.337	4.836
b_{21}	0	0	0	0
b_{23}	4.34	2.687	1.939	4.349
b_{25}	4	0	3.21	3.678
b_{27}	0	0	0	0
b_{29}	0.9	3.448	3.447	1.886
THD%	15.014	15.596	15.658	19.454

Table 5.1 – Harmonic % magnitude table for different values of β_1

5.3.2 TWO-LEVEL VSI

A bi-polar or 2-level fundamental frequency modulation (FFM) strategy, controlled at 180° as presented in Chapter 3, produces the phase and line voltages shown in Figure 5.3. Unlike the multi-level phase voltage waveforms, the 2-level controller has no modulation-switching angle. Therefore the 2-level waveform cannot be optimised at FFM to remove harmonics, as previously presented with the 3-level FFM waveform.

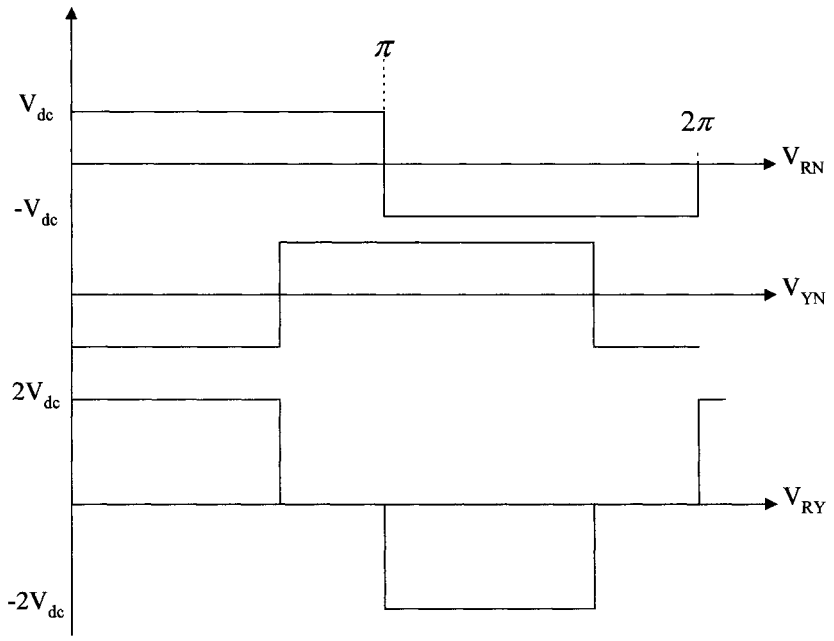


Figure 5.3 – FFM phase and line voltages of the 2-level VSI

From the waveforms illustrated in Figure 5.3, the 2-level phase voltage Fourier coefficient and resultant expression can be shown (Appendix C) as:

$$b_n = \frac{4.V_{dc}}{\pi.n} \tag{5.15}$$

$$V_{RN}(\omega t) = \frac{4.V_{dc}}{\pi.n}\sum_{n=1}^{\infty}\sin(n\omega t) \tag{5.16}$$

The line voltage Fourier series can be derived and expressed as:

$$V_{RY} = \frac{4\sqrt{3}V_{dc}}{\pi}\left[\sin\left(\omega t+\frac{\pi}{6}\right)-\frac{1}{5}\sin 5\left(\omega t+\frac{\pi}{6}\right)-\frac{1}{7}\sin 7\left(\omega t+\frac{\pi}{6}\right)+\frac{1}{11}\sin 11\left(\omega t+\frac{\pi}{6}\right)+.....\right] \tag{5.17}$$

Substituting these Fourier expressions and their respective coefficients into the individual harmonic % amplitude and total harmonic distortion equations, a

comparison between the 3-level FFM and 2-level FFM line voltage harmonic performance can be made, as shown in Table 5.2.

Observation of Table 5.2 illustrates and confirms predictions that the 2-level FFM strategy is not suitable for the continuation of the 3-level FFM harmonic performance under abnormal operating conditions. As the 2-level FFM line waveform is the phase difference between two standard square-waves, there is no possibility of 'recovering' the optimised FFM 3-level harmonic performance. Therefore, as predicted, higher frequency switching strategies will be required.

Harmonic Number	**(b_n/b_1)% 3-level Line Voltage β_1=15°**	**(b_n/b_1)% 2-level Line Voltage**
b_1	100	100
b_3	0	0
b_5	5.35	20
b_7	3.829	14.2
b_9	0	0
b_{11}	9.09	9.09
b_{13}	7.69	7.69
b_{15}	0	0
b_{17}	1.576	5.8
b_{19}	1.41	5.2
b_{21}	0	0
b_{23}	4.34	4.3
b_{25}	4	4
b_{27}	0	0
b_{29}	0.9	3.4
THD%	15.014	31.08

Table 5.2 – Harmonic % magnitude table for optimised 3-level FFM and 180° 2-level FFM

5.4 THREE-LEVEL SELECTIVE HARMONIC ELIMINATION MODULATION (SHEM)

The suitability of optimised PWM switching strategies for high power applications, requiring minimised harmonic distortion at low frequency switching, has now been generally recognised. Selected harmonic elimination techniques have been investigated and proposed as a variable PWM option for the stand-alone 3-level DCMLI based ASVC [51, 52].

Since the proposal of *'Selected Harmonic Reduction in Static DC-AC Inverters'* by Turnbull in 1964, the technique of eliminating low-order harmonic components with an off-line optimised PWM strategy has created much interest [53, 54]. The harmonic elimination (HE) technique, in principle, is quite simple. However, it requires the numerical solution of a number of non-linear equations, dependant upon the number of harmonics to be eliminated. Various mathematical techniques have been reported attempting to modify the numerical process, but generally the technique is found to exhibit multiple solutions for 3-phase systems [55]. Recently, Kato reported a graphical based solution, where a sequential homotopy-based computation of multiple solutions technique has been implemented to reduce the large non-linear equation solving process [56].

The optimised PWM harmonic elimination technique, which is now commonly referred to as Selective Harmonic Elimination Modulation (SHEM), consists of synthesising voltage waveforms with off-line calculated pulse patterns. By optimised selection of the pulse phase angle the specified orders of harmonics can be eliminated. A typical 3-level output phase voltage waveform, with one additional pulse (chop) per quarter cycle is shown in Figure 5.4. For analytical simplicity the voltage is normalised. As illustrated, the modulation strategy must maintain ½-cycle symmetry and ¼-cycle antisymmetry, therefore the Fourier series has only odd-order sine terms.

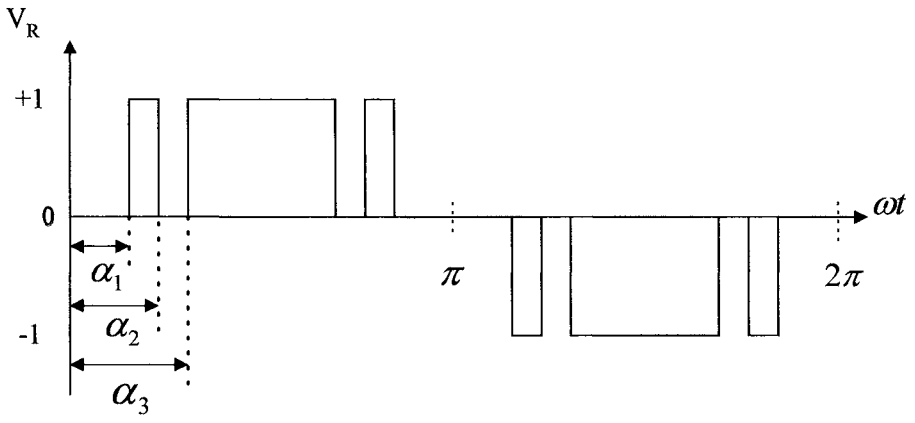


Figure 5.4 – 3-level SHEM output phase voltage waveform

The phase and line voltage waveforms can be expressed as:

$$V_{RN}(\omega t) = \sum_{n=1}^{\infty} b_n \sin(n\omega t)$$

$$V_{YN}(\omega t) = \sum_{n=1}^{\infty} b_n \sin\left(n\left(\omega t - \frac{2\pi}{3}\right)\right) \tag{5.18}$$

$$V_{RY}(\omega t) = \sum_{n=1}^{\infty} b_n \left[\sin n(\omega t) - \sin n\left(\omega t - \frac{2\pi}{3}\right)\right] \tag{5.19}$$

Therefore using the 3-level SHEM waveform in Figure 5.4, the Fourier coefficient can be derived, using ¼ -cycle Fourier analysis, as:

$$b_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} V.\sin(n\omega t)d(\omega t) \tag{5.20}$$

$$b_n = \frac{4}{\pi}.\left\{\int_0^{\alpha_1} 0.\sin(n\omega t)d(\omega t) + \int_{\alpha_1}^{\alpha_2} 1.\sin(n\omega t)d(\omega t) + \int_{\alpha_2}^{\alpha_3} 0.\sin(n\omega t)d(\omega t) + \int_{\alpha_3}^{\frac{\pi}{2}} 1.\sin(n\omega t)d(\omega t)\right\} \tag{5.21}$$

$$b_n = \frac{4}{\pi.n}\left\{\left[\frac{-\cos(n\omega t)}{n}\right]_{\alpha_1}^{\alpha_2} + \left[\frac{-\cos(n\omega t)}{n}\right]_{\alpha_3}^{\frac{\pi}{2}}\right\} \tag{5.22}$$

Which simplifies to:

$$b_n = \frac{4}{\pi.n}\left(\cos(n\alpha_1) - \cos(n\alpha_2) + \cos(n\alpha_3)\right) \tag{5.23}$$

Therefore the magnitudes of the individual harmonic components are given as:

$$|b_1| = \frac{4}{\pi}\left(\cos(\alpha_1) - \cos(\alpha_2) + \cos(\alpha_3)\right)$$

$$|b_5| = \frac{4}{\pi.5}\left(\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3)\right)$$

$$|b_7| = \frac{4}{\pi.7}\left(\cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3)\right) \tag{5.24}$$

$$|b_{11}|\frac{4}{\pi.11}\left(\cos(11\alpha_1) - \cos(11\alpha_2) + \cos(11\alpha_3)\right)$$

There are two techniques for the harmonic elimination solutions:

1 A constant voltage type, which exhibits no solution constraints on the fundamental component [57].

2 A variable voltage type, where the solution includes the constraint of fundamental magnitude control [53].

Due to the d.c. link voltage magnitude control technique, resulting from the basic operating characteristics of the VSI based ASVC, the former solution technique is

more suitable for the application. Whereas, with a high-power drive application, the later (variable voltage type) solution would be required due to a fixed d.c. link magnitude, but the possibility of different modulation indices of the fundamental component.

Therefore assuming a constant voltage (ASVC under ideal steady-state conditions with no d.c. ripple component), the following set of equations may be solved to eliminate the 5th, 7th and 11th harmonics from the output voltage spectrum.

$$\cos(5.\alpha_1) - \cos(5.\alpha_2) + \cos(5.\alpha_3) = 0 \qquad |b_5| = 0$$

$$\cos(7.\alpha_1) - \cos(7.\alpha_2) + \cos(7.\alpha_3) = 0 \qquad |b_7| = 0$$

$$\cos(11.\alpha_1) - \cos(11.\alpha_2) + \cos(11.\alpha_3) = 0 \qquad |b_{11}| = 0 \qquad (5.25)$$

A multiple set of solutions is possible. Therefore a solution must be selected that demonstrates the ability to eliminate the required harmonic and produce an adequate fundamental component. Using a Newton Raphson non-linear equation solution method, the following angles can be obtained which have been suggested as suitable for the 3-level ASVC application [51]:

$$\alpha_1 = 14.016°, \qquad \alpha_2 = 24.504° \text{ and } \alpha_3 = 30.288°$$

Substituting the Fourier coefficients in the line voltage equation gives:

$$V_{RY}(\omega t) = \frac{4}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\left(\cos(n\alpha_1) - \cos(n\alpha_2) + \cos(n\alpha_3)\right)\left[\sin n(\omega t) - \sin n\left(\omega t - \frac{2\pi}{3}\right)\right] \qquad (5.26)$$

Therefore, the individual harmonic magnitudes and resultant total harmonic voltage distortion can be calculated as with the FFM case. Comparative analysis is

summarized in Table 5.3, which shows the spectrum from the optimised FFM case and the SHEM case with the 5^{th}, 7^{th} and 11^{th} harmonics eliminated.

Harmonic Number	3-level Optimised FFM	3-level SHEM (3 angles)
b_1	100	100
b_5	5.36	0
b_7	3.83	0
b_{11}	9.09	0
b_{13}	7.69	7.64
b_{17}	1.576	12.60
b_{19}	1.41	3.38
b_{23}	4.34	12.3
b_{25}	4	9.01
b_{29}	0.9	4.58
THDv%	15.014	9.394

Table 5.3 – Harmonic content % and THDv % for the 3-level waveforms

The results illustrate the suitability of SHEM for the elimination of low-order harmonic components from the 3-level VSI output line voltage. A rise in the magnitude of the 17^{th}, and higher order harmonic components is resultant from any PWM scheme that eliminates the low-order spectra. To further improve the low-order spectrum more pulses, or chops, can be inserted into the 3-level waveform.

If there is no restriction in the switching frequency of the application of the VSI, the off-line calculated SHEM technique will eventually resemble a high frequency carrier PWM output waveform. As the ASVC is typically a high power application the modulation strategy must remain low frequency due to resulting power switching losses. Therefore, the elimination of the 5^{th}, 7^{th} and 11^{th} harmonics from the 3-level output voltage, as presented in [51,52], will be implemented into the ASVC control scheme.

5.4.1 Recovery of 3-level SHEM harmonic Performance Under Abnormal Operating Conditions

The 3-level DCMLI topology inherent redundancy investigations, presented in Chapter 4, illustrated that for certain device failure events the structure could 'revert' to a 2-level topology. The VSI switching controller would therefore have to be able to produce a bi-polar switching strategy. Continual performance of the VSI system is not the only critical condition. The harmonic performance of the 3-level VSI, under normal operation, would also have to be maintained throughout the abnormal operating conditions.

Due to the characteristics of the SHEM strategy, the possibility of 'recovering' the 3-level normal operation harmonic performance with a 2-level modulation strategy under abnormal conditions looks favourable. The objective is principally to maintain the low-order harmonic spectra of the 3-level output line voltage, whilst minimising the effect to the fundamental component. As indicated earlier, the operating characteristics of the VSI based ASVC maintain the required voltage level, by suitably adjusting the phase angle of the a.c. output voltage.

If an adaptive PWM scheme is implemented in abnormal conditions its operation can result in some slight difference in the fundamental component magnitude. In such case, the closed loop phase angle controller should either increase or decrease (dependant upon mode of operation) the d.c. voltage level. Therefore, the main objective of performance recovery is to remove the low-order harmonics to achieve the 3-level waveform harmonic spectrum.

As with the 3-level waveform, two pulses (or notches) resulting from 3 switching angles are required to remove the 5^{th}, 7^{th} and 11^{th} harmonics from the 2-level waveform. A normalised 2-level output phase voltage waveform is shown in Figure 5.5.

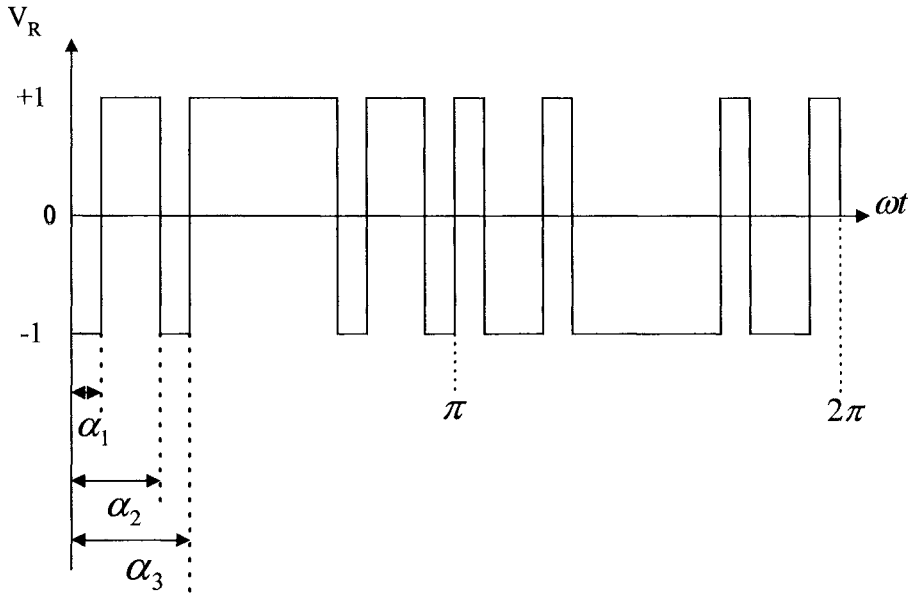


Figure 5.5 – Two-level output phase voltage waveform

It was presented in equation (5.16) that Fourier expression for the two-level FFM phase voltage waveform is:

$$V_{RN}(\omega t) = \frac{4.V_{dc}}{\pi.n}\sum_{n=1}^{\infty}\sin(n\omega t) \tag{5.27}$$

With a Fourier coefficient of:

$$b_n = \frac{4.V_{dc}}{\pi.n} \tag{5.28}$$

To eliminate the 5th, 7th and 11th harmonics from the 2-level voltage, the waveform shown in Figure 5.5 is required. Using ¼ -cycle Fourier analysis, the Fourier coefficient for the 2-level normalised voltage SHEM waveform can be derived as:

$$b_n = \frac{4}{\pi.n}.\left\{-1+2\cos(n\alpha_1)-2\cos(n\alpha_2)+2\cos(n\alpha_3)\right\} \tag{5.29}$$

Therefore, the magnitudes of the individual harmonic components are given as:

$$|b_1| = \frac{4}{\pi}.\{-1+2\cos(\alpha_1)-2\cos(\alpha_2)+2\cos(\alpha_3)\}$$

$$|b_5| = \frac{4}{\pi.5}.\{-1+2\cos(5.\alpha_1)-2\cos(5.\alpha_2)+2\cos(5.\alpha_3)\}$$

$$|b_7| = \frac{4}{\pi.7}.\{-1+2\cos(7.\alpha_1)-2\cos(7.\alpha_2)+2\cos(7.\alpha_3)\}$$

$$|b_{11}| = \frac{4}{\pi.11}.\{-1+2\cos(11.\alpha_1)-2\cos(11.\alpha_2)+2\cos(11.\alpha_3)\} \qquad (5.30)$$

As with the 3-level analysis, the 2-level harmonic coefficients are equated to zero and the resultant set of non-linear transcendental equations are solved. One of the multiple solutions obtained that is suitable for this application is [56]:

$$\alpha_1 = 8.74°, \qquad \alpha_2 = 24.397° \quad \text{and} \quad \alpha_3 = 27.76°$$

Substituting the Fourier coefficient with the calculated angles into the 2-level line voltage Fourier expression gives:

$$V_{RY}(\omega t) = \frac{4}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\left(-1+2\cos(n\alpha_1)-2\cos(n\alpha_2)+2\cos(n\alpha_3)\right)\left[\sin n(\omega t)-\sin n\left(\omega t-\frac{2\pi}{3}\right)\right]$$

(5.31)

Therefore, the individual harmonic magnitudes and resultant total harmonic voltage distortion can be calculated. Table 5.4 shows comparative analysis of the spectrum from the 3-level SHEM output line voltage waveform and the 2-level SHEM output line voltage waveform with the 5^{th}, 7^{th} and 11^{th} harmonics eliminated.

Harmonic Number	2-level SHEM (3 angles)	3-level SHEM (3 angles)
b_1	100	100
b_5	0	0
b_7	0	0
b_{11}	0	0
b_{13}	10.549	7.64
b_{17}	29.304	12.60
b_{19}	25.173	3.38
b_{23}	3.312	12.3
b_{25}	0.337	9.01
b_{29}	12.488	4.58
THDv%	46.588	9.394

Table 5.4 – Harmonic content % and THDv % for the 2-level SHEM line voltage and 3-level SHEM line voltage waveforms

Observation of table illustrates the possibility of recovering the low-order harmonic performance by eliminating the 5^{th}, 7^{th} and 11^{th} harmonic components. As predicted this again results in increased magnitudes of the higher frequency harmonic components.

5.5 SUMMARY OF HARMONIC ANALYSIS AND PERFORMANCE RECOVERY

The harmonic analysis presented throughout this Chapter has illustrated that throughout abnormal operating conditions, if the topology and controller revert to a 2-level structure and a bi-polar modulation scheme, the eliminated low-order harmonic spectrum of a 3-level topology can be recovered.

The initial fundamental frequency modulation (FFM) analysis of the 3-level VSI illustrates the potential for the DCMLI topology to be utilised for high-power applications. However, to meet harmonic requirements the 3-level FFM VSI would have to be implemented within a multiple-bridge arrangement. The 2-level FFM analysis shows that under abnormal operating conditions whilst maintaining continual operation the harmonic performance of the system would have to be temporarily sacrificed.

For stand-alone implementation of the 3-level VSI, various authors have proposed the SHEM technique as a viable option for high power applications. Under normal operating conditions a 3-level SHEM technique to eliminate the 5^{th}, 7^{th} and 11^{th} harmonic components is analysed. For abnormal operating conditions a 2-level SHEM strategy is presented in order to recover the low-order harmonic elimination. Simulation results of the 'ideal' 3-level and 2-level SHEM line voltages together with the resultant Fourier spectra are given in Figures 5.6 and 5.7, respectively. The spectra illustrate the recovered low-order harmonic performance at some expense of the higher order harmonic components. The remaining high-frequency harmonic components may be dealt with easier than requiring large low frequency filters or a system shutdown due to inadequate harmonic performance. Appendix B discusses further work on higher topologies.

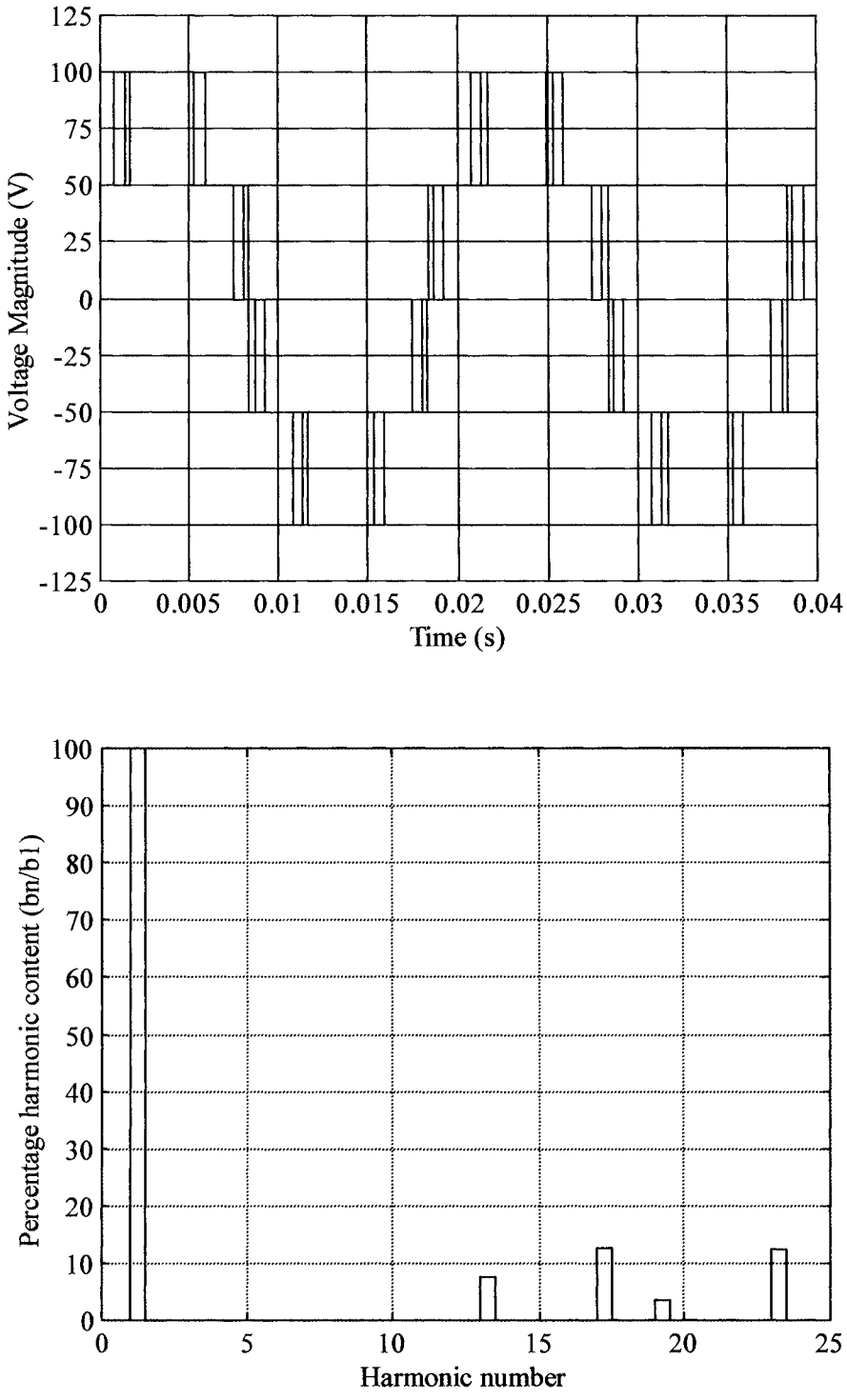


Figure 5.6 – 'Ideal' 3-level SHEM line voltage and Fourier Spectrum

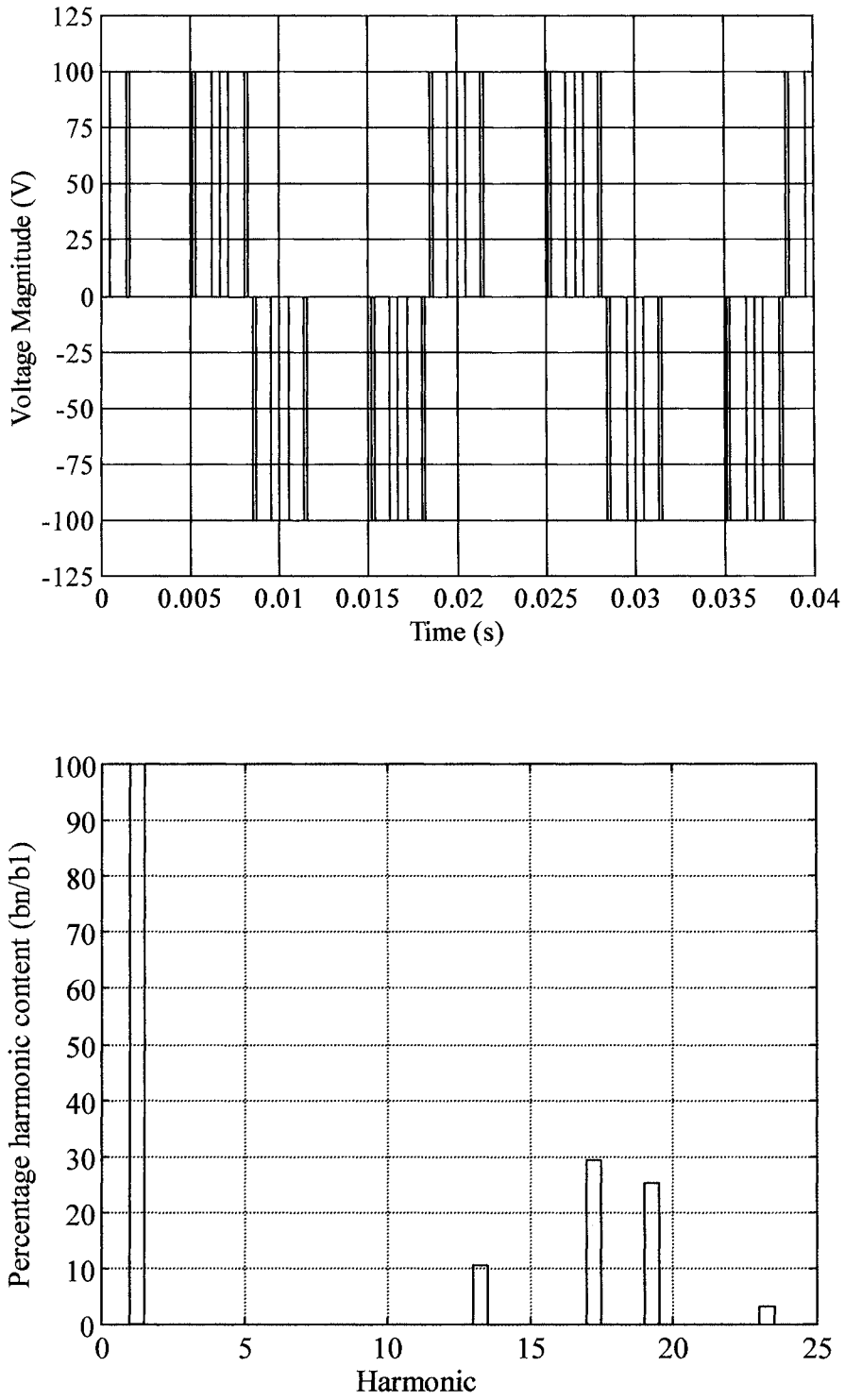


Figure 5.7 – 'Ideal' Two-level SHEM line voltage and Fourier Spectrum

6 PROPOSAL OF A NEW ADAPTIVE DISCHARGE PATH PROTECTION SWITCH CLAMPED (DPPSC) MULTI-LEVEL VSI

6.1 INTRODUCTION

The results of the space vector nodal analysis on the inherent operational redundancy of the multi-level VSI structure, described in Chapter 4 illustrate the requirement for an adaptive fault tolerant topology. The fact that redundancy is only available for certain devices under specified fault conditions leaves the system with limited options under abnormal operating conditions. This results in the generous provision of series device back-up redundancy.

To increase the options available under fault conditions, a new adaptive multi-level VSI scheme is proposed. This Chapter first presents the proposed adaptive multi-level power circuit structure suitable to any 'N'-level system. The associated adaptive switching control strategy is then illustrated for a 3-level adaptive topology under normal and abnormal operating conditions. The structural properties of the proposed VSI topology are investigated to determine its suitability for the high-power ASVC application. Also, the effects of the adaptive controller upon the overall switching losses of the topology are presented. The Chapter is concluded with simulations of the adaptive VSI topology based ASVC under normal and abnormal operating conditions.

6.2 THE ADAPTIVE 'N'-LEVEL DPPSC-MLI TOPOLOGY

In this research, a 'new' adaptive discharge path protection switch (DPPS) scheme is proposed to improve the limited operational redundancy of the diode-clamped multi-level VSI topology. The proposed adaptive DPPS scheme prevents, where possible, the development of a d.c. bus short-circuit path so that continual operation of the multi-level system is possible. The DPPS scheme can be

implemented into all diode-clamped multi-level topologies, odd and even, as illustrated for a generic phase 'N'-level VSI topology in Figure 6.1.

The proposed adaptive VSI topology replaces the clamp-diodes of the standard DCMLI topology scheme with controllable devices, which in the 'on' state have identical (forward bias) characteristics to the clamp diodes. These discharge path protection switches (DPPS) increase the robustness of the inverter system by enabling the adaptive control scheme to protect against system shutdown, under abnormal device fault conditions, using two methodologies:

1. Sequential activation of the DPPS devices throughout the control scheme to maintain the optimal uninterrupted performance of the system during abnormal short-circuit switching device faults.

2. Disable the DPPS devices corresponding to the 'lost' switching-states and revert to a lower multi-level VSI topology control strategy. This is adopted with particular device failure (e.g. d.c. rail devices) when it is not possible to protect the system by the sequential DPPS control scheme. As described in Chapter 5, the application of a raised frequency PWM technique will recover the optimal (normal operating conditions) harmonic spectrum and performance.

Details of the two methodologies are given in section 6.2.2.2. A major advantage of the new adaptive topology is the possibility of optimal-level uninterrupted system performance in the event of central device short-circuit failure, whereas with the conventional DCMLI structure the only option was device back up or shutdown. The sequential control for higher-level topologies (i.e. above 3-level) also presents the possibility of using the inherent redundancy of the structure or maintaining optimal-level performance in the event of intermediate level device short-circuit faults. For example, S_{R2} failing short-circuit on the 6-level structure now has two options, revert to a 4-level operation or maintain 6-level operation with sequential DPPS control. The 6-level operational redundancy is provided in the DPPSC-MLI in such a way that the difficulty for equal voltage sharing between series devices is avoided. The DPPSC-MLI scheme is presented as a

possibility to reduce the probability of system shutdown, in the event of short-circuit switching-device faults. Therefore reducing the number, and necessity, of series connected back-up devices and the associated control hardware required for this traditional minimisation of shutdown resulting from power circuit device faults.

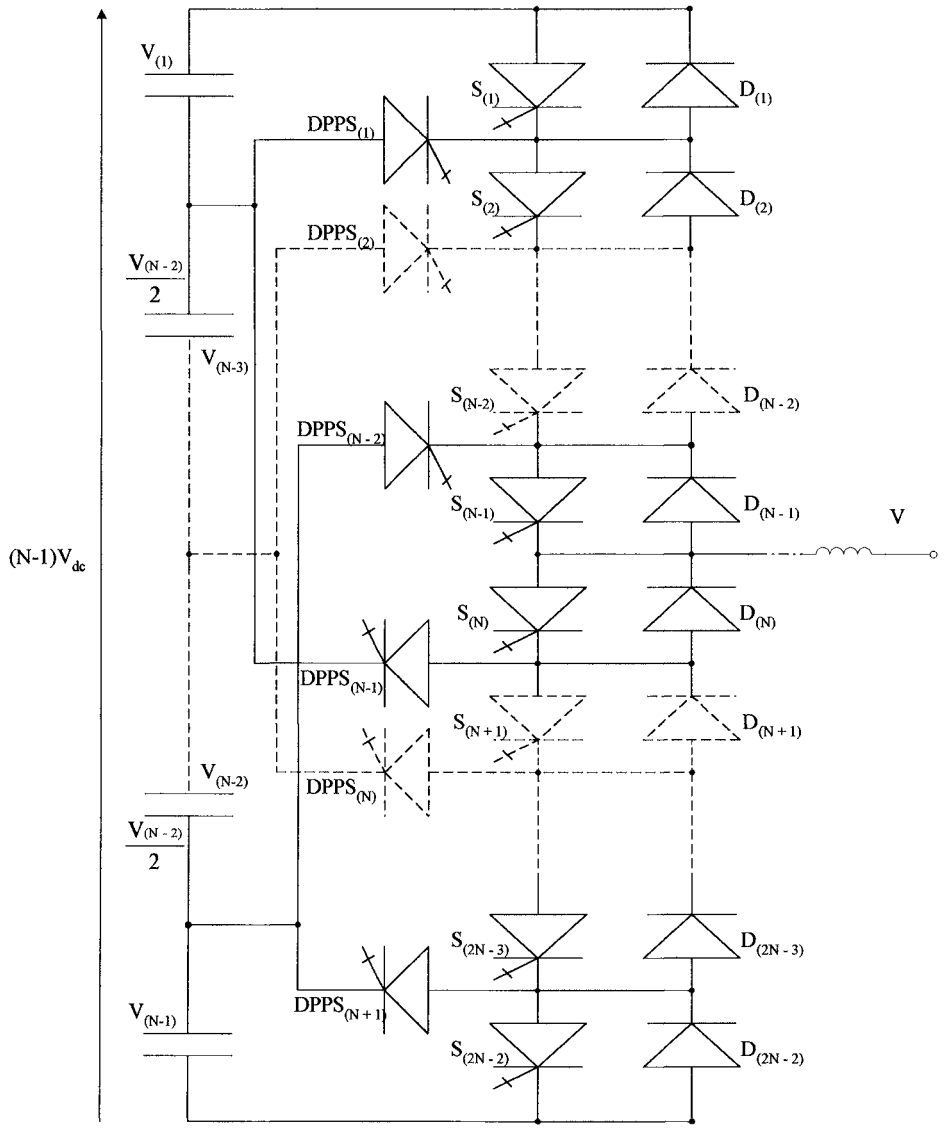


Figure 6.1 – Phase of a generic 'N'-level DPPSC-MLI structure

6.2.1 THE 3-LEVEL DPPSC-MLI TOPOLOGY

To demonstrate the improvement in inherent redundancy and operational robustness, compared to a conventional DCMLI topology, a 3-level DPPSC-MLI power circuit structure is investigated. As with the previous redundancy analysis, a single phase-limb of the DPPSC inverter structure (shown in Figure 6.2) is investigated.

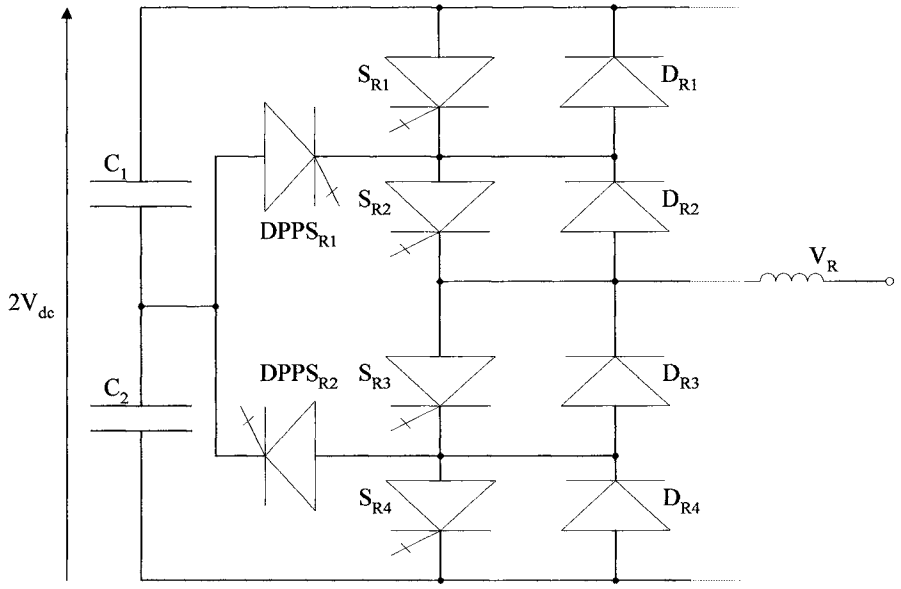


Figure 6.2 – Phase-limb of adaptive 3-level DPPSC-MLI

The 3-level inverter employing the new adaptive DPPSC topology and the basic control methodologies, presented in section 6.2.2, has been analysed for operational redundancy. The results of the 'lost' switching-state analysis, with respect to short-circuit device faults are shown in Table 6.1. Comparative analysis, of the conventional and the adaptive VSI topologies, illustrates that for short-circuit faults to the central devices (S_{R2} or S_{R3}) an optimal performance is possible using the proposed adaptive strategy, whereas the standard topology (using clamp diodes instead of DPPS devices) would result in a system shutdown. Therefore, the control restrictions for the standard 3-level DCMLI are averted for S_{R2} or S_{R3} faults, as the sequential DPPS scheme will maintain the optimum operation.

Short-circuit failure of S_{R1} and S_{R4} results in the loss of the 'zero' (0XX) states as with the standard topology. In such cases, the proposed adaptive controller is used to implement methodology (2) to recover the system harmonic performance. In the event of either of the DPPS devices failing short-circuit there is no effect upon the topology, as the DPPS device will normally have a series diode to ensure reverse voltage blocking capabilities. This will be further discussed in section 6.3 with the structural properties of the DPPSC-MLI topology. It should be noted however that this fault event would result in the DPPSC-MLI topology reverting back to a DCMLI topology with limited inherent redundancy to further device faults.

Device failed	**Number of states lost**	**Number of active vectors lost**	**Lost states of form**
S_{R1} or S_{R4}	9	2	(0XX)
S_{R2} or S_{R3}	0	0	N/A
$DPPS_{R1}$or $DPPS_{R2}$	0	0	N/A

Table 6.1 - States lost due to short-circuit devices on DPPSC-MLI topology

An open-circuit device fault investigation of the proposed DPPSC-MLI topology shows, as predicted, results identical to the standard topology analysis summarised in Table 4.4, i.e. inoperable system. The improved robustness of the adaptive 3-level DPPSC multi-level inverter over the conventional 3-level DCMLI is illustrated in the flow diagram shown in Figure 6.3.

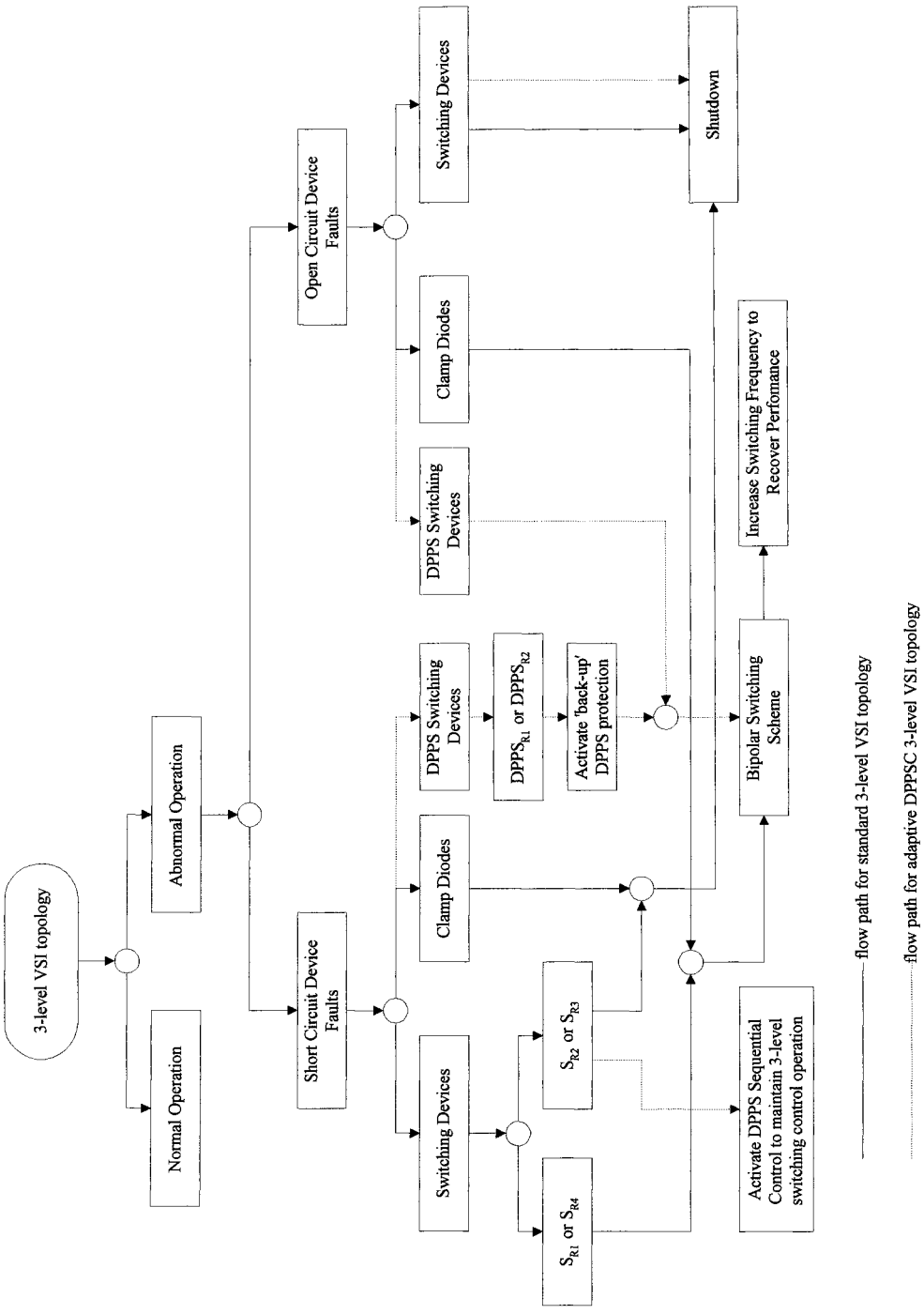


Figure 6.3 – 3-level VSI topology fault flow diagram

6.2.2 THE 3-LEVEL ADAPTIVE DPPS CONTROL STRATEGY

The adaptive DPPSC-MLI topology, which encompasses the multi-level power circuit and the adaptive controller, is proposed as suitable for any high power application requiring a robust voltage source inverter. As this project focuses upon the converter performance of the high power ASVC application, the proposed adaptive VSI topology is also suitable for drive applications or high voltage direct current (HVDC) transmission.

Typically, with VSI applications the system controller comprises an inner (open) loop control strategy, which provides the PWM scheme, and an outer (closed) loop control strategy, which provides the dynamic response required for the application. With the ASVC application the closed loop control would provide dynamic control of the reactive power compensation. Whereas the open loop control, which is equally as important to the overall system performance, provides the required VSI switching PWM pattern and maintains the characteristic operation of the ASVC according to the closed loop control requirements. Therefore the proposed adaptive DPPS control scheme is fundamentally an open loop switching controller. As such, an 'open loop' control strategy is presented in this research work. The adaptive switching controller for the 3-level DPPS VSI topology has three main objectives:

1. For normal operating conditions provide and maintain an acceptable system performance.

2. For short-circuit fault conditions to central switching devices (S_{R2} or S_{R3}), maintain continual 3-level operation through sequential activation of the DPPS control scheme. (Adaptive Control Methodology 1)

3. For short-circuit faults to the d.c. rail devices (S_{R1} or S_{R4}), provide an acceptable harmonic performance from the inherent redundancy operation of the inverter, utilising a low frequency switching strategy suitable for high power applications. (Adaptive Control Methodology 2)

The following sections present possible adaptive DPPS switching control schemes to enable continual operation of the 3-level DPPSC-MLI topology with suitable harmonic performance during normal and abnormal operating conditions.

6.2.2.1 NORMAL OPERATION CONTROL SCHEME

The normal operation control scheme to be utilised throughout this project for a 3-level VSI is a low-frequency SHEM strategy. As presented in Chapter 5, the 3-level (Red) phase voltage waveform illustrated in Figure 6.4 will be free of the 5^{th}, 7^{th} and 11^{th} harmonics if the correct switching angles are applied through the controller.

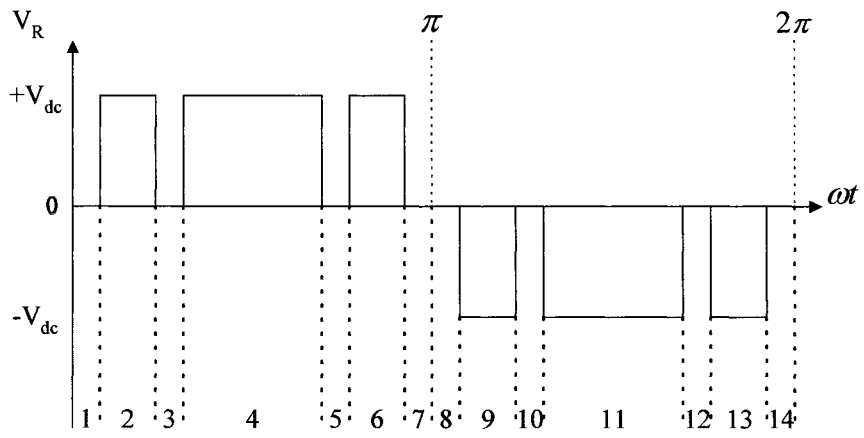


Figure 6.4 – SHEM 'sections' of a 3-level output phase voltage

It should be noted that the switching strategy adopted should exhibit 120° phase-shift symmetry between the three phases of the inverter to provide a balanced 3-phase output. The switching strategy for a complete cycle of the red (R) phase voltage waveform shown in Figure 6.4 is illustrated in Table 6.2. The cycle is subdivided into sections to illustrate the operational devices providing voltage levels at any one time throughout the waveform. As the VSI is operating under normal conditions the DPPS devices remain 'activated' (closed) thereby the topology exhibits identical operation to a conventional 3-level DCMLI topology.

SHEM Section	Switching State (1=on, 0=off)						Output
	S_{R1}	S_{R2}	S_{R3}	S_{R4}	$DPPS_{R1}$	$DPPS_{R2}$	V_{R0}
1	0	1	1	0	1	1	**0**
2	1	1	0	0	1	1	$+V_{dc}$
3	0	1	1	0	1	1	**0**
4	1	1	0	0	1	1	$+V_{dc}$
5	0	1	1	0	1	1	**0**
6	1	1	0	0	1	1	$+V_{dc}$
7	0	1	1	0	1	1	**0**
8	0	1	1	0	1	1	**0**
9	0	0	1	1	1	1	$-V_{dc}$
10	0	1	1	0	1	1	**0**
11	0	0	1	1	1	1	$-V_{dc}$
12	0	1	1	0	1	1	**0**
13	0	0	1	1	1	1	$-V_{dc}$
14	0	1	1	0	1	1	**0**

Table 6.2 – Normal operation 3-level SHEM switching strategy

6.2.2.2 ABNORMAL OPERATION CONTROL SCHEME

Under device fault conditions the open loop controller must adapt into an alternative switching control strategy to maintain system performance. Dependent upon the positioning of the device within the phase-limb of the inverter, two alternative adaptive DPPS control methodologies are proposed.

ADAPTIVE CONTROL METHODOLOGY 1

In the event of the central switching devices (S_{R2} or S_{R3}) failing short-circuit a sequential DPPS control scheme is implemented. The objective of the switching controller is to prevent a capacitor discharge path whilst maintaining optimal system performance. That is, with a short-circuit fault to either S_{R2} or S_{R3}, the switching controller maintains 3-level operation.

A possible sequential DPPS control strategy for 3-level SHEM, with a short-circuit fault to device S_{R2}, is illustrated in Table 6.3. The short-circuit fault is indicated by the device (S_{R2}) remaining 'on' throughout the complete cycle of the switching strategy. Observation of the switching column for $DPPS_{R1}$ illustrates the preventive discharge path control. Redundancy analysis of the conventional 3-level VSI illustrates the 'loss' of states (-1XX) with a short-circuit fault on device S_{R2}. Therefore, the sequential DPPS control de-activates (turns-off) the corresponding device ($DPPS_{R1}$) to 'open' the discharge loop and enable 'recovery' of the 'lost' switching states.

Device switching during the sequential activation period is of utmost importance. Table 6.3.1 illustrates an expanded 'window' of SHEM sections 10 to 12. As shown the de-activation (turn-off) and activation (turn-on) of the DPPS device is controlled to operate within the 'dead-band' region of the normal switching control. Dead-band regions are always implemented into PWM switching strategies as a protective means to prevent 'd.c. shoot-through' which basically means short-circuit between the d.c. rails.

SHEM Section	Switching State (1=on, 0=off)						Output
	S_{R1}	S_{R2}	S_{R3}	S_{R4}	$DPPS_{R1}$	$DPPS_{R2}$	V_{R0}
1	0	1	1	0	1	1	**0**
2	1	1	0	0	1	1	**$+V_{dc}$**
3	0	1	1	0	1	1	**0**
4	1	1	0	0	1	1	**$+V_{dc}$**
5	0	1	1	0	1	1	**0**
6	1	1	0	0	1	1	**$+V_{dc}$**
7	0	1	1	0	1	1	**0**
8	0	1	1	0	1	1	**0**
9	0	1	1	1	0	1	**$-V_{dc}$**
10	0	1	1	0	1	1	**0**
11	0	1	1	1	0	1	**$-V_{dc}$**
12	0	1	1	0	1	1	**0**
13	0	1	1	1	0	1	**$-V_{dc}$**
14	0	1	1	0	1	1	**0**

Table 6.3 – Abnormal operation 3-level SHEM switching strategy - S_{R2} short-circuit – sequential DPPS operation

SHEM Section	Switching State (1=on, 0=off)						Output
	S_{R1}	S_{R2}	S_{R3}	S_{R4}	$DPPS_{R1}$	$DPPS_{R2}$	V_{R0}
10	0	1	1	0	1	1	**0**
10-11	0	1	1	0	0	1	**0**
11	0	1	1	1	0	1	**$-V_{dc}$**
11-12	0	1	1	0	0	1	**0**
12	0	1	1	0	1	1	**0**

Table 6.3.1 – S_{R2} short-circuit – Sequential 'dead-band' DPPS operation

Table 6.4 illustrates a possible sequential DPPS control strategy with a short-circuit fault to device S_{R3}. As with the previously presented case, the DPPS device prevents capacitor discharge paths by de-activating and hence breaking the potential loop. In the event of S_{R3} failing short-circuit device $DPPS_{R2}$ 'recovers' the 'lost' (1XX) states; therefore, maintaining uninterrupted 3-level SHEM system performance.

Again the sequential operation of the DPPS device is of utmost importance and the prevention of discharge paths, whilst also maintaining the correct 'paths' for the uninterrupted switching scheme, is provided by turning the device 'off' and 'on' within the 'dead-band' region of S_{R3}.

SHEM	**Switching State (1=on, 0=off)**						**Output**
Section	S_{R1}	S_{R2}	S_{R3}	S_{R4}	$DPPS_{R1}$	$DPPS_{R2}$	V_{R0}
1	0	1	1	0	1	1	**0**
2	1	1	1	0	1	0	$+V_{dc}$
3	0	1	1	0	1	1	**0**
4	1	1	1	0	1	0	$+V_{dc}$
5	0	1	1	0	1	1	**0**
6	1	1	1	0	1	0	$+V_{dc}$
7	0	1	1	0	1	1	**0**
8	0	1	1	0	1	1	**0**
9	0	0	1	1	1	1	$-V_{dc}$
10	0	1	1	0	1	1	**0**
11	0	0	1	1	1	1	$-V_{dc}$
12	0	1	1	0	1	1	**0**
13	0	0	1	1	1	1	$-V_{dc}$
14	0	1	1	0	1	1	**0**

Table 6.4 – Abnormal operation 3-level SHEM switching strategy - S_{R3} short-circuit – sequential DPPS operation

ADAPTIVE CONTROL METHODOLOGY 2

In the event of phase-limb d.c. rail devices (S_{R1} and S_{R4}) failing short-circuit, the sequential DPPS control scheme cannot maintain optimal system performance due to device structural positioning. Therefore, the adaptive control methodology 2 is implemented whereby the VSI 'reverts' to a lower level topology and the harmonic performance is recovered by implementing a slightly higher switching frequency modulation scheme.

The redundancy analysis presented in Chapter 4 indicates the inherent redundancy of a bi-polar operation in the event of S_{R1} or S_{R4} failing short-circuit. Also, the harmonic analysis presented in Chapter 5 illustrates the possibility of low-order harmonic recovery through implementation of a bi-polar SHEM strategy. Therefore, this adaptive harmonic recovery technique will be utilised to demonstrate the possibility of continual performance at a lower level of operation.

Harmonic analysis of the 2-level SHEM waveform presented in Chapter 5 illustrates that elimination of the 5^{th}, 7^{th} and 11^{th} harmonics can be obtained through a bi-polar strategy, whilst maintaining a low switching frequency. Implementation of the bi-polar SHEM waveform, given in Figure 6.5, to the adaptive control scheme will offer the possibility of continual system operation with minimum low-order harmonics performance, if the correct pulse angles are applied through the switching controller.

As a short-circuit fault event to devices S_{R1} or S_{R4} will result in identical adaptive control methodologies, only the S_{R1} case is demonstrated. In both cases the (0XX) switching-states are 'lost'. Therefore, there is no requirement for a 'zero' clamp path. In the event of either device failing short-circuit, both $DPPS_{R1}$ and $DPPS_{R2}$ are de-activated to open the unnecessary clamp path and reduce power losses associated with the devices. The switching strategy for the red (R) phase to synthesise the 2-level SHEM voltage waveform shown above is illustrated in Table 6.5.

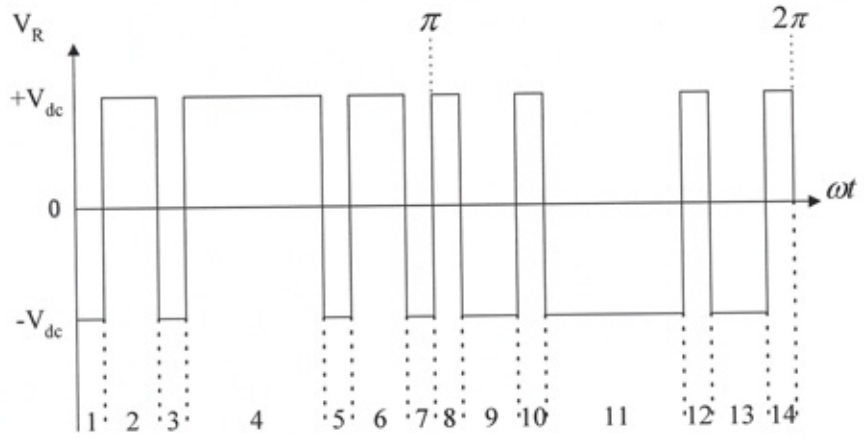


Figure 6.5 – SHEM 'sections' of a 2-level output phase voltage

SHEM Section	Switching State (1=on, 0=off)						Output
	S_{R1}	S_{R2}	S_{R3}	S_{R4}	$DPPS_{R1}$	$DPPS_{R2}$	V_{R0}
1	1	0	1	1	0	0	$-V_{dc}$
2	1	1	0	0	0	0	$+V_{dc}$
3	1	0	1	1	0	0	$-V_{dc}$
4	1	1	0	0	0	0	$+V_{dc}$
5	1	0	1	1	0	0	$-V_{dc}$
6	1	1	0	0	0	0	$+V_{dc}$
7	1	0	1	1	0	0	$-V_{dc}$
8	1	1	0	0	0	0	$+V_{dc}$
9	1	0	1	1	0	0	$-V_{dc}$
10	1	1	0	0	0	0	$+V_{dc}$
11	1	0	1	1	0	0	$-V_{dc}$
12	1	1	0	0	0	0	$+V_{dc}$
13	1	0	1	1	0	0	$-V_{dc}$
14	1	1	0	0	0	0	$+V_{dc}$

Table 6.5 – Abnormal operation 3-level SHEM switching strategy

- S_{R1} or S_{R4} short-circuit – bi-polar SHEM strategy

6.3 STRUCTURAL PROPERTIES OF THE DPPSC-MLI TOPOLOGY

In proposing a new adaptive VSI topology it is essential to investigate the structural characteristic properties of the inverter phase-limbs. As presented earlier, the overall continual performance can be maintained with adaptive control schemes and protective DPPS devices. However, in the event of a short-circuit fault there will be additional voltage stresses associated with the continual operation that must be acceptable for the topology to be suitable for industrial applications. Therefore, the device voltage stresses during normal and abnormal operation must be considered.

During normal operation, voltage stress on each switching device in a clamped multi-level structure is given as [45]:

$$V_{SW.D.} = \frac{V_{dc(total)}}{N_{levels} - 1} \tag{6.1}$$

Therefore, if the total d.c. voltage is considered as 1 p.u., for the 3-level DDPSC-MLI structure each device must withstand 0.5 p.u. of the total d.c. bus voltage.

Also, in a conventional DCMLI topology, each clamp-diode will see reverse voltage stress of [45]:

$$V_{CD} = \left\{ \frac{N_{levels} - 1 - k}{N_{levels} - 1} \right\} \times V_{dc(total)} \tag{6.2}$$

Where k ranges from 1 to ($N_{levels} - 2$) dependant upon the clamp-diode positioning and level of the structure.

Therefore, for the 3-level DCMLI structure each clamp-diode will have a reverse voltage stress of 0.5 p.u. of the total d.c. bus voltage. However, as the multi-level structure increases in levels the highest voltage stresses seen by outer-positioned clamp-diodes can be almost full V_{dc}. It should be noted that the voltage stresses

for each pair of clamp diodes throughout a multi-level structure will summate to 1 p.u. V_{dc}. In the proposed DPPSC-MLI structure, the conventional clamp-diodes are replaced with controllable switching devices. The equation illustrating the requirement for reverse voltage stress on the clamp-diodes immediately causes concern. This is resultant from the fact that power diodes normally exhibit reverse voltage blocking capability, whereas a typical power switching device usually has a very low reverse voltage blocking capability. For the DPPSC-MLI topology to be implemented with standard IGBT devices, as will be utilised in the laboratory model, the structure will require series-connected diodes with the DPPS devices in the clamp path. Therefore, the requirement for reverse blocking capabilities will be maintained. This will be further discussed in Chapter 7 where the construction of the 3-level DPPSC-MLI laboratory model is presented.

Under abnormal operating conditions, the voltage stresses upon the switching devices have the potential to increase dependant upon the current switching state of the inverter. Device short-circuit analysis has shown that the resultant voltage stress, across the remaining 'healthy' devices, is dependant upon the phase limb positioning of the faulty device and the number of levels (N) of the inverter. To illustrate this analysis, the 3-level and 6-level VSI topology results are presented.

Initially considering the 3-level structure. In both adaptive control methodologies the switching device in the same phase-limb polarity as the faulty device (i.e. S_{R1} and S_{R2}) will have an increase in voltage stress under certain switching state conditions. For example, if S_{R1} fails short-circuit and the topology reverts to a 2-level switching strategy then device S_{R2} will have twice the normal voltage stress (1 p.u. V_{dc}) applied to it throughout switching states (-1XX). Also, in the event of S_{R2} failing short-circuit and the adaptive DPPS control maintaining a 3-level switching strategy, the device S_{R1} will have to block 1 p.u. V_{dc} applied to it through switching states (0XX) and (-1XX).

Therefore, prior to implementation of the adaptive 3-level scheme, an operational power study must be performed to ensure rating suitability of the devices to be utilised within the adaptive power circuit. Although it is typical for an inverter operating level to be much less than the switching device rating, in a worst case

scenario the reactive power compensation level may have to be reduced for abnormal operating conditions. However, this is still foreseen as advantageous to the options available to the standard DCMLI topology. In the event of a device fault to the conventional structure, the only methodology to prevent complete loss of reactive compensation (due to system shutdown) is the implementation of redundant series connected back-up devices. As presented previously, this technique exhibits the possibility of voltage sharing problems, contradicts the objectives of implementing multi-level VSI topologies and adds additional costs to the overall power circuit and associated control peripherals.

Analysis of the adaptive 6-level VSI topology illustrates that the increase in device voltage stresses throughout abnormal operating conditions is proportionally less as the number of levels increase. This is due to the inherent structure of the power circuit and the effective voltage divisional properties of the topology. Under normal operating conditions the maximum possible voltage stress across devices in the 6-level phase limb can be calculated from equation (6.1) as 0.2 p.u. of the total V_{dc}. For abnormal fault conditions, if an adaptive control scheme is applied to maintain continual operation, the maximum potential voltage stress is again double the normal operating condition requirements for devices positioned close to the d.c. rails. However, as the positioning of the phase limb devices moves more central and the switching state moves away from the faulty device the resultant voltage stress for abnormal operating conditions reduces.

For example, if S_{R1} fails short-circuit and the topology reverts to a 4-level switching strategy then the voltage stress across device S_{R2} will again double in the event of switching state (1XX). However, due to the reduced voltage blocking requirements of the 6-level structure, this now only equates to 0.4 p.u. V_{dc}. Also maintaining a fault on device S_{R1}, in the event of switching state (-3XX) being applied the voltage stress across devices $S_{R2} \rightarrow S_{R5}$ is only 0.25 p.u. V_{dc}. This is an increase of only 0.05 p.u. V_{dc} from the normal operating conditions.

In the event of S_{R4} failing short-circuit, an adaptive DPPS control scheme can be applied to maintain a 6-level switching strategy. If switching state (-2XX) is activated the resultant voltage stresses across devices $S_{R1} \rightarrow S_{R3}$ is 0.266 p.u. V_{dc}. Which equates to an increase of only 0.066 p.u. V_{dc} across each device. Table 6.6 illustrates the potential maximum voltage stress across each device in the upper half phase limb of the 6-level topology if operation is maintained throughout abnormal operating conditions.

Device Short-circuit	**Abnormal operation maximum total V_{dc} (p.u.) voltage stress upon remaining devices in phase limb**				
	S_{R1}	**S_{R2}**	**S_{R3}**	**S_{R4}**	**S_{R5}**
S_{R1}	N/A	0.4	0.3	0.266	0.25
S_{R2}	0.4	N/A	0.3	0.266	0.25
S_{R3}	0.3	0.3	N/A	0.266	0.25
S_{R4}	0.266	0.266	0.266	N/A	0.25
S_{R5}	0.25	0.25	0.25	0.25	N/A

Table 6.6 - Potential device voltage stresses for abnormal conditions

The 6-level analysis illustrates that although an operational power study should be performed to ensure suitability of the adaptive topology and controller, the resultant stresses under abnormal operating conditions effectively reduce as the topology level increases.

6.4 EFFECT OF ADAPTIVE SWITCHING CONTROL ON SWITCHING FREQUENCY

The ASVC application for the proposed adaptive DPPSC-MLI topology is typically high power, such as transmission or distribution level. It is therefore essential to maintain an acceptable switching frequency in the event of implementing a bi-polar SHEM harmonic recovery scheme under abnormal operating conditions. To reduce switching power losses, the switching frequency of the ASVC inverter is restricted to a few hundred Hertz (Hz). However, with the rapid development of IGBT's, GTO's and IGCT's it is foreseen that this restriction may be extended to 1 kHz.

For the adaptive bi-polar switching strategy to be suitable for the high power application, switching frequencies during normal and abnormal operation must be compared. The switching frequency for a pulse width modulated device is given as:

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}} \tag{6.3}$$

Where t_{ON} = time device is on throughout one period of switching

t_{OFF} = time device is off throughout one period of switching

Therefore, with a bi-polar fundamental frequency modulation strategy the switching frequency is $f_{SW} = 50$ Hz. For optimised SHEM switching strategies the switching frequency can be derived for the 2-level and 3-level from the number of switching angles (per quarter period) introduced to the waveform. The switching frequency for a 3-level SHEM operated VSI can be defined by [52]:

$$f_{3,SW} = j.f_1 \tag{6.4}$$

Where j denotes the number of switching angles (α) per quarter cycle and f_1 represents the fundamental frequency.

Therefore, for the normal operation 3-level SHEM strategy illustrated in Figure 6.4 the switching frequency is:

$$f_{3,SW} = 3 \times 50 = 150Hz \qquad (6.5)$$

The switching frequency for a 2-level SHEM operated VSI can be defined as [52]:

$$f_{2,SW} = (2.j + 1).f \qquad (6.6)$$

Therefore, for the proposed abnormal operation 2-level SHEM strategy illustrated in Figure 6.5, the switching frequency can be calculated as:

$$f_{2,SW} = ((2 \times 3) + 1) \times 50 = 350Hz \qquad (6.7)$$

This illustrates that the adaptive bi-polar control will result in an increase in switching frequency of 200 Hz. This will result in an increase in switching power losses in the remaining operational devices. This must be taken into account by, perhaps, restricting the maximum current during abnormal operation. Also, it may be worth pointing out that this will be partially counteracted by the non-operation of the faulty device plus the de-activation of the clamp path and their associated losses. In addition, in the event of device S_{R1} failing short-circuit there is no requirement to switch device S_{R4} as the bi-polar strategy can be implemented with devices S_{R2} and S_{R3} only. Therefore, the switching losses associated with device S_{R4} will be minimised to 'on' (conduction) losses, which are relatively low.

6.5 SIMULATION OF 3-LEVEL DPPSC-MLI BASED ASVC

Before constructing the experimental model of the proposed 3-level inverter topology, it is essential to validate the theoretical proposals with computer simulations of the circuit. Two forms of simulation are suitable for power system application analysis, mathematical modelling and numerical modelling. Typical mathematical modelling of the 3-level VSI topology gives system currents and d.c. voltages by solving simultaneous differential equations incorporating switching functions of the proposed PWM scheme [9]. This analysis method was not suitable for the implementation of an adaptive controller responding to particular device faults. Although not implemented for this initial operational analysis, mathematical modelling of the 3-level ASVC is derived and utilised for a.c.-d.c. harmonic interaction analysis in Chapter 9.

The utilisation of numerical modelling simulation packages with Graphical User Interface (GUI) was thought most suitable to investigate both normal and abnormal operation of the ASVC. The GUI simulation package used for the analysis of this application is the Simulink Power System Blockset (PSB), which is one of the Matlab Toolboxes. Utilising the PSB with the various Matlab analysis tools permits the user to visualise the power circuit and power network whilst programming the adaptive controller for the 3-level VSI in a CMEX file format. Therefore, the 3-level DPPSC-MLI based 3-phase ASVC was modelled using this simulation package. The developed Matlab/Simulink PSB models were used to study the steady-state performance of the ASVC in normal and abnormal operating conditions.

Operation of the 3-level DPPSC-MLI based ASVC in both leading and lagging modes of reactive power compensation has been carried out and is presented in the following sections of this Chapter.

6.5.1 THE ASVC DURING NORMAL OPERATION

Initial simulations were conducted to observe the normal operation of the ASVC in both modes of reactive power compensation. A representation of the power circuit and simple power system model constructed in the PSB GUI simulation package is shown in Figure 6.6. The SHEM switching controller for the 3-level DPPSC-MLI was programmed as a CMEX file which offers control and user interaction during simulation through an S-function block within Simulink [58].

By constructing an interactive 'mask' for the programmed switching controller the reactive power transfer between the ASVC and the power system could be controlled. By pre-setting of the phase angle between the inverter output voltages and the corresponding a.c. system voltages, the mode of operation and magnitude of reactive compensation could be manipulated. This programmed form of open loop switching controller is a simulated representation of the laboratory model DSP implementation with the phase angle being set by the user through a serial-link connected PC.

The ASVC output current harmonic distortion depends upon the ASVC output voltage and the value of the a.c. side inductance, which effectively acts as a harmonic attenuator. Assuming that the phase angle between the inverter fundamental output voltage and the a.c. system voltage is negligible, the r.m.s. value of the fundamental current can be found by:

$$\left|i_{(1)}\right| = \frac{\left|V_S\right| - \left|V_{ASVC(1)}\right|}{\omega . L} \tag{6.8}$$

Where (1) indicates fundamental quantity and V_S and V_{ASVC} are r.m.s. values. Therefore assuming an ideal supply voltage the nth harmonic current can be obtained by:

$$\left|i_{(n)}\right| = \frac{\left|V_{ASVC(n)}\right|}{\omega . L} \tag{6.9}$$

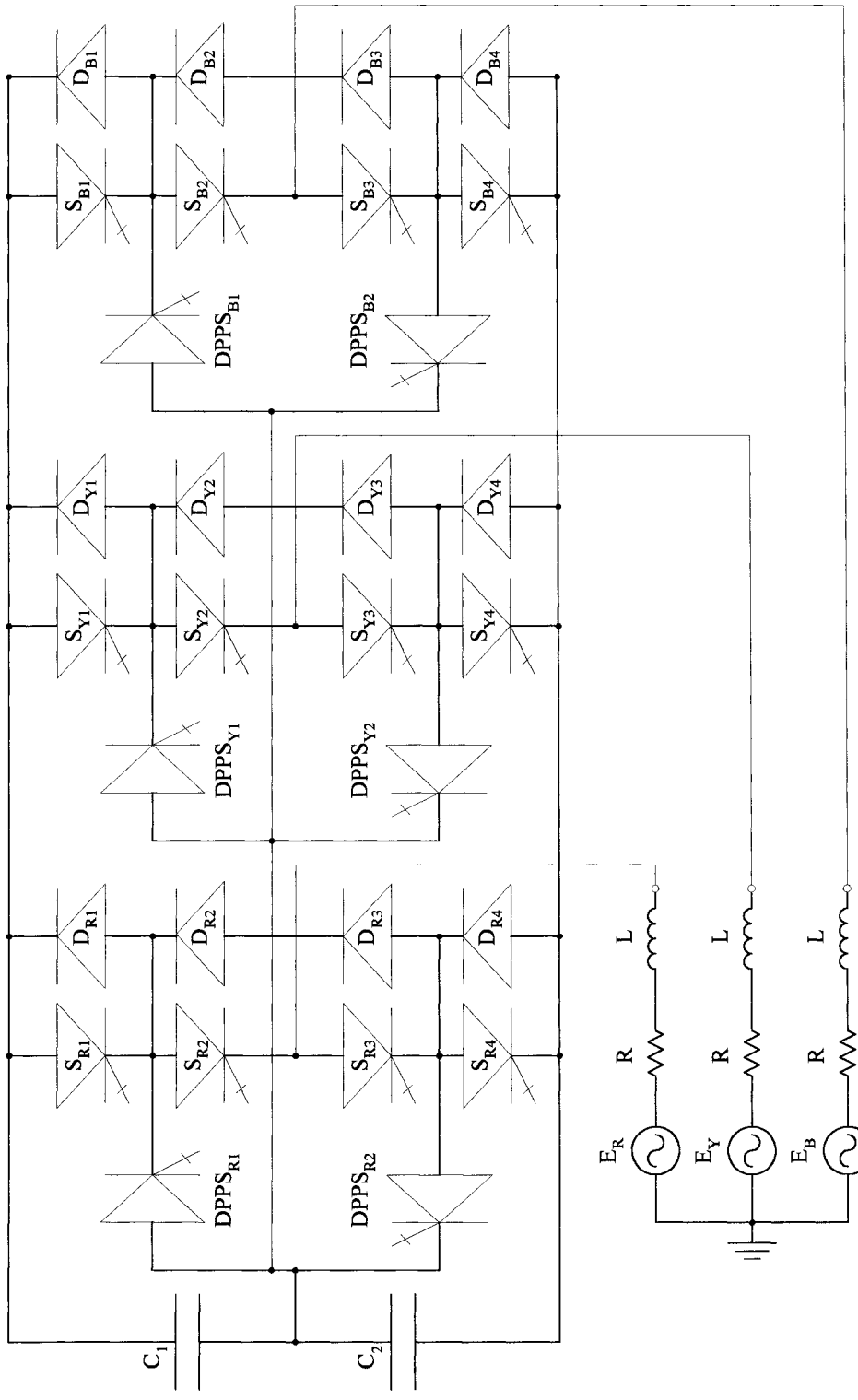


Figure 6.6 – Simulink PSB model for 3-level DPPSC-MLI based ASVC

Equations (6.8) and (6.9) illustrate the attenuating properties resulting from the interconnecting inductors associated with the VSI based ASVC.

For the simulation the following values were specified: V_S = 35 volts, C = 333 μF, R = 0.31 Ω and L = 10 mH. The value of capacitance was selected with regards to knowledge of suitably rated available capacitors for the laboratory model. Large value capacitors offer a reduced d.c. ripple but degrade the dynamic performance of the ASVC. As the purpose of these simulations is to observe the steady-state performance during normal and abnormal operation of the ASVC, not the dynamic response, this capacitor value was selected. Also, the analysis focuses upon the resultant current waveform from the 3-level SHEM not the possibility of re-modulation of harmonics, which will be further analysed in Chapter 9. The inductance and resistor values were selected to give a typical X/R ratio of 10.

The lagging mode of reactive power compensation for the ASVC was modelled by selecting a leading phase angle for the inverter output voltage with respect to the a.c. system voltage. This results in the capacitor d.c. voltage lowering such that the ASVC output voltage is less than the a.c. system voltage. The voltage and current waveforms for operation in the lagging mode are shown in Figure 6.7.

By selecting a small lagging phase angle for the inverter output voltage, with respect to the a.c. system voltage, the leading mode of reactive power compensation was obtained. This now results in the inverter a.c. output voltage rising above the a.c. system voltage and hence, generating reactive current as illustrated in the waveforms of Figure 6.8.

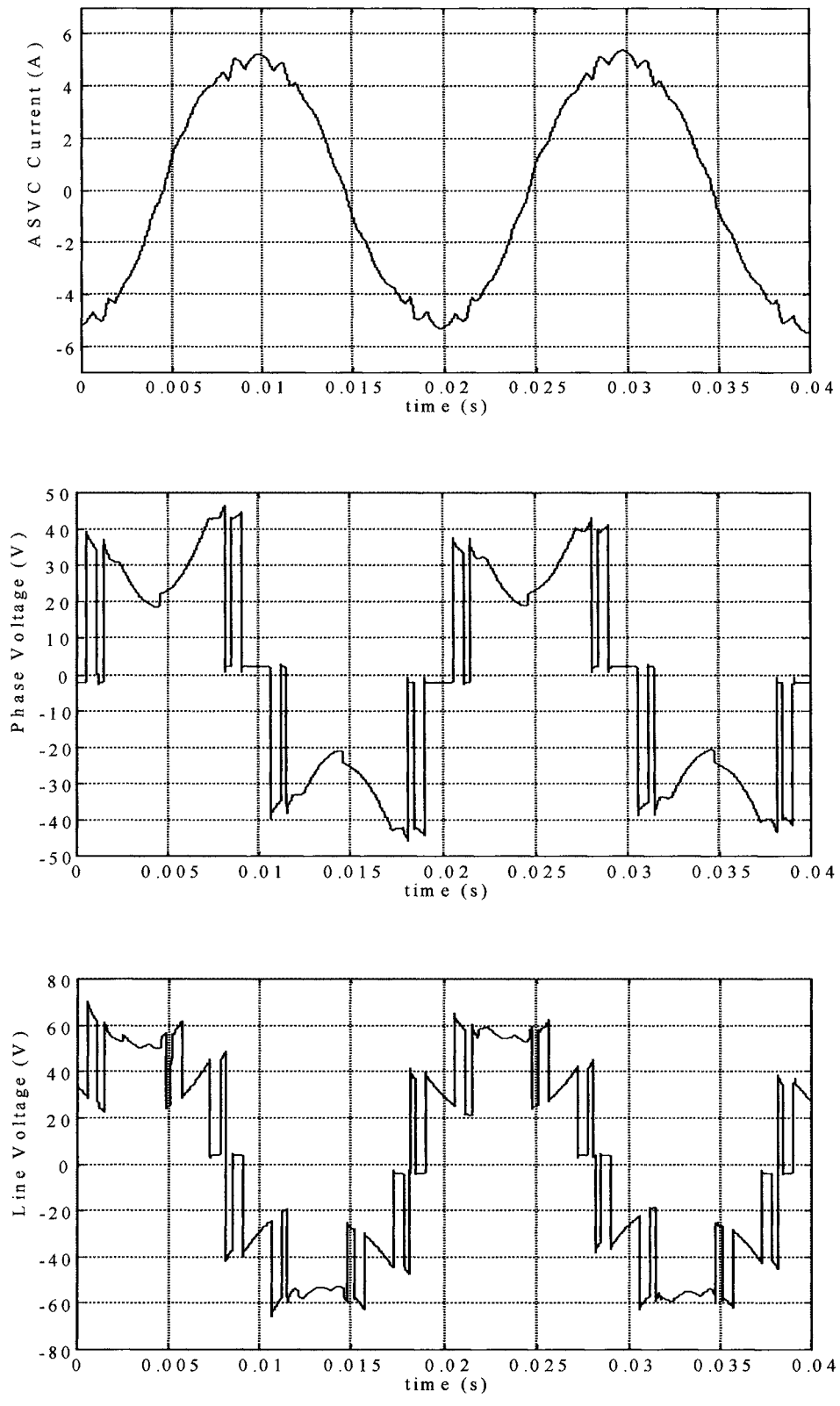


Figure 6.7 – Current and Voltage waveforms for a 3-level SHEM VSI based ASVC operating in the lagging mode.

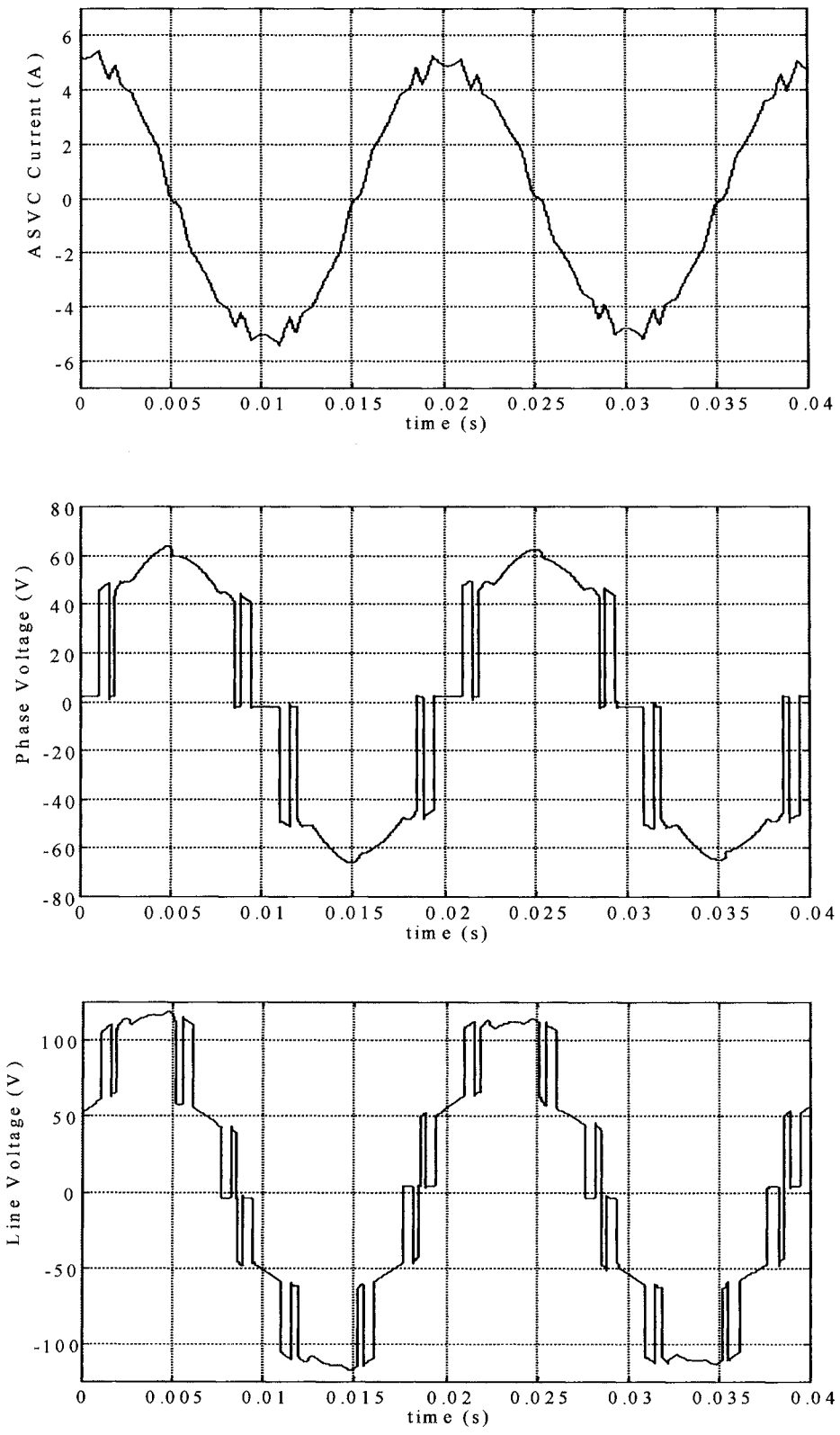


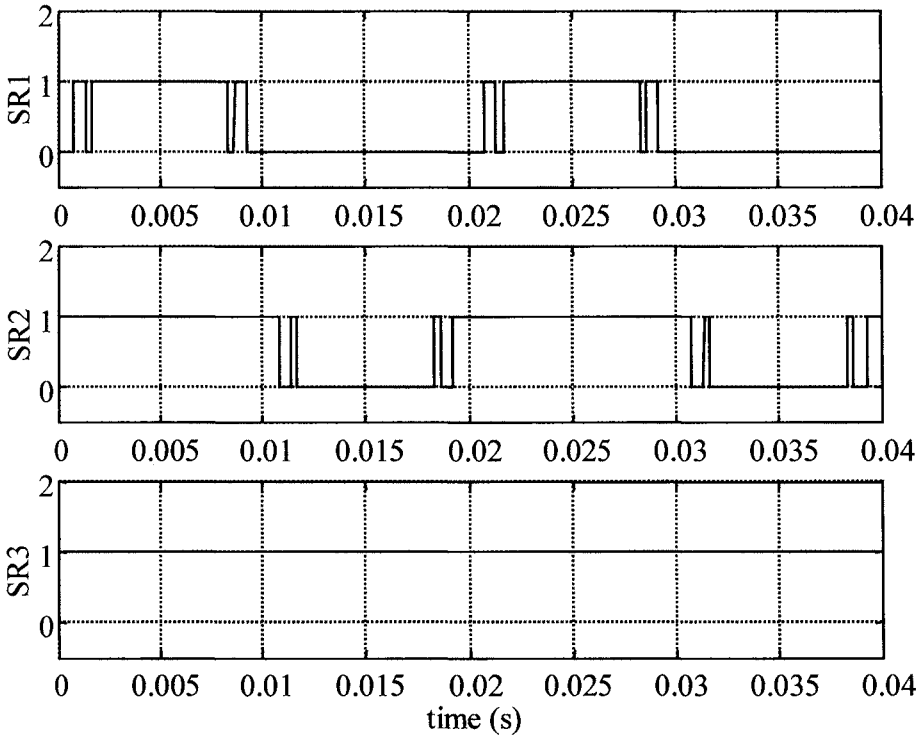
Figure 6.8 – Current and Voltage waveforms for a 3-level SHEM VSI based ASVC operating in the leading mode.

6.5.2 THE ASVC DURING ABNORMAL OPERATION

For the simulation of abnormal operation, the ASVC model is tested on either an uninterrupted 3-level SHEM VSI (adaptive control method 1) or a 2-level SHEM VSI performance (adaptive control method 2). The programmed 3-level SHEM switching controller was altered to provide the required sequential DPPS control or a 2-level SHEM strategy, depending on the type of abnormal condition. Fault detection was programmed into the overall controller to enable the user to simulate, through a GUI 'mask', short-circuits to specific devices at specified times.

As a fault to the central devices S_2 or S_3 in any limb would results in sequential DPPS control being implemented (to maintain optimal 3-level SHEM performance), the resultant current and voltage waveforms will be as presented for the normal operation in Figures 6.7 and 6.8. The sequential operation of the DPPS devices to prevent the discharge path is demonstrated in the waveforms shown in Figure 6.9. The waveforms illustrate two steady-state cycles of switching pulses to the devices in the red (R) phase. As shown, device S_{R3} has failed short-circuit and is therefore represented by the firing pulse being permanently 'on'. The firing pulses indicate how the sequential control of device $DPPS_{R2}$ maintains an uninterrupted 3-level SHEM strategy. It is illustrated by $DPPS_{R2}$ signal going low every time S_{R1} goes high, to prevent the creation of a short-circuit path.

Short-circuit faults to devices S_{R1} or S_{R4} results in the adaptive VSI topology reverting to a 2-level SHEM system to maintain continual operation with an acceptable harmonic performance. Using simulated faults and the conventional phase angle control of the inverter output voltages the ASVC was operated with a 2-level SHEM strategy implemented on the 'reverted' power circuit structure. The results for the lagging and leading modes of operation are shown in Figures 6.10 and 6.11, respectively. These results show that an 'acceptable' performance is maintained in terms of harmonic performance and characteristic operation of the ASVC.



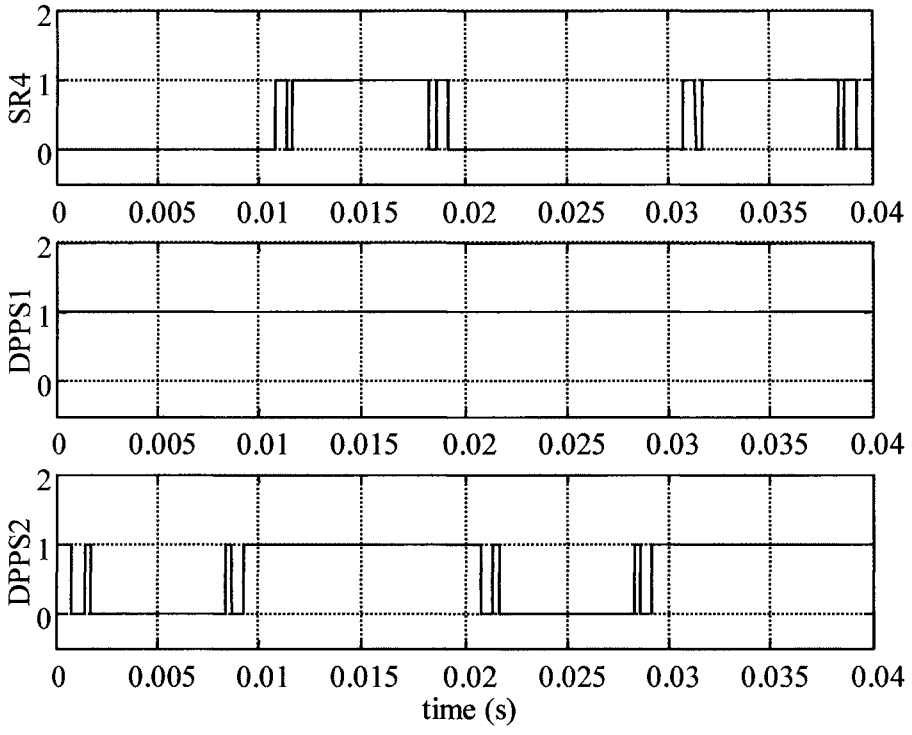


Figure 6.9 – Sequential DPPS firing pulses for S_{R3} short-circuit and $DPPS_{R2}$ preventing discharge path

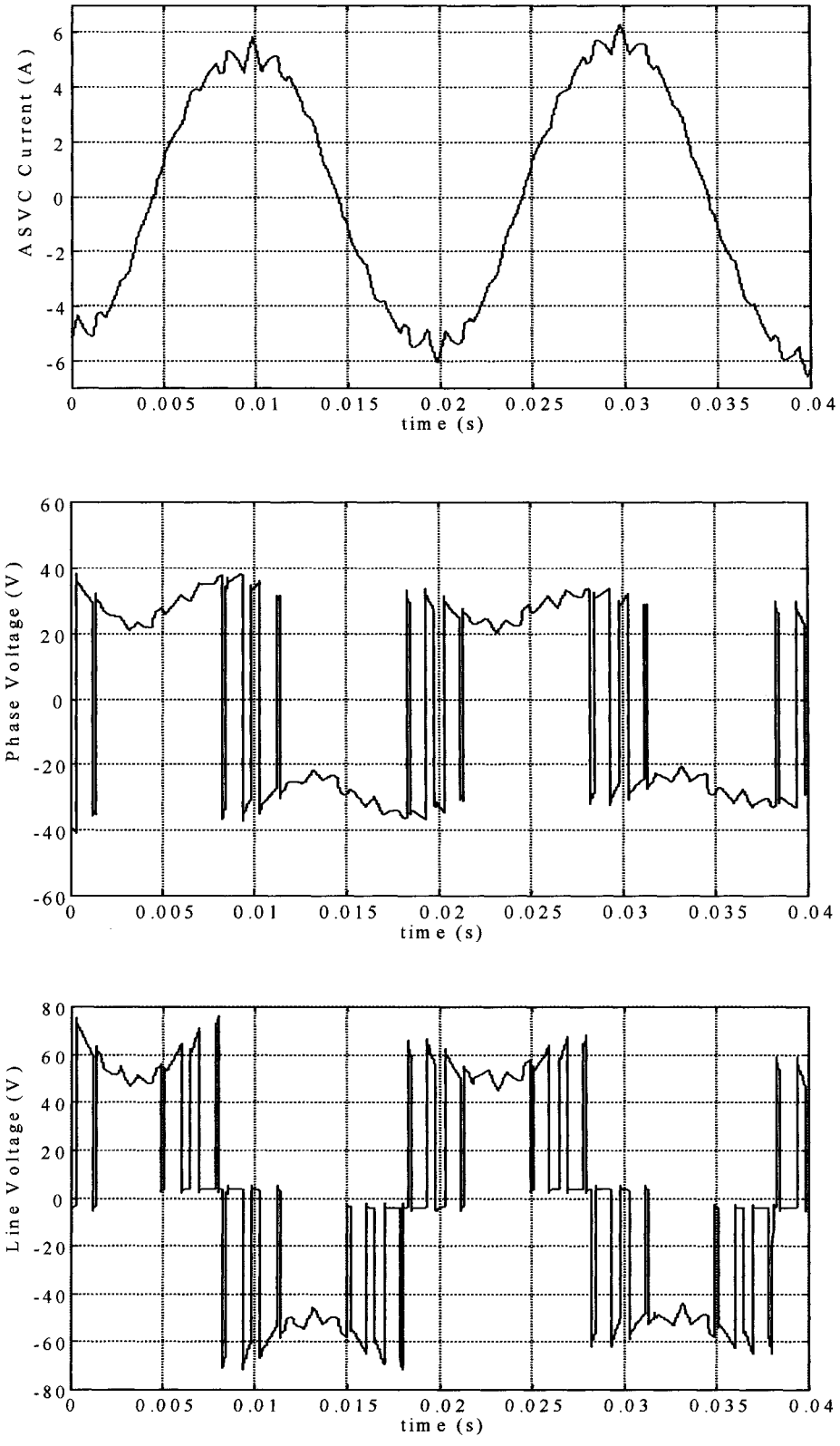


Figure 6.10 – Waveforms for a 2-level SHEM VSI based ASVC operating in the lagging mode.

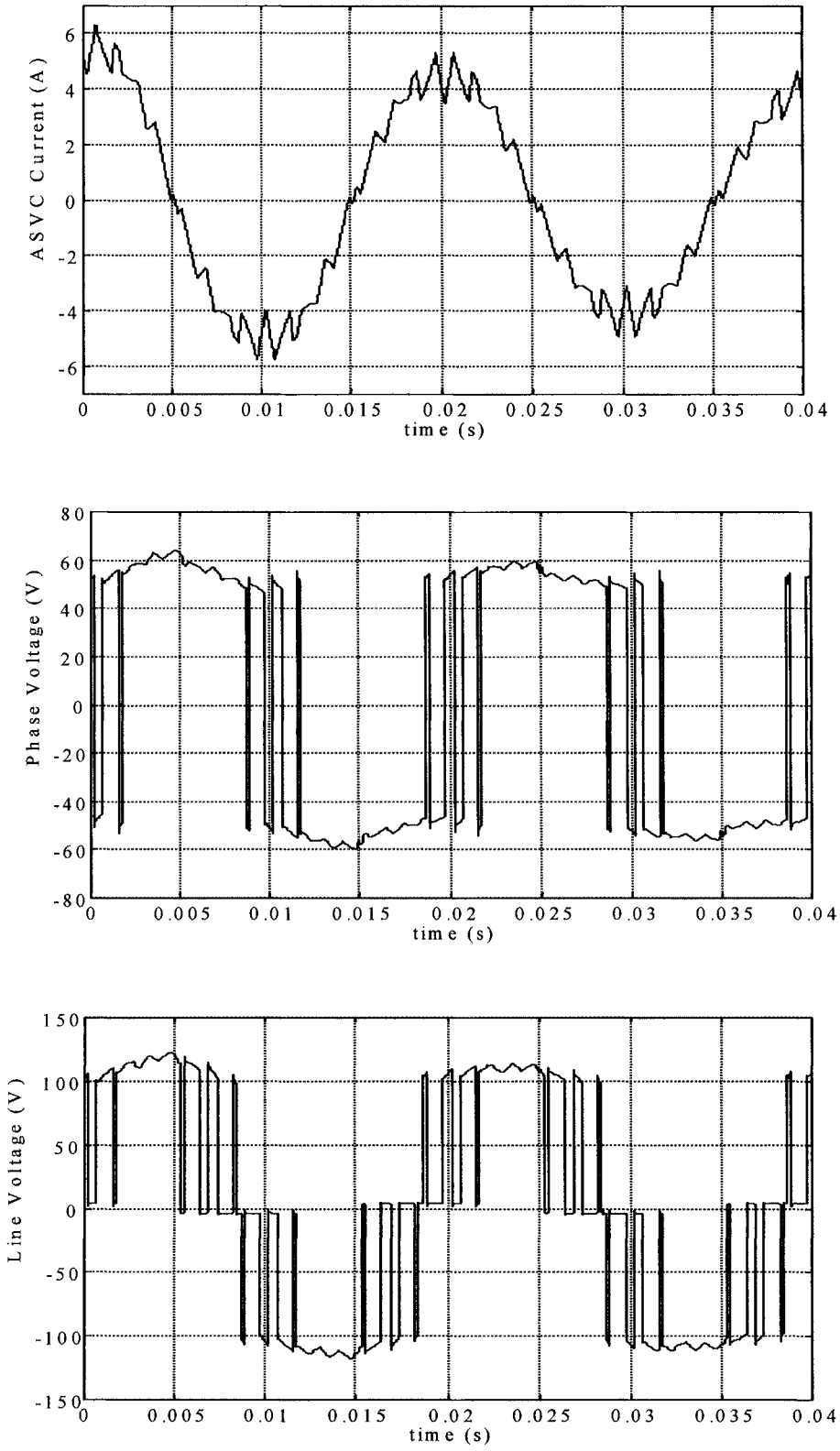


Figure 6.11 – Waveforms for a 2-level SHEM VSI based ASVC operating in the leading mode.

6.5.3 THE ASVC DURING SHORT-CIRCUIT DEVICE FAULTS

It is essential to maintain characteristic performance of the ASVC during the transient period of a device fault. If the ASVC is in either lagging or leading mode during normal operation, the adaptive VSI and controller must maintain the same mode of operation and the required level of compensation (i.e. same magnitudes of line current and output voltage) during the transient change to abnormal operating conditions.

It is predicted that there may be some requirement for a small phase angle change to maintain the required reactive power compensation in the event of the adaptive controller reverting to a 2-level SHEM strategy. This is entirely dependant upon the accuracy of the fundamental voltage magnitude that is selected when solving the harmonic equations required for calculating SHEM angles.

A short-circuit fault to S_{R1} is simulated to occur at t = 0.02 S. This is for visual simplicity of the simulated waveforms and it should be noted that the adaptive controller is operational at any point throughout the cycle. With the ASVC controlled to operate in the lagging mode the respective line current and output voltages during the transition period from 3-level SHEM to 2-level SHEM are illustrated in Figure 6.12. The waveforms for the transition during the leading mode of ASVC operation are also given in Figure 6.13.

The waveforms for both modes of operation illustrate a slight increase in the peak value of the ASVC current. This is due to a small increase in the fundamental component resultant from the 2-level SHEM. However, this is considered negligible and an effective closed loop reactive power control would easily correct this small difference. Also due to the difference between normal and abnormal operating currents being an increase it is put forward that this is beneficial rather than detrimental to the continual performance. For performance critical implementations, the off-line optimisation routines used to calculate the 2-level SHEM switching angles should use the fundamental component magnitude and the elimination of the required harmonics as its criteria.

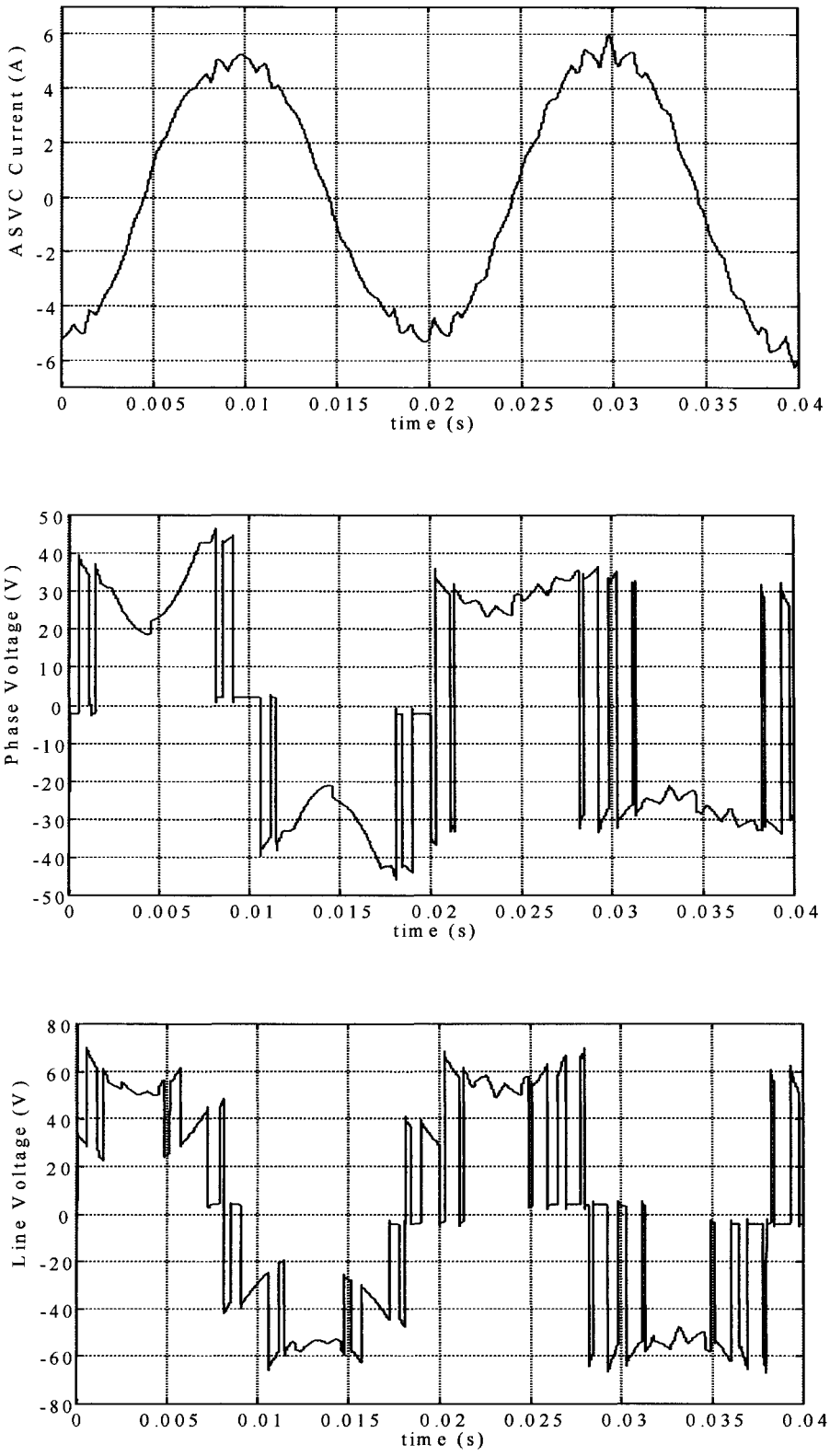


Figure 6.12 – Adaptive 3-2 scheme during lagging mode of ASVC operation

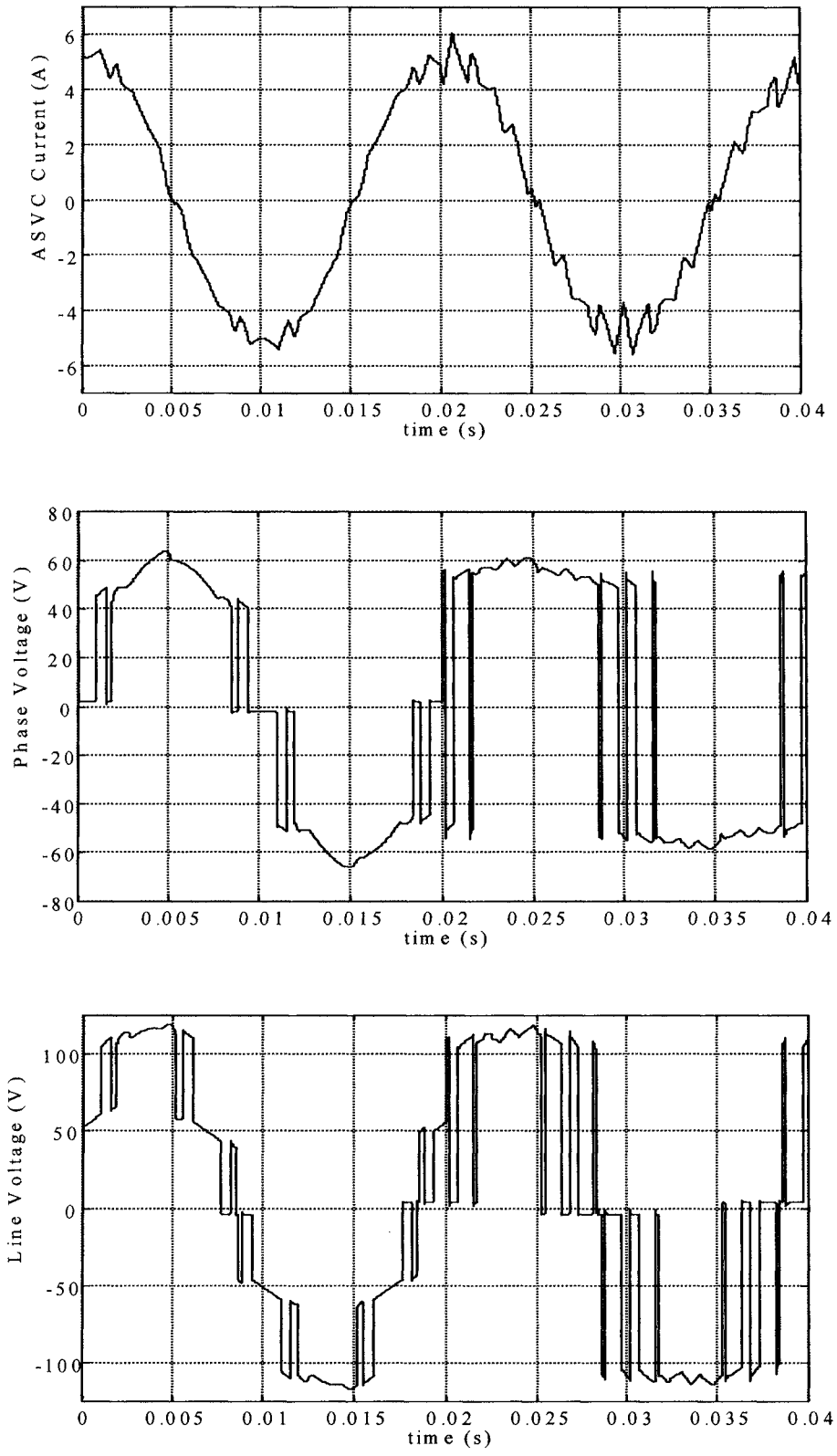


Figure 6.13 – Adaptive 3-2 scheme during leading mode of ASVC operation

7 CONSTRUCTION OF A LABORATORY MODEL THREE-LEVEL DPPSC-MLI

7.1 INTRODUCTION

The development of a hardware model 3-level DPPSC-MLI is presented throughout this Chapter. Utilising an analogue power circuit and a DSP based digital control system, the laboratory model enables real time analysis in order to verify the theoretical proposals and simulated results.

The construction and testing of a hardware model in real time is essential when proposing a 'new' inverter topology to be used within industrial applications. The simplification and assumptions used in the mathematical analysis or computer simulations of control circuitry and semiconductor characteristics will lead to errors in the obtained results. This is particularly the case with regards to the 'instantaneous' on/off response of an ideal switching device to a firing signal, or the off-line calculated optimised PWM switching angles. Therefore, whilst accepting that the simulation results provide indication for the design of the hardware model, possible testing procedures and predicted operation, it is crucial that operational errors are identified and when possible eliminated.

A general-purpose adaptive 3-level DPPSC-MLI topology with open-loop DSP based digital control and interactive serial-communication through a Pentium PC has been developed. The general structure is illustrated schematically in Figure 7.1. The hardware model was successfully built to demonstrate the operation of a ±1.2 kVAr ASVC and a +0.5 kVAr inductive load system representing a possible application to supply a passive load. The circuit diagram of the constructed laboratory power circuit with an inductive load is illustrated in Figure 7.2. The power-circuit hardware, inclusive of wiring current ratings, was suitably rated for envisaged forthcoming high power projects. The operational analysis of the proposed adaptive topology for both test procedures is presented in detail in Chapter 8. A schematic description of the main units of the laboratory hardware model is presented in the following sections.

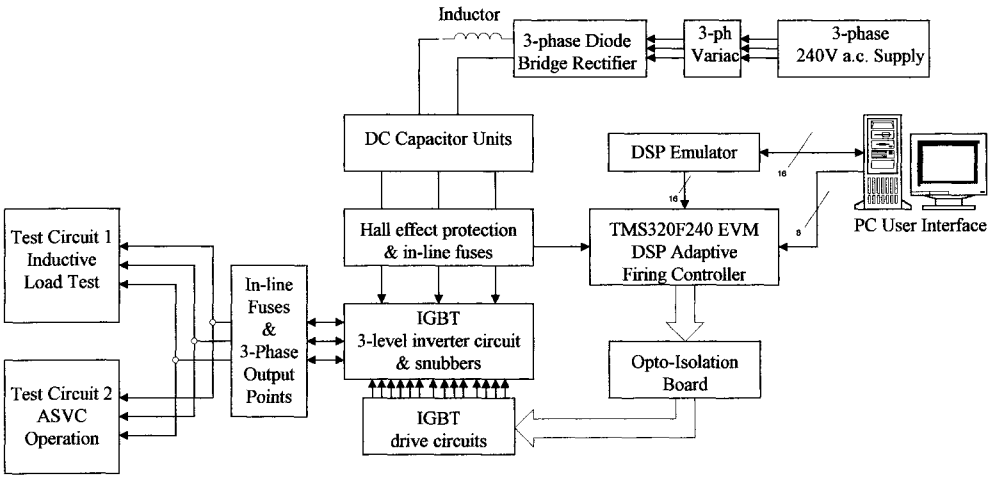


Figure 7.1 – Proposed Layout of the Hardware Model

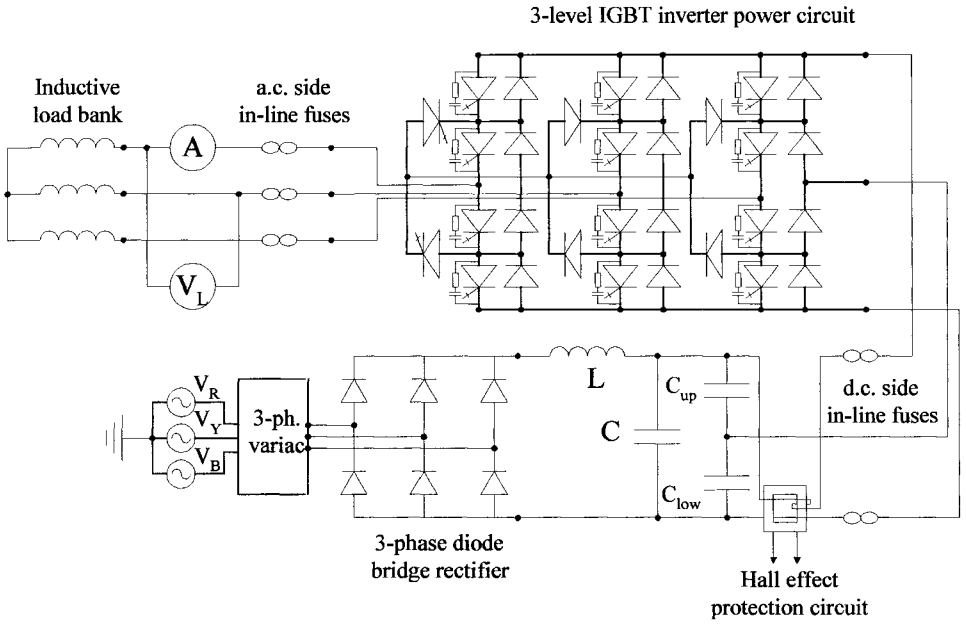


Figure 7.2 – Circuit diagram of the laboratory power circuit

7.2 DEVELOPMENT OF THE MAIN POWER CIRCUIT

The 3-level inverter power circuit can be subdivided into three units; the 3-level voltage source inverter circuit, the associated drive circuitry and the 'dc link' constructed from capacitor units. The actual 3-level VSI power circuit with associated device drivers is illustrated in Figure 7.3.

7.2.1 THE THREE-PHASE INVERTER CIRCUIT

In order to provide an inverter power-circuit that could be adapted into higher-level VSI topologies for future research, a modular design was adopted. By constructing three identical phase-limbs the design is both simplified and visually preferential for the identification of independent components. As the entire system was mounted within a cabinet with removable side panels, a layout for the inverter power circuit was selected to provide the researcher with accessibility to all power components in each phase-limb. The top surface device and wiring approach also enables ease of re-wiring for further manipulation of the power circuit. Each main phase-limb complete with main switching devices, anti-parallel diodes, auxiliary 'clamp' diodes and DPPS devices were mounted on individual SEMIKRON P3 heatsinks. The P3 range of heatsinks is ideal for the application as they provide mounting channels for the power modules as well as for additional accessories, e.g. device drivers [59].

It is acknowledged that for high-power industrial applications of the ASVC, due to present device ratings, the output power rating would require GTO's as the switching device to develop valves for the phase-limbs. However, for the purpose of constructing a laboratory scaled model, low power IGBT devices are more suitable. A suitable number of dual IGBT modules were available which have purposely built anti-parallel diodes within each module. Therefore, due to availability, the SEMIKRON SKM50GB100D IGBT modules, rated at 1000 V forward blocking voltage and maximum average on state current of 50 A, were used for the main switching devices in the phase-limbs. Although these particular

devices appear largely over-rated for the present application, they enable future research projects to develop the unit into a higher power rated system.

In the system developed for this project, the IGBT devices would be operated under normal conditions where they would be operated individually and simultaneously. In the case of a simulated device fault one of the devices would be continuously turned-on, simulating a short-circuit device. A simple RC snubber circuit in parallel with each device was implemented. The snubber circuit was constructed with the following component values: R = 10 Ω 2 W, C = 0.01 μF. The configuration of the SEMIKRON IGBT module with anti-parallel diode together with the designed RC snubber circuit is shown in the hardware implementation Appendix D, Figure D.2. Single discrete IGBT's were selected for the discharge path protection switch (DPPS) devices with comparable ratings to the dual modules. The international rectifier IRG4PH40U IGBT with a forward blocking rating of 1200 V and maximum average on-state current of 40 A was chosen for the DPPS devices. The emitter-to-collector breakdown voltage of this device is 18 V, illustrating the necessity for a series-connected diode to prevent reverse voltage breakdown.

Due to the availability of devices, SEMIKRON SEMIPACK SKKD45/08 fast diode modules with a peak reverse voltage of 800 V and average current of 45 A were used for the auxiliary 'clamp' diodes. As with the main switching devices, suitably rated dual modules were selected for two main reasons. Firstly, the modules were physically desirable with respect to size and fixing requirements for the heatsinks. Secondly, the module design minimises the requirement for additional wiring and therefore improves the overall layout of the power circuit to reduce RFI and switching noise.

7.2.2 IGBT Driver Circuits

Two types of driver circuits were used for the hardware model 3-level inverter. A hybrid double IGBT SEMIKRON SKHI 21 driver unit was used, largely due to availability and also due to its excellent performance and protection features

inherently constructed within the unit [59]. Although the typical application of the SKHI 21 driver is for IGBT modules used in a six-pulse bridge circuit, the dual outputs of the unit can be associated to devices within the 3-level phase limb making the driver suitable for the multi-level topology. However, due to the interlock protection feature of the SKHI 21 between the upper and lower drive signals, the driver is not suitable for demonstrating the adaptive 3-level DPPSC-MLI operation. This will be further discussed in the hardware protection for the system. To enable demonstration of the adaptive topology, further IGBT drivers were designed and constructed using a standard discrete component IGBT driver circuit. The design and testing is further discussed in Appendix D.

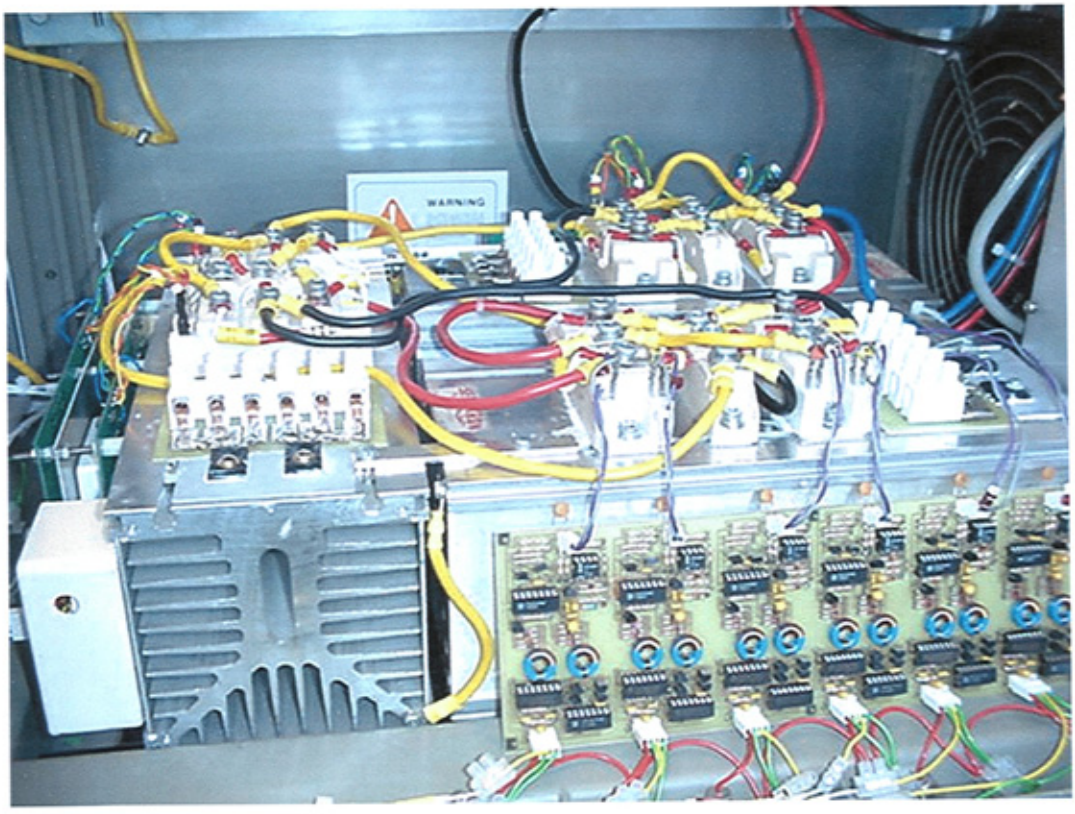


Figure 7.3 – Digital image of actual constructed power circuit

7.2.3 THE DC LINK AND ASSOCIATED '3-LEVEL' CAPACITOR BANK

As the 3-level VSI topology was being developed to provide a multi-application hardware model, the overall system required a simple d.c. link and a 3-level capacitor bank unit. The basic d.c. link was supplied from a 3-phase diode bridge with a series 25 mH inductor and a 2000 μF capacitor unit. The large capacitance provided an almost constant d.c. bus voltage that could be controlled simply by varying the three-phase a.c. input voltage with an in-line variac. The d.c. link capacitor was then connected in parallel to the 3-level capacitor unit. Also as the 3-level VSI ASVC was implemented with an open-loop control system, the charging and discharging of the 3-level capacitor bank, for control of reactive power flow, was not available through conventional ASVC closed loop phase angle control. Therefore the variable d.c. bus voltage enabled multiple experimental tests, as will be further presented in Chapter 8. Details illustrating the construction of the d.c. link and associated '3-level' capacitor bank are given in Appendix D.

7.3 DEVELOPMENT OF THE DSP BASED ADAPTIVE DPPS CONTROLLER

7.3.1 DEVELOPMENT OF CONTROL HARDWARE

The digital control system hardware is developed around a digital signal processor (DSP) evaluation module (EVM). The TMS320F240 EVM, which was selected for this application, is a standalone evaluation PCB that enables operational and system architectural exploration of the 'F240 CPU and its associated peripherals. The TMS320F240 DSP controller is proposed by Texas Instruments as being optimised for digital motor control and power conversion applications [60].

Using the parallel port of a host PC the evaluation board is targeted using a standard IEEE1149.1 cable connected to the emulation port on the DSP EVM. The main interface between the software debugger host and the 'F240 evaluation board is provided by an XDS510PP emulator included with the evaluation package. A Pentium PC is used as the host processor for the assembly language tools and code debugging software. This provides a user interface for creation and debugging of switching control schemes and real-time user interaction, through the XDS510PP emulator, to the digital controller. The 'F240 evaluation board also has an on-board RS-232 compatible serial port for asynchronous communication. Using this serial port on the EVM the serial communications interface (SCI) peripheral on the 'F240 DSP can be configured for user interaction communications protocols. For this project, the Microsoft Windows HyperTerminal protocol was utilised for real-time interaction of reference signal phase shifting and generated sinewave frequency manipulation.

The evaluation board provides a bank of eight D.I.P. switches enabling possible user interaction with DSP real-time operation. These switches are mapped as read-only inputs to the I/O memory space of the 'F240 DSP. For this project the D.I.P. switches are used for initialisation of the control scheme (on/off) and also to simulate short-circuit faults to the devices in the red (R) phase.

On-chip, dual, 10-bit analogue-to-digital converter (ADC) modules are provided by the 'F240 DSP. These are complemented with EVM on-board, quad, 12-bit digital-to-analogue converter (DAC) modules. The provision of the input ADC's and output DAC's is utilised within this project. Although a phase-locked-loop (PLL) system is not implemented into the open loop switching controller developed in this project, the ADC's are ideal for further development of digital-phase-locked-loop (DPLL) techniques to be implemented in further research. For observation of the operational performance of the PLL the on-board DAC's provide an ideal analysis point for the reference sinewaves. As this project generates reference sinewaves through interpolation routines, the DAC outputs are used for observation of the angular quality of the waveforms used to derive the SHEM switching angles. They are also used to indicate leading or lagging phase shifting of the generated system voltage reference and the switching angle reference sinewave.

A control expansion board was designed to provide 4x34-pin IDC connection points for the DSP signal buses of the EVM. Also, test points were provided to allow observation of generated reference sine waves, firing signals or software protection signals. Using 34 way ribbon cable, unshrouded headers and bump polarised sockets the EVM connector signals were transferred to the control expansion board and distributed to an array of tests point pins suitable for connecting oscilloscope probes without actual contact with the EVM board. Driver signal isolation was then provided in the form of a bank of logic-to-logic high-speed optocouplers. These were implemented to isolate the DSP from the driver boards. All driver output signals after the opto-isolation stage and required power supply signals were provided with on-board connectors. The constructed control board with the 'F240 EVM mounted in position is illustrated in the digital image given in Figure 7.4.

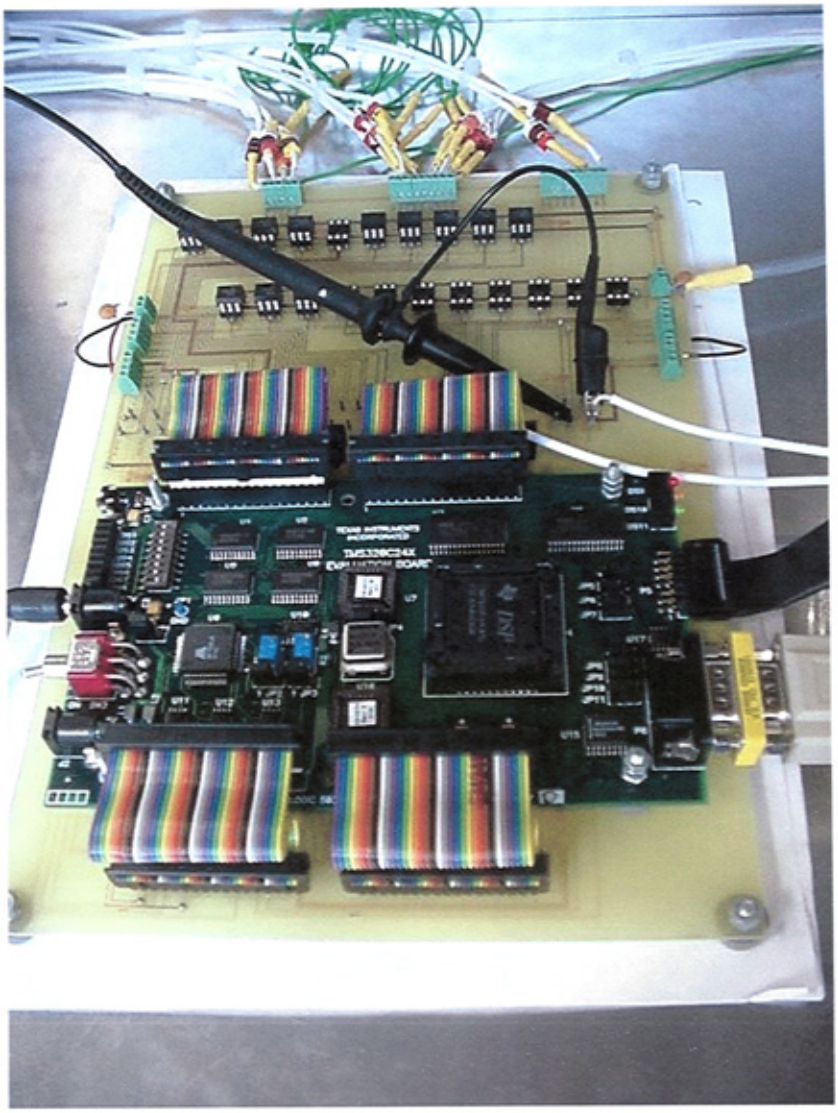


Figure 7.4 – TMS320F20 DSP EVM mounted on the control board.

7.3.2 DEVELOPMENT OF ADAPTIVE SWITCHING CONTROL SOFTWARE

The control software for the experimental model digital DSP controller was initially developed in assembly language and converted into a machine code format suitable to be embedded on the TMS320F240 DSP EVM target board. Due to the requirement for a real-time system, this programming methodology provides suitable sequential running of the implemented code. The development of the adaptive switching control scheme software can be separated into two principle areas:

- Generation of reference sinewaves and serial communication for real-time user interface through host PC.
- Production of adaptive switching control algorithms.

The methodology behind developing these two areas of control software independently and then combining them to produce the complete open-loop adaptive switching control scheme software is presented in the following sections. A section of the assembly language code, to illustrate the generated sinewave and switching control, for a 3-level to 2-level adaptive SHEM switching strategy is presented in Appendix E.

7.3.2.1 REFERENCE SINEWAVES AND SERIAL COMMUNICATION

For the open-loop switching controller two reference sinewaves were required to be generated. The first sinewave represents the reference signal that would be normally obtained through a phase-locked-loop (PLL). The second sinewave is developed for phase angular control of the switching firing signals. The operational performance of the system with a SHEM switching strategy, with respect to elimination of harmonics, is largely dependant upon the accuracy of the firing signals. The generation of reference sinewaves is achieved using look-up tables and then interpolation algorithms to obtain the required accuracy.

A serial communication link was developed to the host PC providing a user interface. As the system generates reference sinewaves the controller requires a user interface that allows reference signal frequency manipulation similar to a PLL. Therefore, the user can select the required system frequency for the output firing signals. Also, the second generated reference sinewave for the switching angles required the possibility of phase shift with respect to the 'PLL' sinewave. This was implemented such that the reference signal algorithm could later be developed to demonstrate the operation of the ASVC in both leading and lagging VAr compensation modes. The Windows HyperTerminal serial communications protocol was used for the user interface application. Using the vast library of suitable pre-developed code available from Texas Instruments application notes, the serial link and sinewave generation code was developed by manipulation of two EVM code templates [61]. The reference sinewave generation and serial communication algorithm, together with initialisation routines required for the DSP, are illustrated in the flow diagram shown in Figure 7.5.

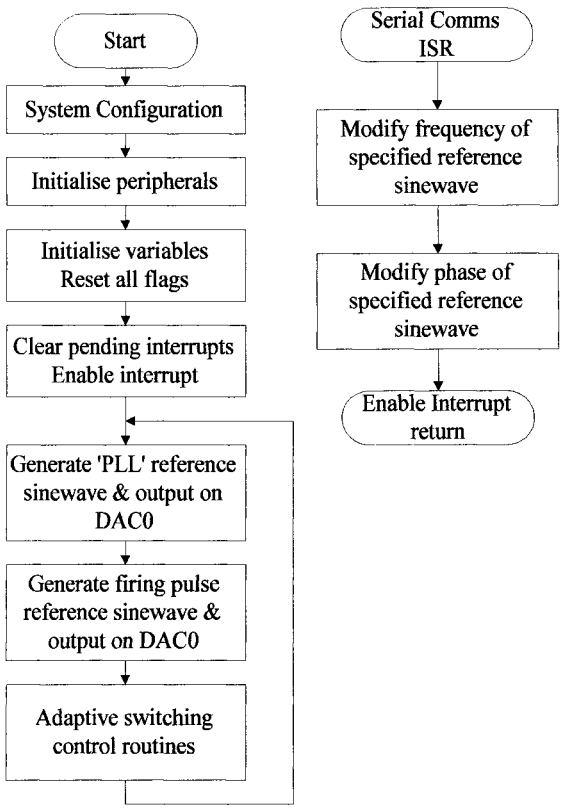


Figure 7.5 – DSP initialisation and main program algorithm

7.3.2.2 ADAPTIVE SWITCHING CONTROL ALGORITHMS

Adaptive switching control algorithms were developed for various FFM and SHEM strategies for both 3-level and 2-level operation of the inverter. All developed switching strategy codes were implemented and analysed for performance, as will be illustrated in Chapter 8. However, a generalised development that mainly focuses upon the 3-level to 2-level adaptive SHEM strategy software is presented in this section.

Once the DSP EVM board was initialised from the host PC, the generation of reference sinewaves and the serial communication link was developed to run continuously. However, the requirement of the adaptive switching controller is such that the user must be able to activate or de-activate the switching strategy. An initial template for the adaptive switching control was developed before any PWM schemes were produced. As illustrated in Figure 7.6 the adaptive control scheme software template controlled the flow of the adaptive controller strategy under normal or abnormal operating conditions.

The next stage of development was to configure the required output ports for the firing signals to the 3-level inverter. Table 7.1 illustrates the DSP I/O ports and there associated device-firing signals. As the adaptive controller was being developed to demonstrate system performance in the event of a short-circuit device fault in the red phase, no drive signals were configured for the yellow and blue phase DPPS devices. As far as the fault tolerant operation capability is concerned, it is adequate to consider faults on a representative phase.

S_{R1}	S_{R2}	S_{R3}	S_{R4}	$DPPS_{R1}$	$DPPS_{R2}$
IOPA0	IOPA1	IOPA2	IOPA3	IOPB4	IOPB5
S_{Y1}	S_{Y2}	S_{Y3}	S_{Y4}	$DPPS_{Y1}$	$DPPS_{Y2}$
IOPB0	IOPB1	IOPB2	IOPB3	N/A	N/A
S_{B1}	S_{B2}	S_{B3}	S_{B4}	$DPPS_{B1}$	$DPPS_{B2}$
IOPC4	IOPC5	IOPC6	IOPC7	N/A	N/A

Table 7.1 – Assignment of digital I/O ports to firing signals

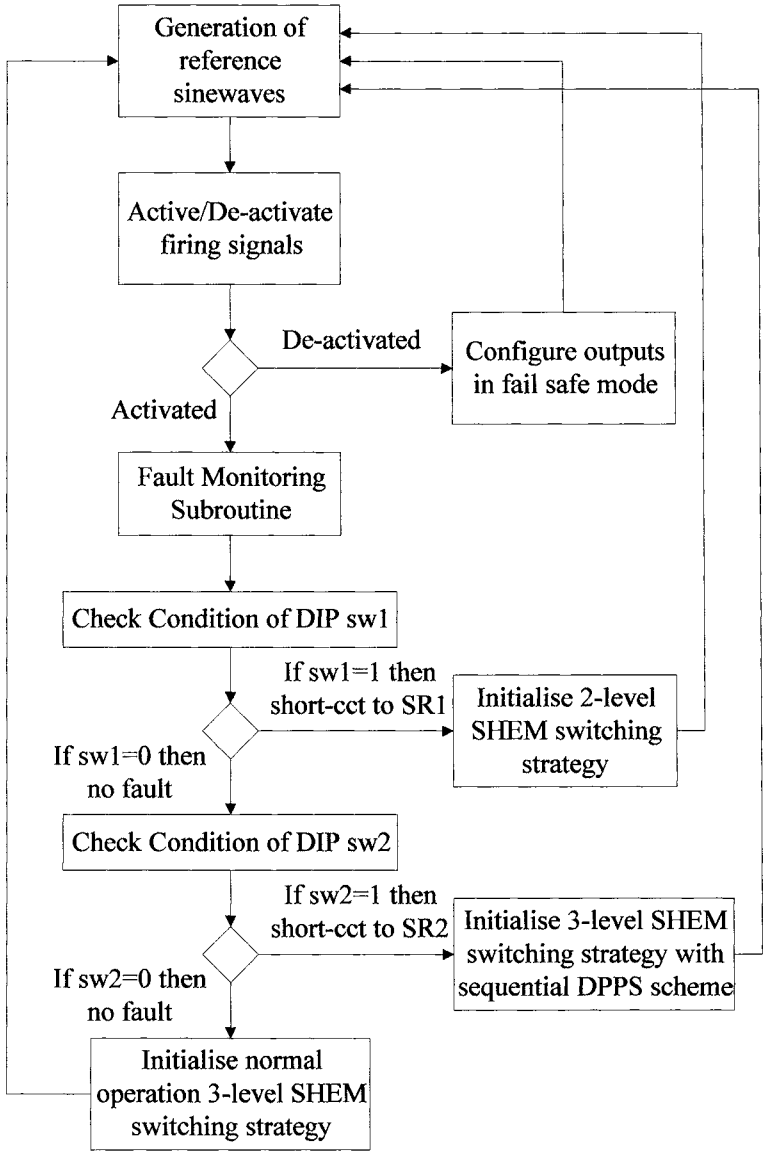


Figure 7.6 – Simplified flow chart of adaptive control template

The digital firing pulse generation for normal or abnormal operating conditions was produced with the control strategies presented in Chapter 6. Thereby for normal operating conditions the DPPS devices remained activated and under abnormal operating conditions the DPPS devices were either sequentially activated within the dead band region of the faulty device, or de-activated for implementing a 2-level switching strategy. Using the second generated reference sinewave the interpolation look-up table was implemented to determine a firing angle reference point. As with standard digital PWM schemes one sinusoidal

reference is used to produce the firing signals for all three-phases of the inverter. By gradient calculations and determining the appropriate half cycle of the reference sinewave, a subroutine was developed to generate the required firing signals. A generalised form of the firing pulse subroutine is illustrated in Figure 7.7. Developing a form of three-phase angular timing diagrams produced a methodology of determining the required digital output port conditions, for the generation of firing signals to the inverter. The angular reference diagrams were produced in two sections for the positive half cycle and negative half cycle of the required three-phase output. This is illustrated for the normal operation 3-level SHEM strategy in Figures 7.8 and 7.9, together with tabulated angular switching conditions. This is also illustrated for the abnormal 2-level SHEM three-phase switching strategy in Figures 7.10 and 7.11. The switching angles, illustrated in these diagrams for the 3-level and 2-level schemes, are obtained from the harmonic analysis presented in Chapter 5.

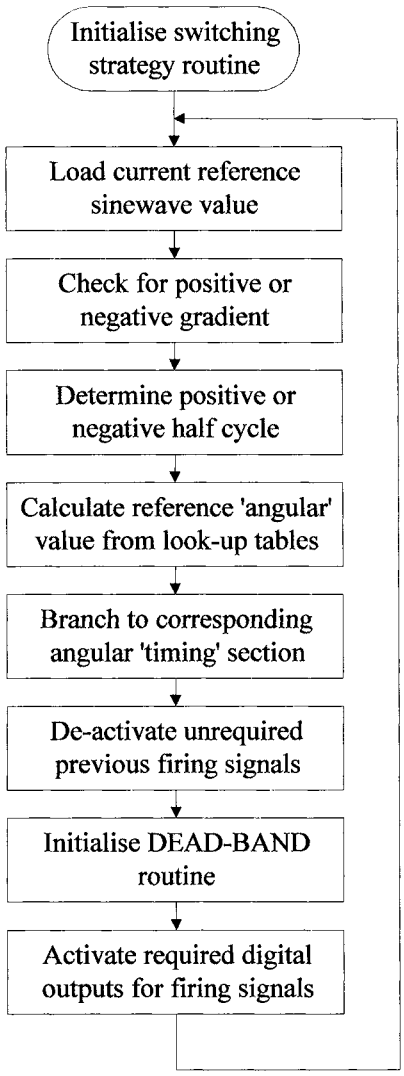
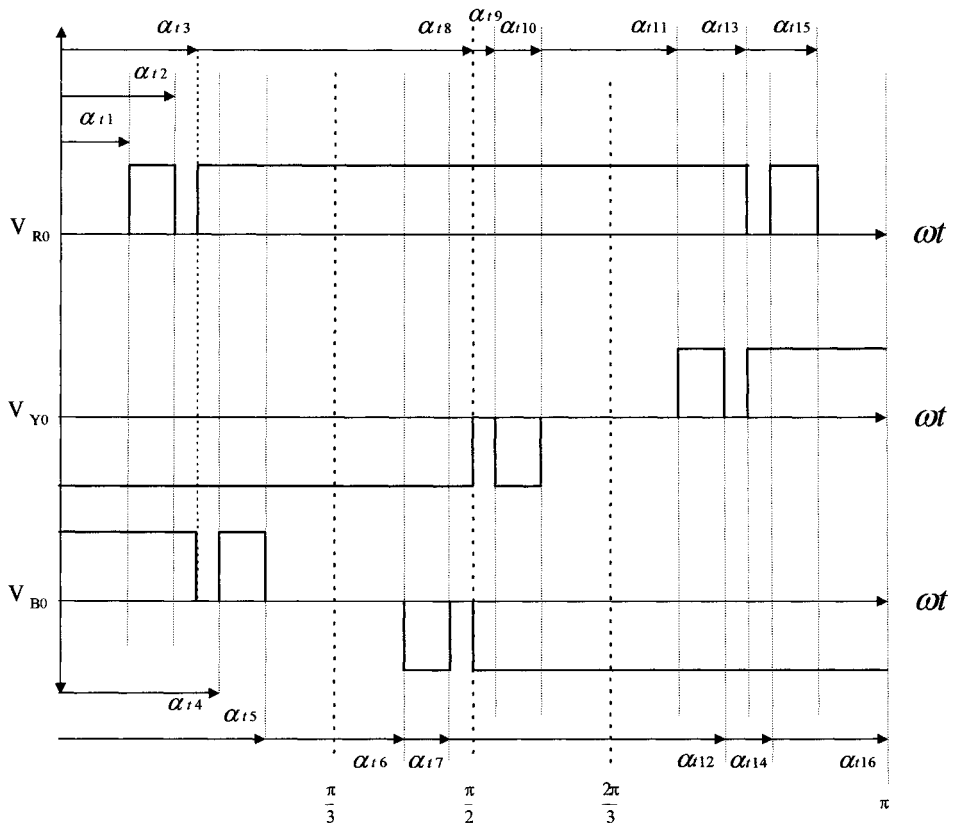


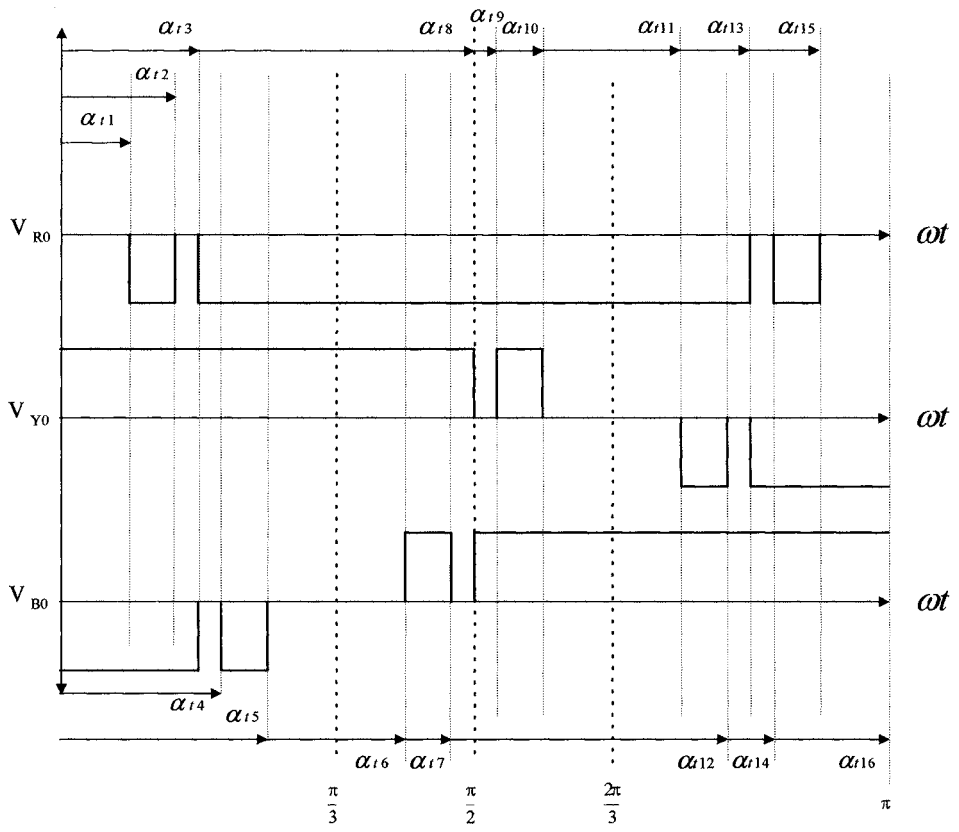
Figure 7.7 – Outline of firing pulse generation subroutine



α_{t1}	α_{t2}	α_{t3}	α_{t4}	α_{t5}	α_{t6}	α_{t7}	α_{t8}
14.016°	24.504°	30°	35.496°	45.984°	74.016°	84.504°	90°

α_{t9}	α_{t10}	α_{t11}	α_{t12}	α_{t13}	α_{t14}	α_{t15}	α_{t16}
95.496°	105.98°	134.02°	144.504°	150°	155.49°	165.98°	180°

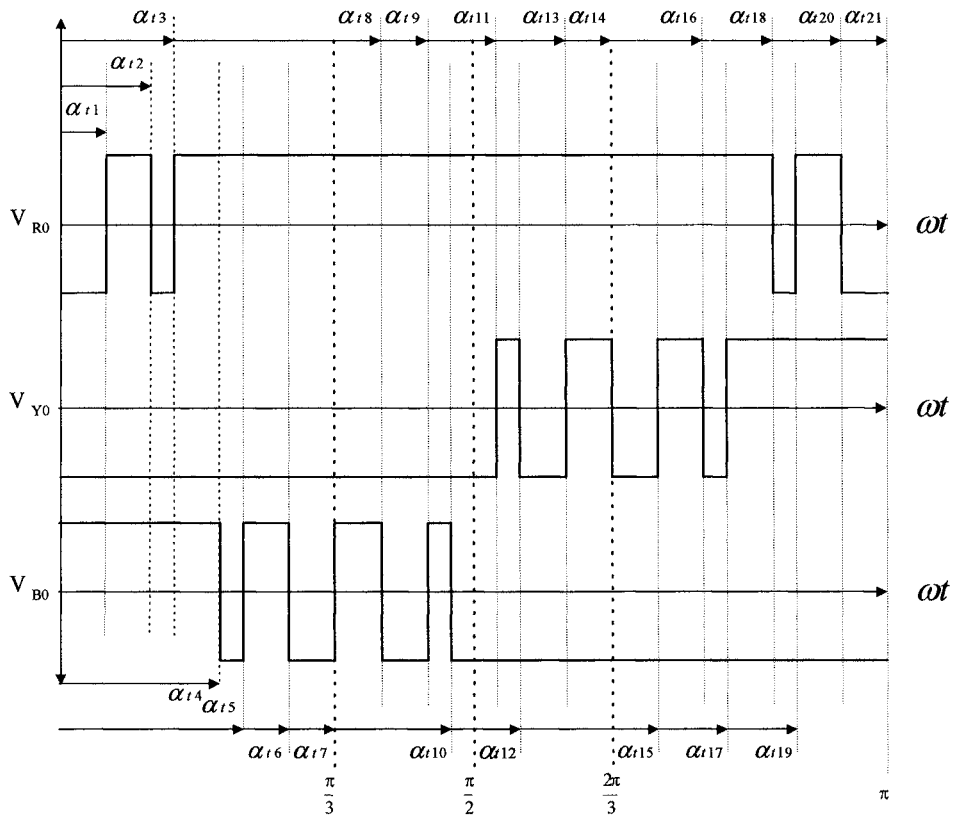
Figure 7.8 – Angular 'timing' reference diagram for production of the positive cycle three-phase 3-level SHEM firing signals.



α_{t1}	α_{t2}	α_{t3}	α_{t4}	α_{t5}	α_{t6}	α_{t7}	α_{t8}
194.016°	204.504°	210°	215.496°	225.984°	254.016°	264.504°	270°

α_{t9}	α_{t10}	α_{t11}	α_{t12}	α_{t13}	α_{t14}	α_{t15}	α_{t16}
275.496°	285.984°	314.016°	324.504°	330°	335.496°	345.984°	360°

Figure 7.9 – Angular 'timing' reference diagram for production of the negative cycle three-phase 3-level SHEM firing signals.

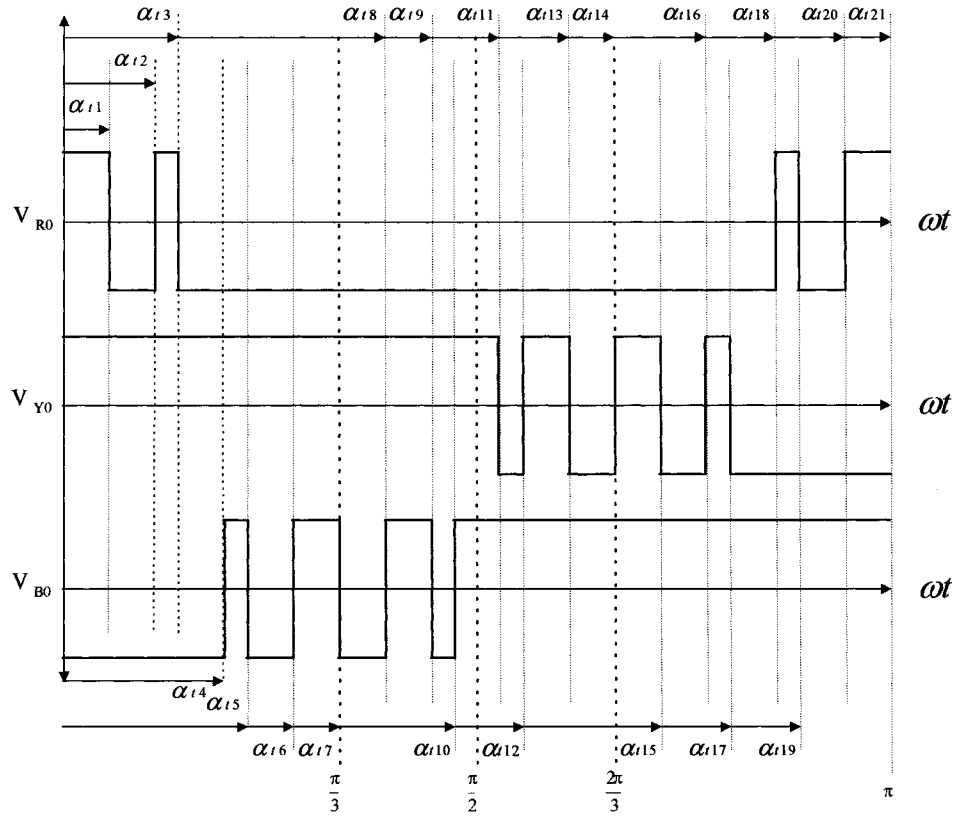


α_{t1}	α_{t2}	α_{t3}	α_{t4}	α_{t5}	α_{t6}	α_{t7}
8.74°	24.397°	27.76°	32.24°	35.603°	51.26°	60°

α_{t8}	α_{t9}	α_{t10}	α_{t11}	α_{t12}	α_{t13}	α_{t14}
68.74°	84.397°	87.76°	92.24°	95.603°	111.26°	120°

α_{t15}	α_{t16}	α_{t17}	α_{t18}	α_{t19}	α_{t20}	α_{t21}
128.74°	144.397°	147.76°	152.24°	155.603°	171.26°	180°

Figure 7.10 – Angular 'timing' reference diagram for production of the positive cycle three-phase 2-level SHEM firing signals.



α_{t1}	α_{t2}	α_{t3}	α_{t4}	α_{t5}	α_{t6}	α_{t7}
188.74°	204.397°	207.76°	212.24°	215.603°	231.26°	240°

α_{t8}	α_{t9}	α_{t10}	α_{t11}	α_{t12}	α_{t13}	α_{t14}
248.74°	264.397°	267.76°	272.24°	275.603°	291.26°	300°

α_{t15}	α_{t16}	α_{t17}	α_{t18}	α_{t19}	α_{t20}	α_{t21}
308.74°	324.397°	327.76°	332.24°	335.603°	351.26°	360°

Figure 7.11 – Angular 'timing' reference diagram for production of the negative cycle three-phase 2-level SHEM firing signals.

7.4 PROTECTION CIRCUITS

The possibility of both normal and abnormal operation of the 3-level DPPSC-MLI, with respect to device faults, exemplifies the requirement for a well-designed protection scheme to cover all eventualities. Together with providing protection against the conventional overcurrent possibilities associated with the application, the overall scheme must also protect the power circuit devices, drivers, d.c. link capacitors and the digital controller. A combination of hardware and software methods was implemented to provide the required control scheme, as presented in the following sections.

7.4.1 HARDWARE PROTECTION

Two methodologies were applied for the hardware protection scheme; overcurrent protection and driver interlock. After consultations with SEMIKRON engineers, to determine the most effective 'belt and braces' overcurrent protection scheme to protect both the inverter circuit and the dc link capacitors, ultra rapid European D11 type fuses were selected. Rated at 500 V AC / 440 V DC and 6 A or 15 A, depending upon the particular test procedure, the fuses were implemented in-line at both the d.c. (input) and a.c. (output) sides of the inverter circuit. The positioning of the in-line fuses is illustrated in Figure 7.1. The d.c. side fuses protect both the inverter and the d.c. link capacitors. The a.c. side fuses protects against overcurrents resulting from the driven synchronous machine if the excitation was too large and the reactive power back to the inverter increased or the machine became unstable. This test procedure is presented in Chapter 8.

Hardware protection of the inverter IGBT's is also provided through the driver units. The SEMIKRON SKHI 21 double IGBT driver unit features built in circuit protection in the form of short-circuit device protection by V_{ce} monitoring. Drive interlock protection is also provided between the upper and lower drive signals to prevent the occurrence of d.c. shoot through in a six-pulse bridge. However, due to the arrangement of the 3-level phase-limb and the switching strategy required for a three-level operation, the V_{ce} monitoring protection had to be disabled as it

was preventing the operation of the circuit [59]. As the hardware model was to demonstrate the adaptive topology with faults to the red phase-limb the interlock protection was not suitable. However, the drive interlock protection was found useful for the yellow and blue phases of the power circuit as by interconnecting the output drive signals of two of the SKHI 21 units, as illustrated in Figure 7.12, the protection prevents the possibility of the upper and lower devices being turned on simultaneously. After artificially introducing the fault on phase R, the digital controller would apply a continuous drive signal to the simulated 'faulty' device to represent a short-circuit fault. Therefore the SKHI21 driver is not suitable, as it would lockout the other drive signal that the driver unit was providing and prevents continual operation. For this reason the single IGBT driver circuits were developed for the red phase as presented earlier.

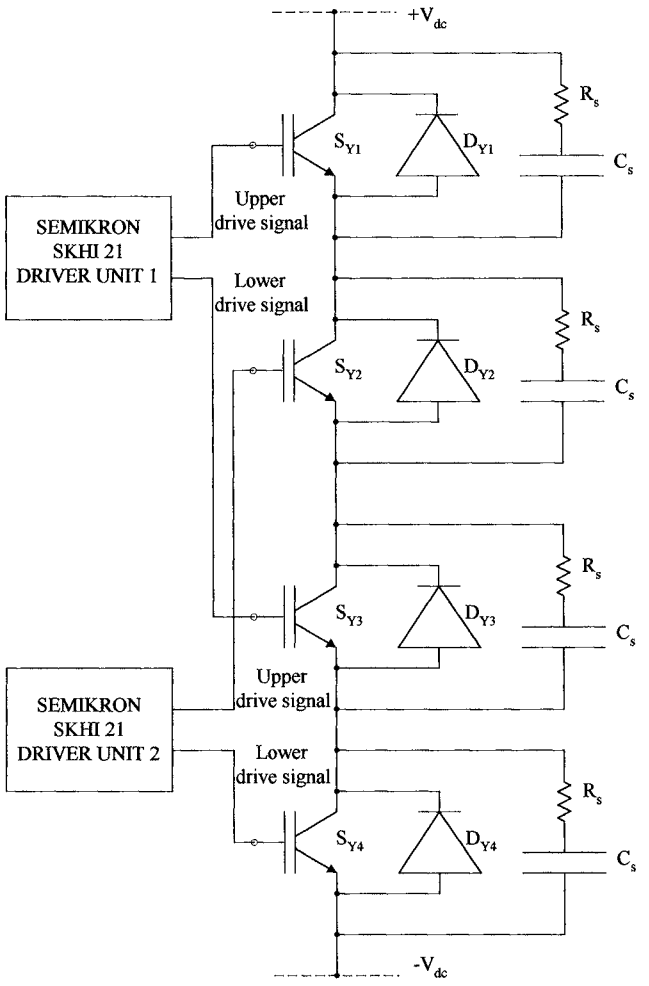


Figure 7.12 – SKHI 21 driver configuration

7.4.2 SOFTWARE PROTECTION

For improved response time an overcurrent software protection scheme was implemented to inhibit the firing signals from the switching controller to the drivers and therefore shutting down the inverter in a fail-safe mode. The software protection scheme was developed by programming an interrupt sub-routine into

the adaptive switching controller, which receives a control signal from the current measuring devices connected to the power circuit. Due to the test procedures for this laboratory hardware model the most effective position for the current sensors was between the d.c.-link and the inverter phase-limbs, as illustrated in Figure 7.1. The current was measured using a LEM LTA 100-P/SP1 current transducer. This Hall effect module provided the required sensitivity and a very fast response time. The overcurrent protection scheme, as shown in Figure 7.13, was calibrated such that if the d.c. current level of the capacitor bank output was too high, a signal would isolate the firing signals via the DSP digital controller and thus inhibit the operation of the IGBT's until a manual reset was performed.

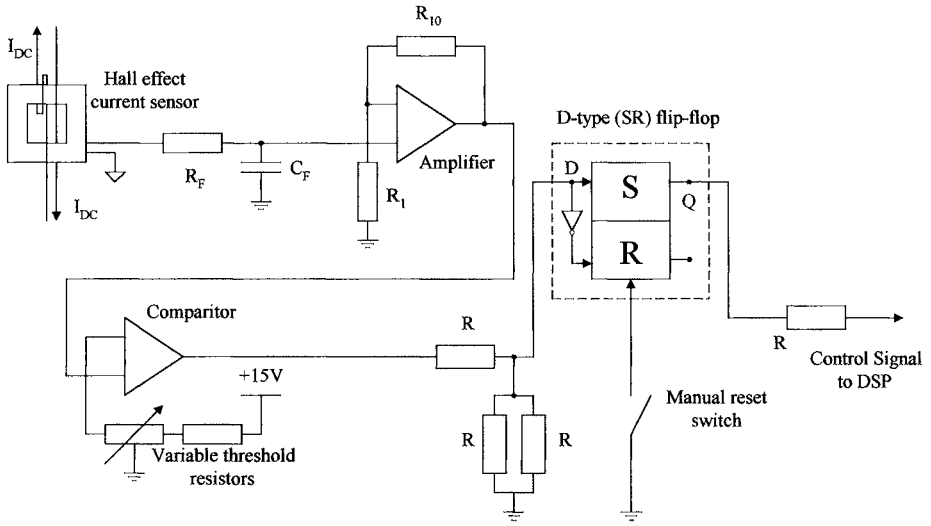


Figure 7.13 – Overcurrent protection circuit layout

7.5 CONSTRUCTION OF COMPLETE HARDWARE MODEL

The 3-level DPPSC-MLI power circuit with drivers, d.c. link capacitor units, DSP controller and power supplies were mounted inside a cabinet, as illustrated in Figure 7.14. Shelves were constructed within the cabinet using 4mm aluminium sheets to reduce radio frequency interference (RFI) and switching noise coupling from the power circuit to the DSP controller. The power circuit was mounted in the lower section of the cabinet as a cooling fan was already fixed at this position. The d.c. link capacitor units and protection circuits were located on the next two

levels with the TMS320F240 EVM and control board mounted to the top shelve. All drive and control signal wiring was implemented using Belden single core screened cable to minimise the switching noise and to prevent misfiring or spurious tripping of the protection circuits. The phase-limbs and cabinet shelves were also earthed with separate power grounds for safety and signal grounds for noise reduction. The Pentium PC user terminal (not shown) was positioned on the workbench next to the cabinet and the test loads were situated outside the cabinet so they could be easily modified for further research.

Figure 7.14 – The hardware model mounted within a shelved cabinet

8 PERFORMANCE ANALYSIS OF 3-LEVEL DPPSC-MLI

8.1 INTRODUCTION

Once the hardware model had been constructed and preliminary tests had been performed, a series of tests were devised to investigate the performance of the 3-level VSI and the adaptive DPPS controller. The performance of the adaptive VSI topology hardware model was analysed in the event of a device fault and for operation as an ASVC. Details of the tests are given in the following sections. The experimental laboratory set up is shown in Figure 8.1 and overall performance is discussed at the end of this Chapter.

8.2 ADAPTIVE TOPOLOGY PERFORMANCE UNDER NORMAL & ABNORMAL OPERATING CONDITIONS (TEST 1)

To demonstrate the operational performance of the adaptive 3-level VSI topology experimental model, under normal and abnormal operating conditions, the system was set up as illustrated in Figure 8.2. The load impedance was selected to obtain an output line current of 4 A for a d.c. link voltage of 100 V. The dc link was supplied from a 6-pulse diode bridge rectifier, as presented in section 7.2.3. A 2000 μF capacitor was used for the dc link and 333 μF capacitors for the upper and lower links. A voltage divider (R_1 and R_2) is used to balance the capacitors voltage. The inductive load bank exhibits an X/R ratio of approximately 10. All currents and voltages were measured using a Tectronics current probe and differential voltage unit respectively. The results were captured using a Tectronics TDS3034 digital 300MHz 4-channel oscilloscope.

(a) – The experimental layout for adaptive performance (test 1)

(b) – Generalised machine experimental layout to demonstrate ASVC performance (test 2)

Figure 8.1 – Experimental layouts for the laboratory model tests.

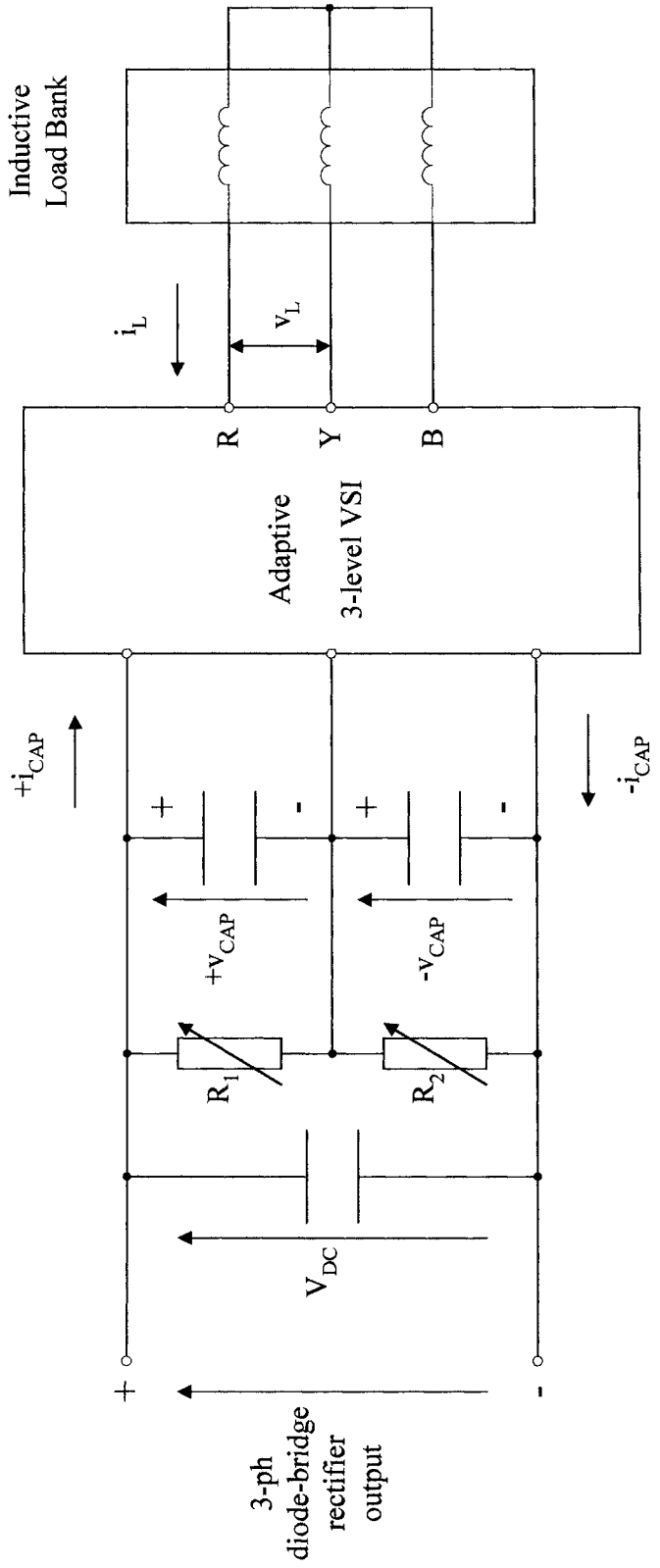


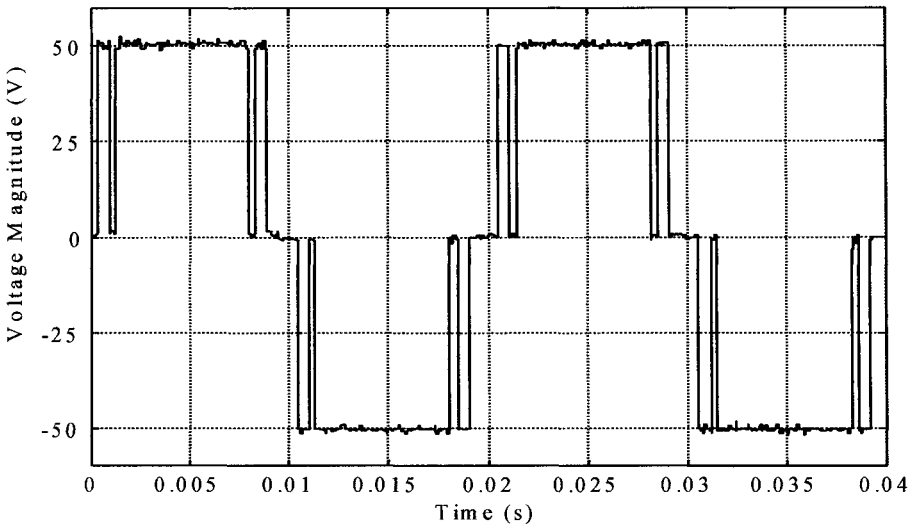
Figure 8.2 – Adaptive Performance with Inductive Load Bank Test Circuit.

8.2.1 SHEM OPERATED VSI SYSTEM PERFORMANCE WITH NO-LOAD

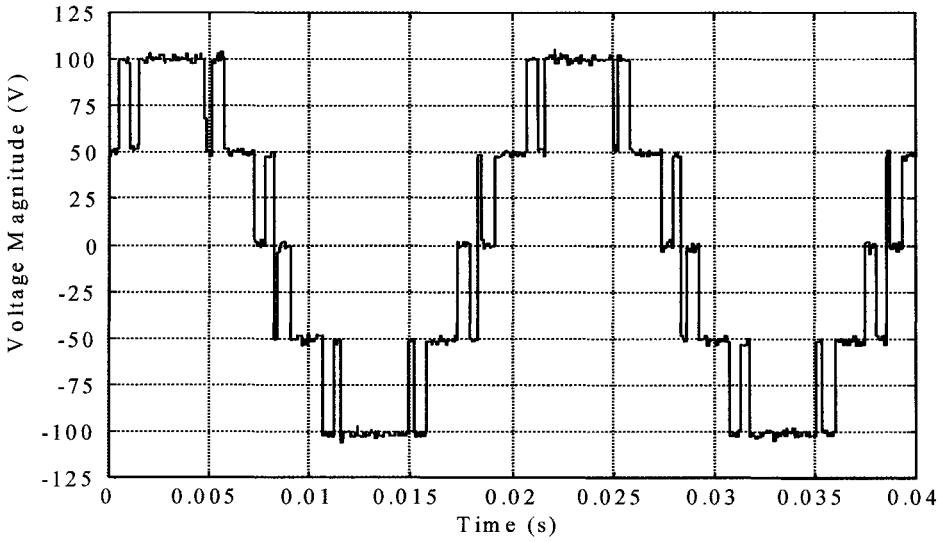
Using the experimental layout given in Figure 8.2, the adaptive 3-level VSI topology was initially tested with the inductive load bank switched out to represent a no-load or 'floating' operating condition. This test enables observation of the harmonic performance of the hardware model output voltages using a SHEM switching strategy under normal and abnormal operating conditions. Both adaptive control strategies, as described in Chapter 6, have been tested and results obtained are presented in the form of voltage waveforms to demonstrate continual operation and the additional voltage stress upon each device.

For normal operation, the 3-level VSI topology was implemented with a 3-angle SHEM switching control strategy, as presented in Chapter 6. The reference sinewave frequency was set to 50 Hz using the host processor user terminal to represent the UK power system frequency. Figure 8.3 shows the phase and line voltages obtained from the laboratory model for normal operation at no-load conditions. The phase voltage is referenced to the d.c. neutral.

To demonstrate the adaptive controller operation, a short-circuit fault was simulated to device S_{R1}. As presented in Chapter 6 the controller should revert the VSI topology to a 2-level system and produce a bi-polar 3-angle SHEM switching strategy to recover the performance. The results obtained are shown in Figure 8.4 where the frequency and the r.m.s. values of the phase and line voltages are maintained during the abnormal operation. Removing the simulated short-circuit fault to S_{R1}, the system reverts back to the normal operation 3-level SHEM control scheme. The harmonic spectra of the original 3-level and the post-fault 2-level output line voltages for floating conditions with a 3-angle SHEM strategy are shown in Figure 8.5. For each case, the percentage values of the individual harmonic component in the output line voltages for both normal and abnormal operating conditions are compared in Table 8.1. These values are also compared with the theoretical calculation result.

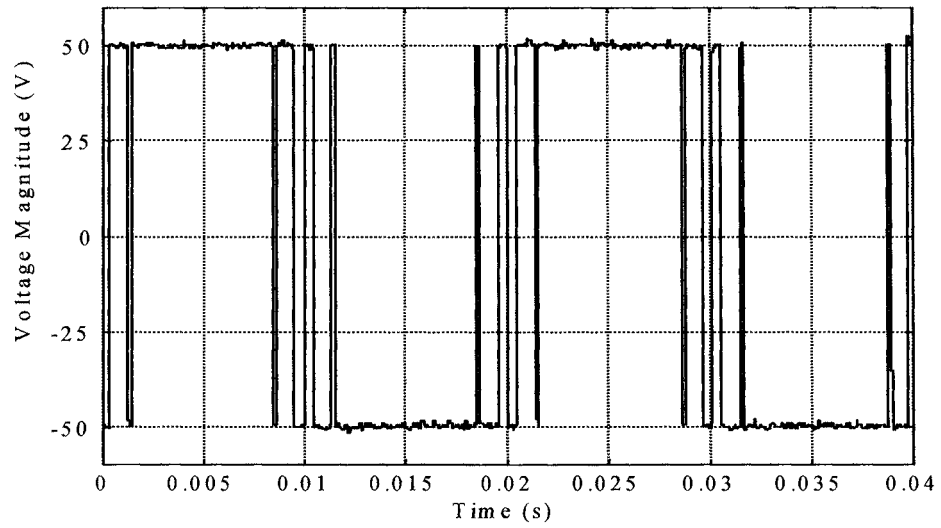


(a) – 3-level VSI output phase voltage

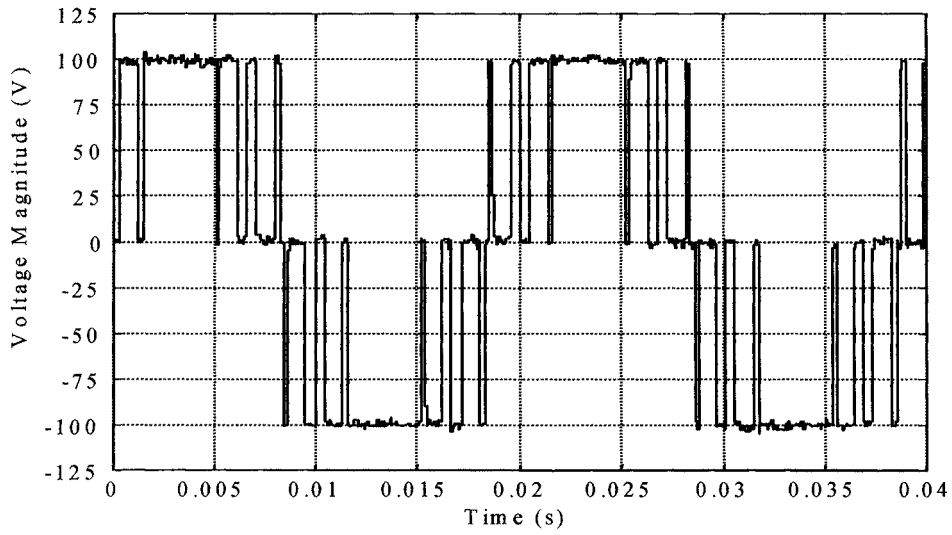


(b) – 3-level VSI output line voltage

Figure 8.3 – Waveforms for 3-level SHEM operation with the VSI at no-load

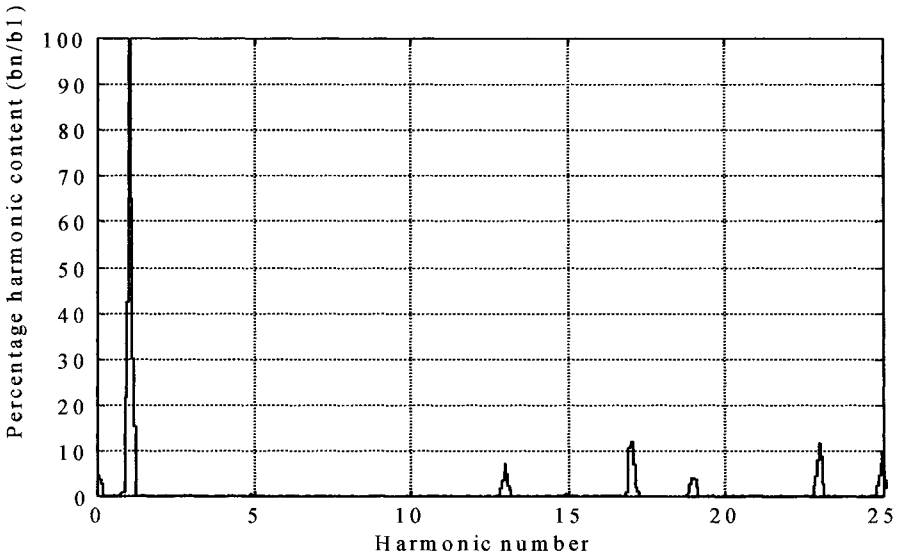


(a) – 2-level VSI output phase voltage

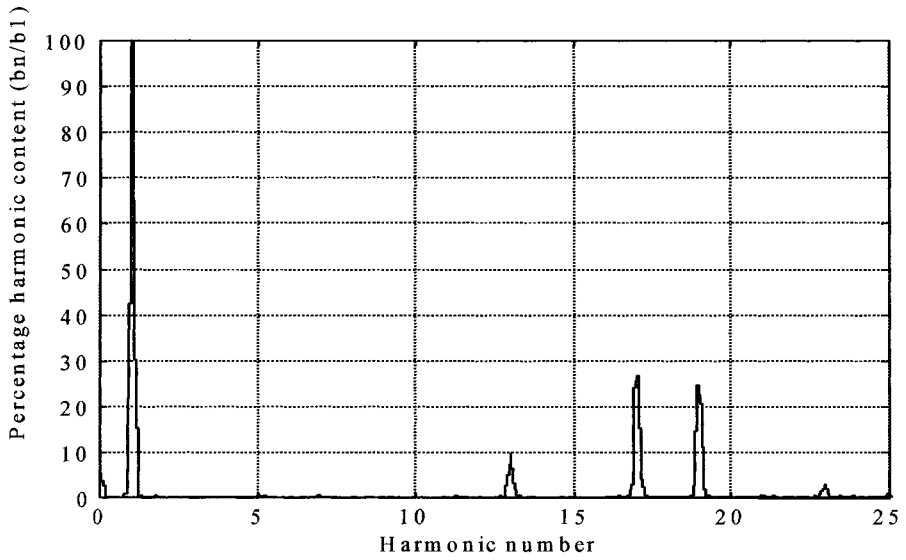


(b) – 2-level VSI output line voltage

Figure 8.4 – Waveforms for 2-level SHEM operation for no-load conditions



(a) – 3-level VSI output phase voltage – Fourier spectrum



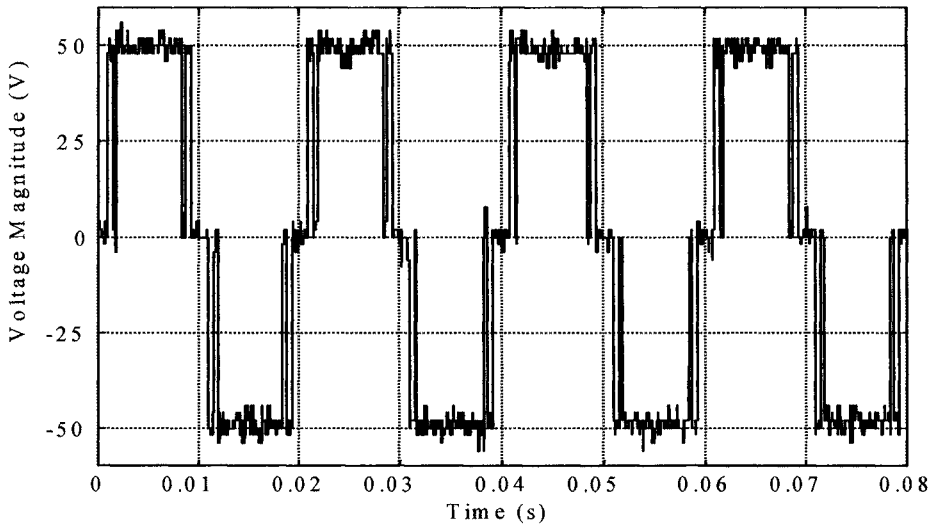
(b) – 2-level VSI output line voltage- Fourier spectrum

Figure 8.5 – Fourier Spectra's for SHEM operation for no-load conditions

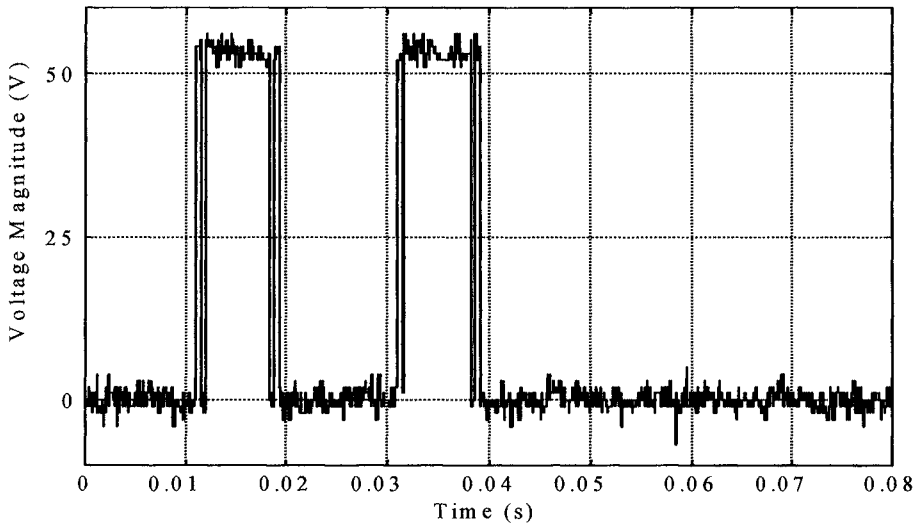
Harmonic Number	3-level SHEM (Lab model)	3-level SHEM (Theoretical)	2-level SHEM (Lab model)	2-level SHEM (Theoretical)
1	100	100	100	100
5	0	0	0	0
7	0	0	0	0
11	0	0	0	0
13	7.39	7.64	9.77	10.549
17	11.895	12.60	26.64	29.304
19	4.21	3.38	24.67	25.173
23	11.837	12.3	2.98	3.312
25	10.015	9.01	0.95	0.337

Table 8.1 – Line Voltage Harmonic Component % Values – No Load

The sequential DPPS adaptive control strategy was then tested. To demonstrate the sequential control operation, a short-circuit fault is simulated to device S_{R2}. Referring to the proposed adaptive control schemes as described in Chapter 6, in the event of S_{R2} failing short-circuit the topology should maintain uninterrupted 3-level SHEM operation by sequential firing control of $DPPS_{R1}$. In the event of such a fault the control scheme initially fails safe with a 'zero' voltage condition for one deadband period. The resultant voltage stresses to the DPPS device and remaining 'healthy' switching devices in the phase-limb can be observed. Figure 8.6a shows the 3-level SHEM output phase voltage with a fault applied at approximately t = 0.04 S. Observation of Figure 8.6b shows the short circuit fault applied to S_{R2}, when V_{CE} forward blocking voltage drops to about zero as the device fails.



(a) – 3-level VSI output phase voltage – fault applied to S_{R2} - adaptive sequential DPPS control maintains 3-level SHEM



(b) – Normal and device short-circuit measured V_{CE} for S_{R2}

Figure 8.6 – Waveforms for 3-level SHEM operation with adaptive DPPS control applied for S_{R2} short-circuit

The waveform for $DPPS_{R1}$ V_{CE}, shown in Figure 8.7, illustrates the forward and reverse voltage blocking requirements of this device under normal and abnormal operating conditions. As the DPPS devices were implemented in the experimental model with a series-connected diode to provide the required reverse blocking characteristic, the voltage stress waveform is measured for the V_{CE} of the complete unit. Before the fault is applied, the DPPS device unit prevents breakdown by forward bias blocking in the positive half-cycle of the output voltage. After the fault is applied the sequential control is apparent as the DPPS unit now opens the potential fault discharge loop, as illustrated by the additional reverse bias blocking voltage stress.

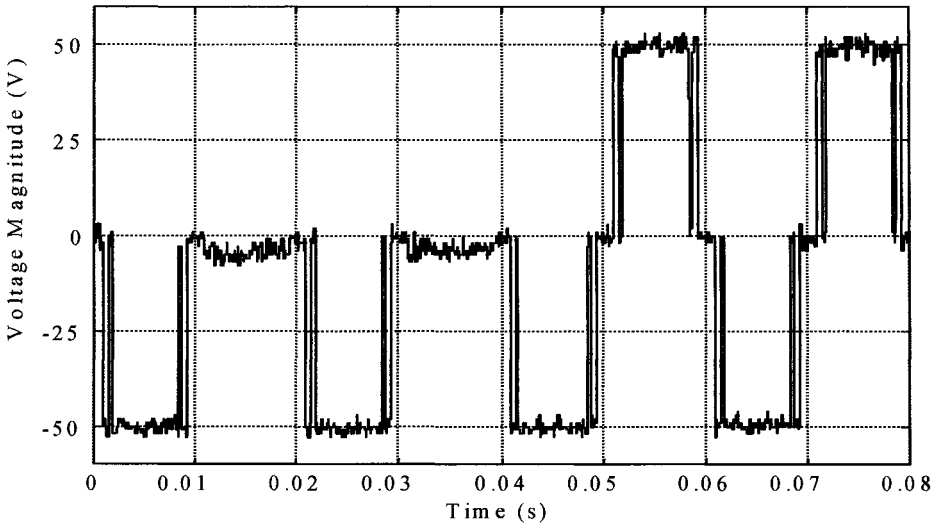
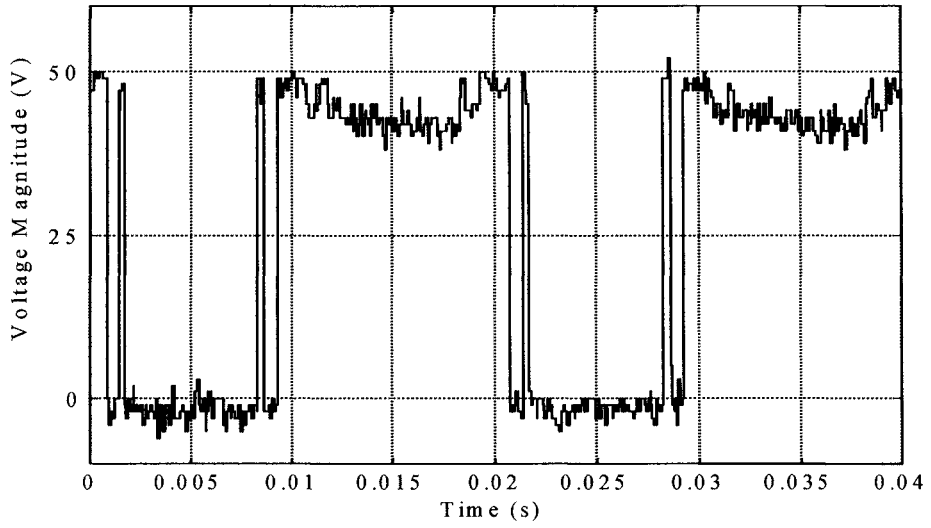
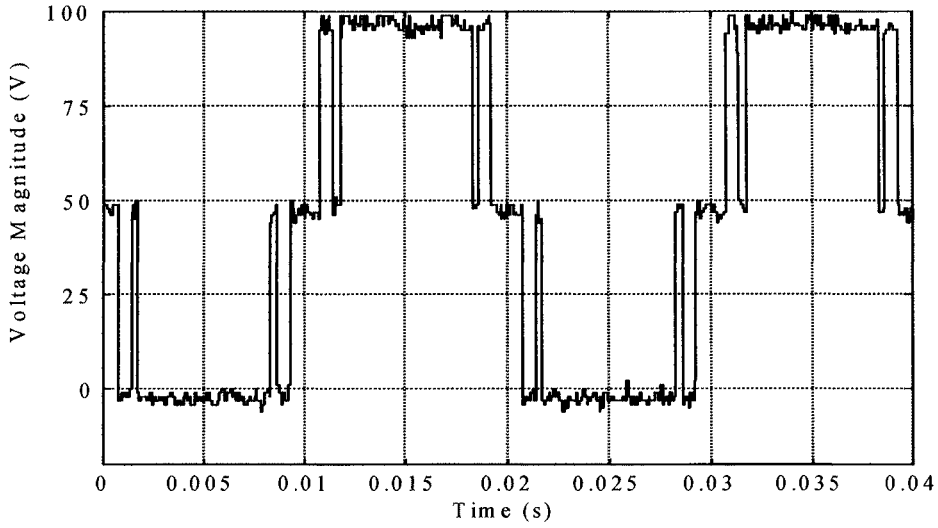


Figure 8.7 – Waveform of measured $DPPS_{R1}$ V_{CE} before and after device S_{R2} short-circuit fault

The voltage stress to device S_{R1} during normal operation and in the event of S_{R2} failing short-circuit, the system operating with the appropriate DPPS sequential control scheme, is illustrated in Figure 8.8. Observation of the measured S_{R1} V_{CE} shows that under abnormal operating conditions the S_{R1} device must be rated suitably to withstand twice the normal operation forward blocking voltage.



(a) – Waveform of S_{R1} V_{CE} before device S_{R2} fails short-circuit



(b) – Waveform of S_{R1} V_{CE} after device S_{R2} fails short-circuit

Figure 8.8 – Waveforms of measured S_{R1} V_{CE}

The adaptive control operation reverting to a 2-level SHEM strategy in the event of S_{R1} failing short-circuit is illustrated in Figure 8.9. The voltage stress on the remaining 'healthy' device in the upper leg of the phase-limb (S_{R2}) can be observed from Figure 8.10.

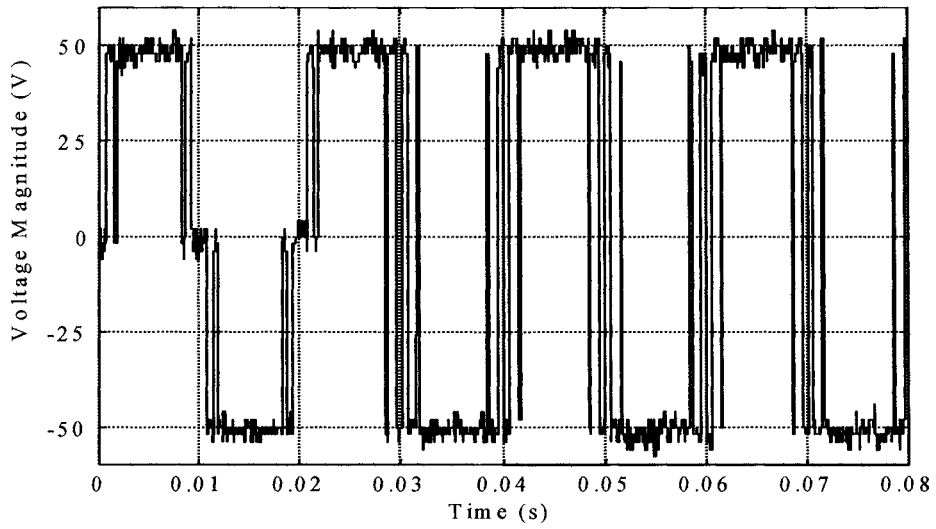


Figure 8.9 – Output phase voltage illustrating 3-level to 2-level SHEM adaptive switching control

The results of these no-load tests illustrate the importance for suitably rating the devices within the phase-limb, to maintain continual performance in the event of a device short-circuit fault. These observations will be further discussed at the end of this Chapter.

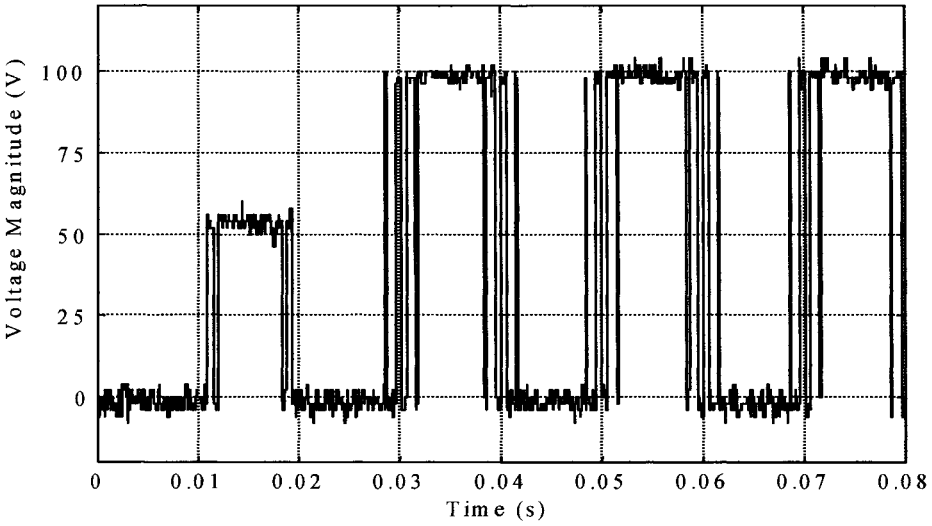


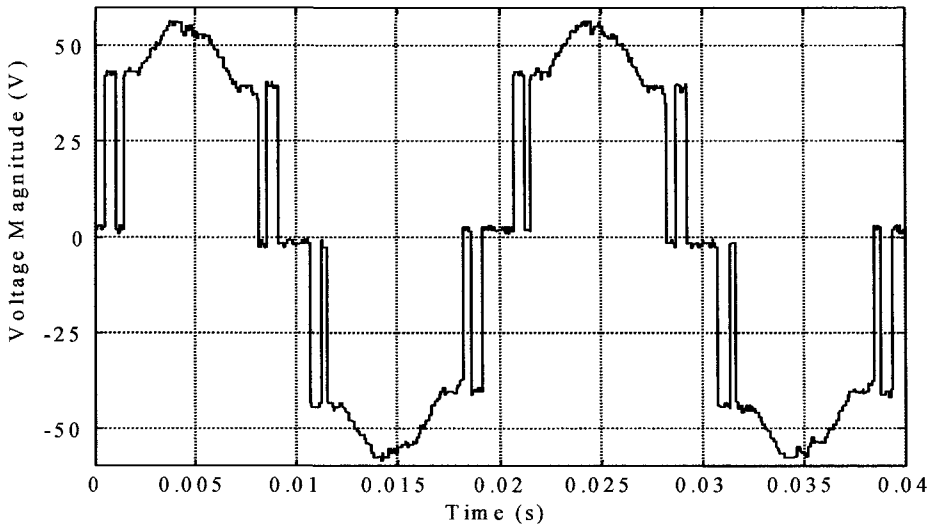
Figure 8.10 – Waveforms of S_{R2} V_{CE} before and after S_{R1} fails

8.2.2 THREE-LEVEL VSI PERFORMANCE WITH INDUCTIVE LOAD BANK

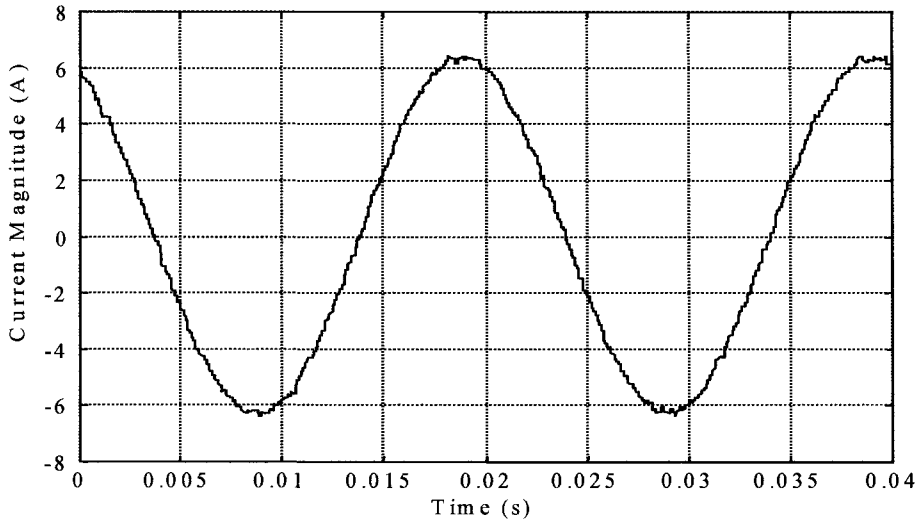
The overall system performance of the adaptive 3-level VSI topology was tested with a 4 A inductive load. This mode of operation represents the experimental model operating as an ASVC in the leading mode of VAr compensation. Again 3-angle SHEM switching strategies were applied to maintain the harmonic performance. With the d.c. link steady-state voltage at 100 V and the reference sinewave set to 50 Hz the inductive load was applied.

The output phase voltage and line current produced by the 3-level VSI for normal operating conditions are shown in Figure 8.11. Compared with the no-load condition, the measured voltage waveform shows the effects of the conduction volt-drop of the semiconductor devices and the ripple in the d.c. side capacitor voltage. Observation of the line current illustrates a phase shift (more than 90°) due to the large resistance of the inductive load bank. The 90° phase shift of the current leading the phase voltage indicates operation of the 3-level DPPSC-MLI as a VAr compensator. The output line voltage and corresponding harmonic spectrum produced by the system are given in Figure 8.12.

As an open-loop system was applied, the problem of balancing the d.c. capacitor voltages was minimised by applying a resistive potential divider as illustrated in Figure 8.2. With the d.c. link maintained at a steady-state 100 V, the upper and lower capacitor voltages are shown in Figure 8.13. As can be observed from Figure 8.14, the inductive load resulted in a large d.c. voltage ripple on the upper and lower capacitors. The current from the d.c. link capacitor bank was also measured for the SHEM switching strategy. This is shown for $+i_{cap}$ and $-i_{cap}$ (see Figure 8.2), in Figure 8.15. The 3rd harmonic frequency, developed in the voltage and current across the upper and lower capacitors, is resultant from loaded operating conditions and the existence of 2nd and 4th harmonic components in the positive and negative half cycle switching functions. This is analysed in Chapter 9, together with the phenomena of 5th and 7th harmonic remodulation in the output voltage spectrum.

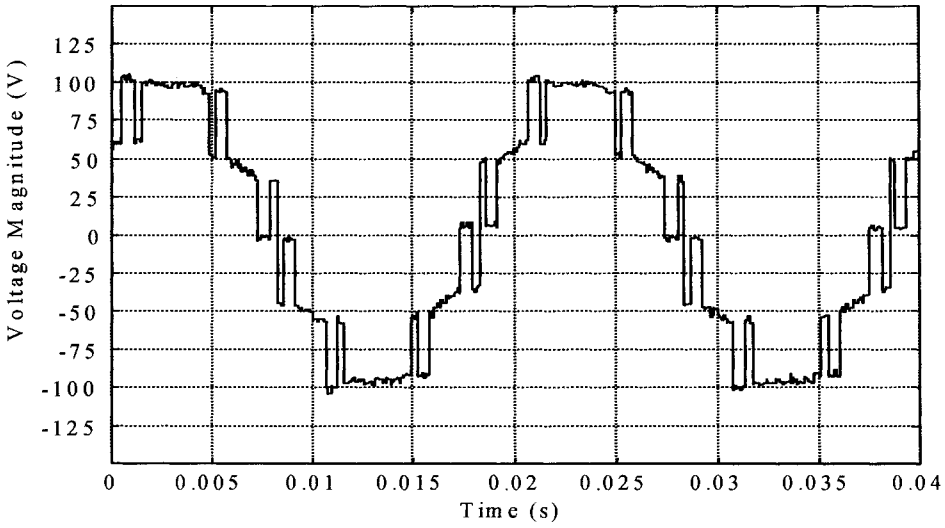


(a) – 3-level SHEM output phase voltage

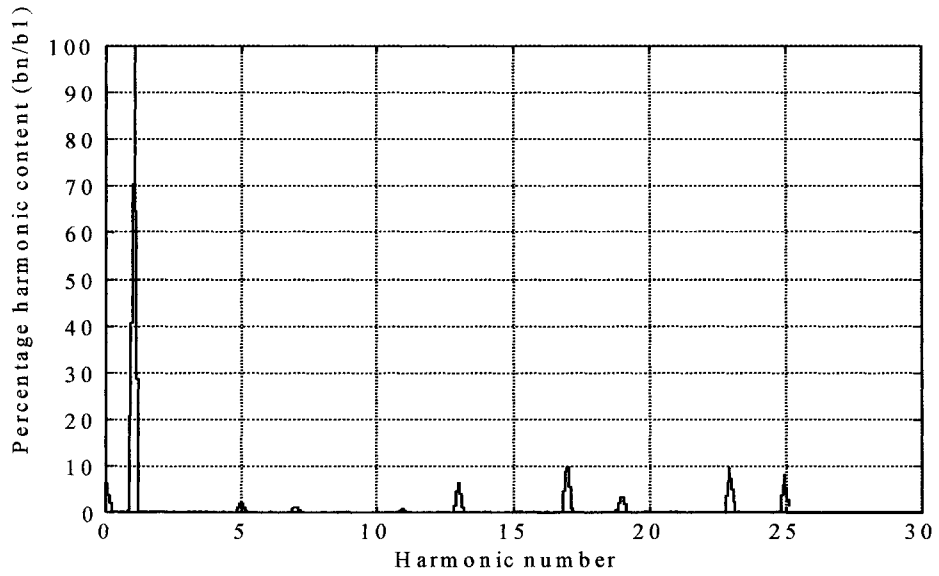


(b) – 3-level SHEM output line current

Figure 8.11 – Waveforms for 3-level SHEM VSI with an inductive load

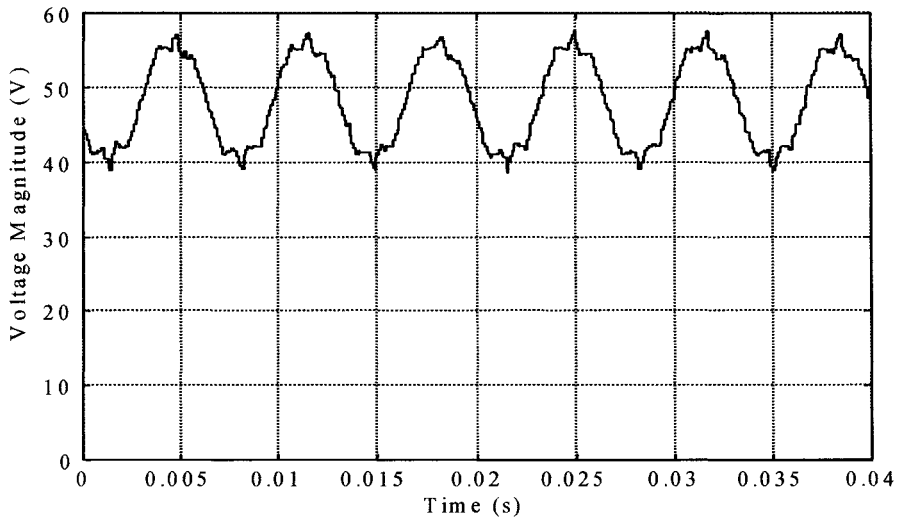


(a) – 3-level SHEM output line voltage

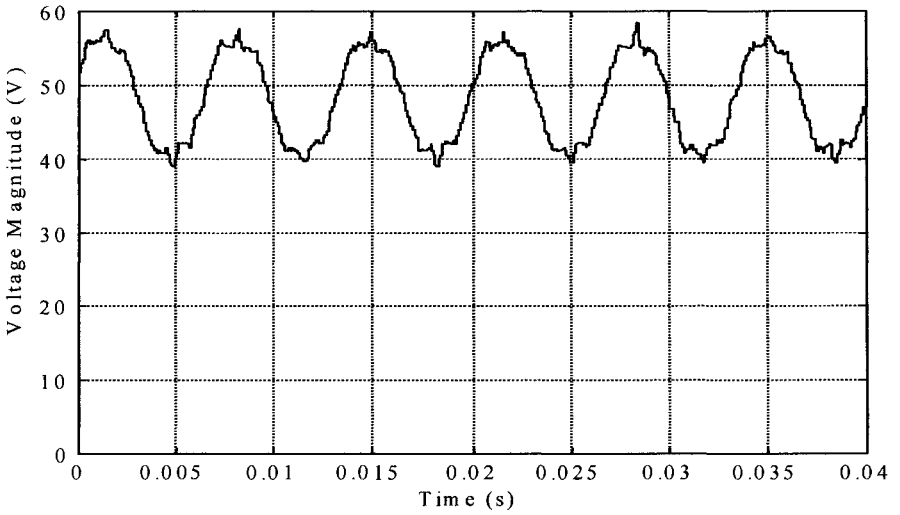


(b) – 3-level SHEM output line voltage Harmonic Spectrum

Figure 8.12 – Waveforms for 3-level SHEM VSI with an inductive load

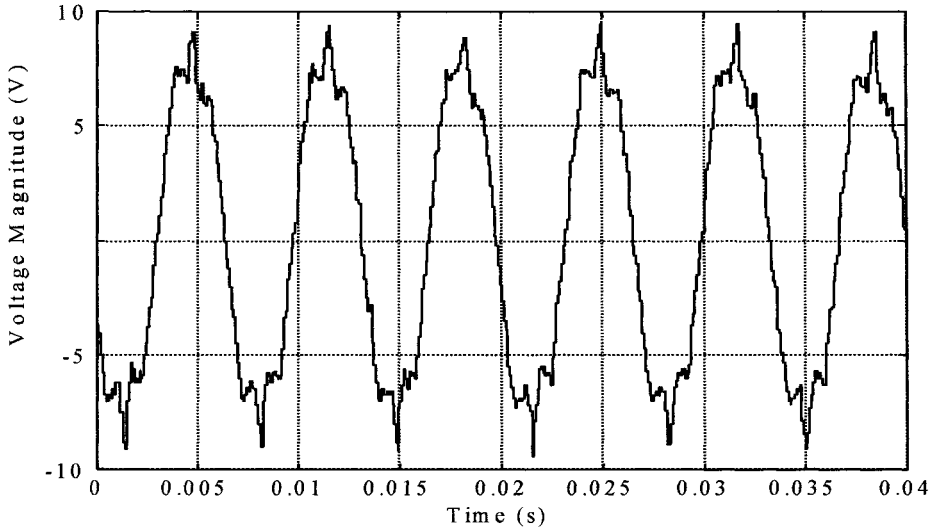


(a) – DC voltage on upper capacitor ($+v_{cap}$)

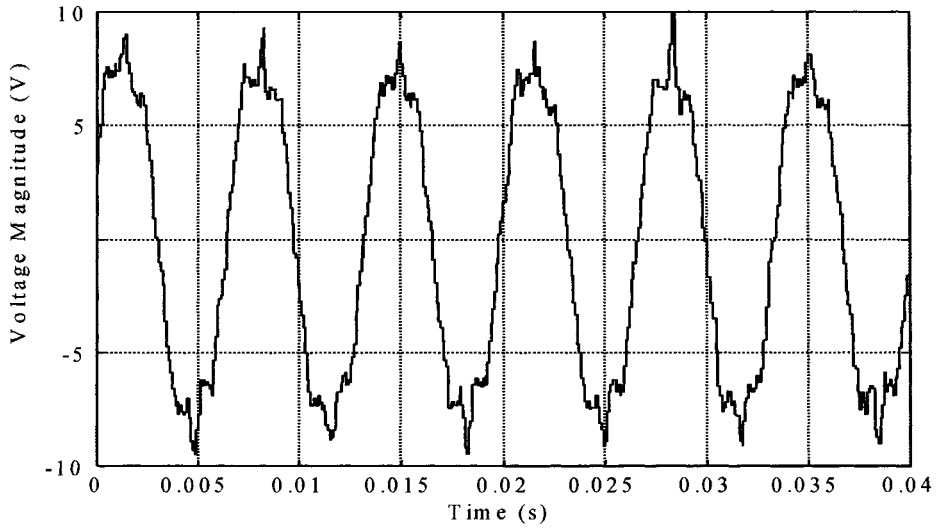


(b) – DC voltage on lower capacitor ($-v_{cap}$)

Figure 8.13 – Waveforms for 3-level SHEM VSI with an inductive load

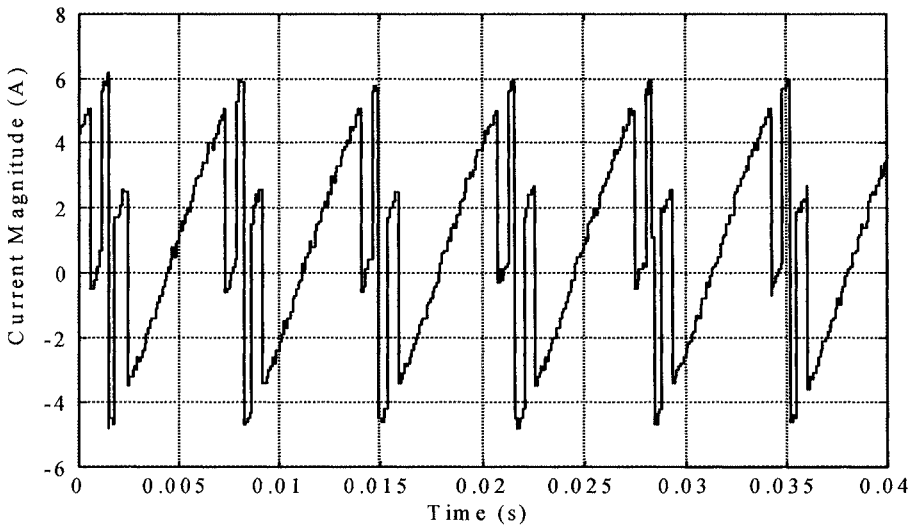


(a) – DC voltage ripple on upper capacitor

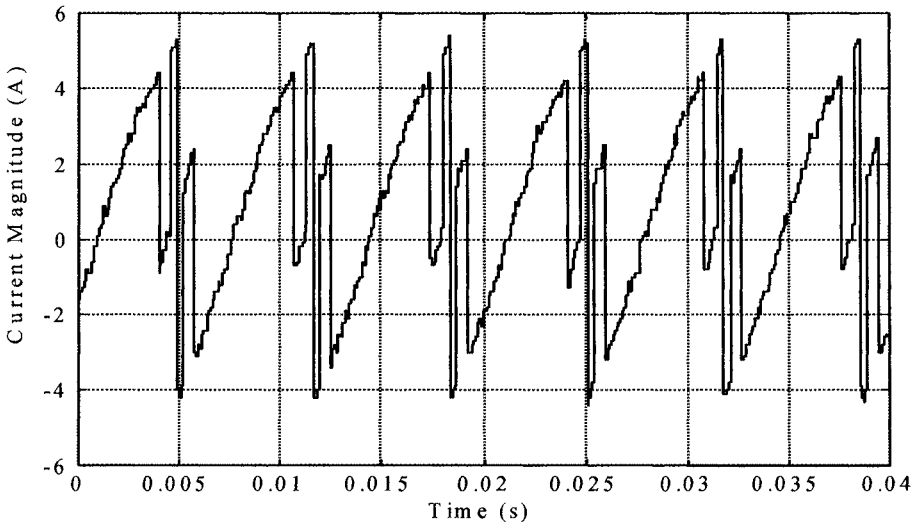


(b) – DC voltage ripple on lower capacitor

Figure 8.14 – Waveforms for 3-level SHEM VSI with an inductive load



(a) – Capacitor current ($+i_{cap}$)

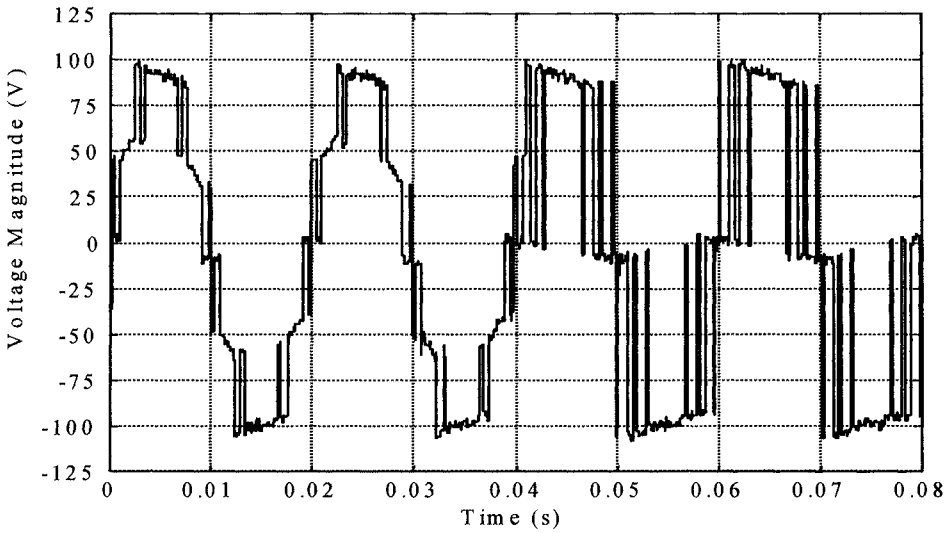


(b) – Capacitor current ($-i_{cap}$)

Figure 8.15 – Waveforms for 3-level SHEM VSI with an inductive load

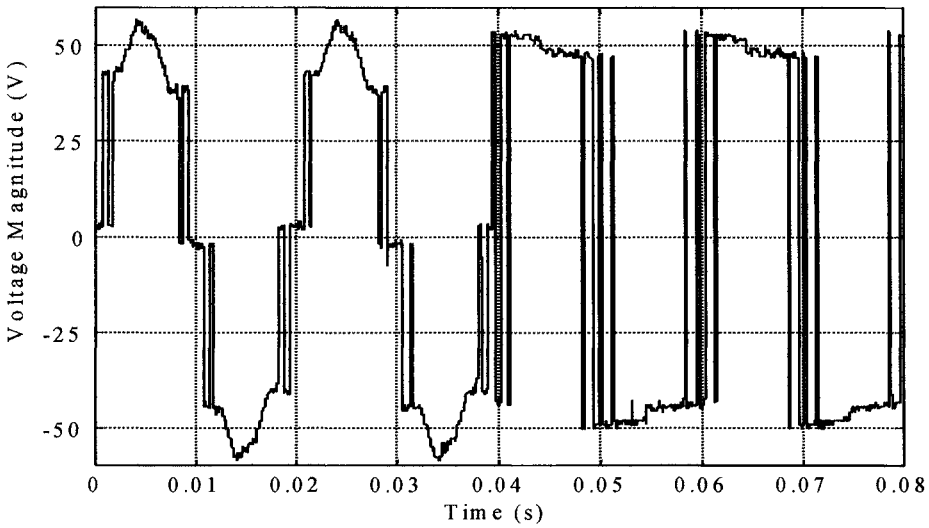
To demonstrate the performance of the adaptive 3-level VSI topology, with a 4 A inductive load, under abnormal operating conditions a short-circuit fault was simulated to device S_{R1}. As with the previous no-load condition tests, the adaptive controller reverts to a bi-polar switching strategy to maintain the harmonic performance and the fundamental voltage. As the recovery of harmonics has already been verified in section 8.2.1, in this test case the continual output power performance is investigated. It is accepted that, due to the accuracy of the off-line calculated SHEM angles, the fundamental voltage magnitude may slightly differ in the event of changing modulation strategies resulting in a small difference in the output line current. However, it is important to maintain the output throughout the modulation transient, as demonstrated by the results presented below.

Figure 8.16 illustrates the output line voltage with a short-circuit fault applied to S_{R1}. The resultant output phase voltage and line current, shown in Figure 8.17, demonstrate the uninterrupted ASVC characteristic performance provided by the adaptive strategy in the event of such a fault.

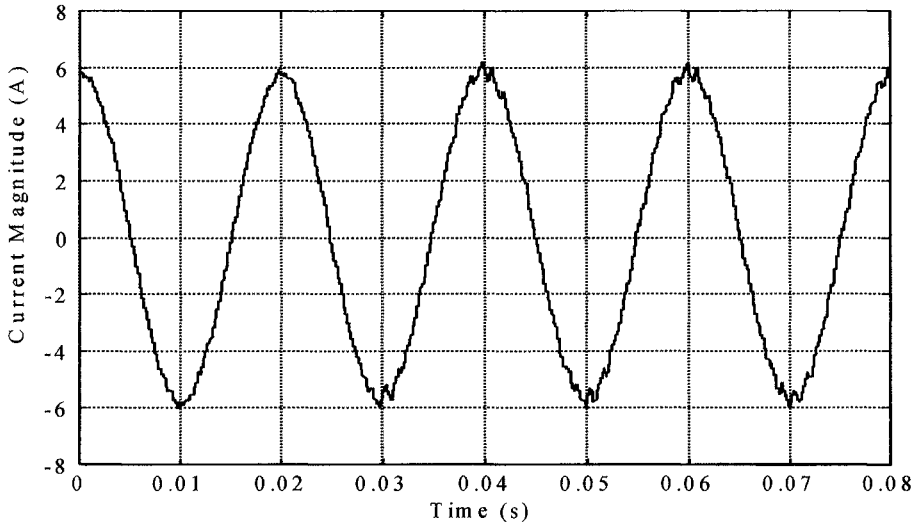


Adaptive 3-level VSI output line voltage

Figure 8.16 – Waveforms illustrating transient from normal to abnormal operating conditions with an inductive load



(a) – Adaptive 3-level VSI output phase voltage



(b) – Adaptive 3-level VSI output line current

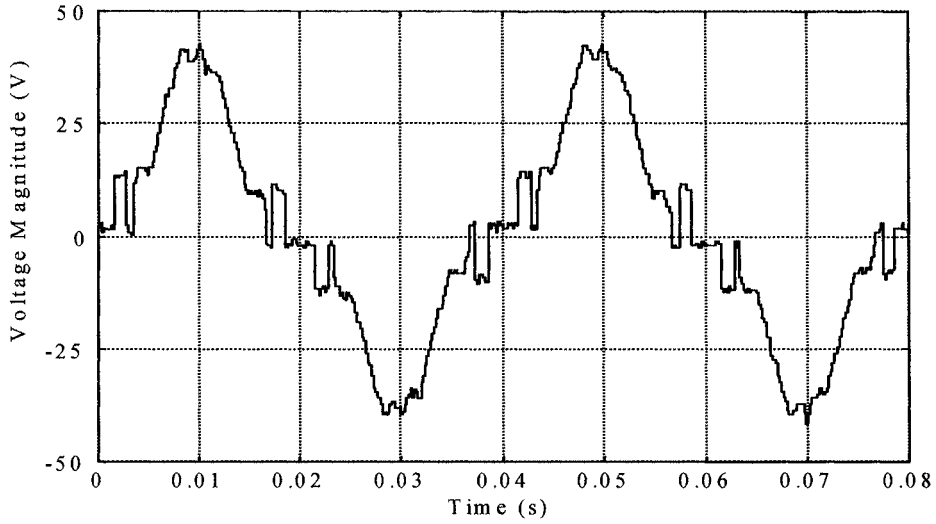
Figure 8.17 – Waveforms illustrating transient from normal to abnormal operating conditions with an inductive load

8.2.3 HARMONIC PERFORMANCE OF 3-LEVEL VSI WITH INDUCTIVE LOAD

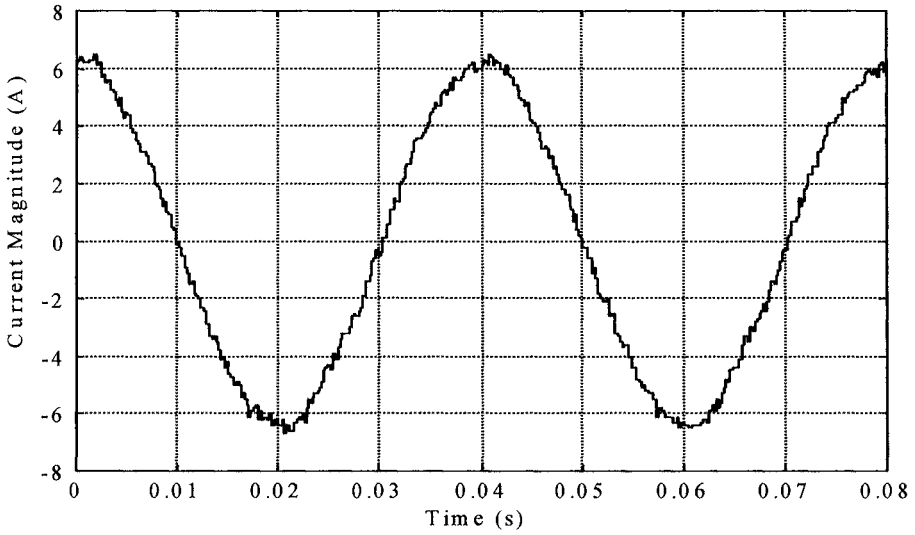
The results presented in section 8.2.1 illustrate that for 'floating' no-load operating conditions the 3-level VSI SHEM switching strategy eliminates the 5^{th}, 7^{th} and 11^{th} harmonics in the output voltage spectrum. However, observation of the harmonic spectrum obtained for the 3-level output line voltage with a 4 A inductive load (at 50 Hz) indicates that the elimination of these low-order harmonics is not fully achieved.

To investigate the effect of the load upon the elimination of selected harmonics, a larger inductive load was required. Unfortunately the ratings of the available load bank could only provide 4 A for the available inverter output line voltage. Therefore, to further demonstrate the effect of increasing the load, with the reference frequency was set to 25 Hz and the d.c. link steady-state voltage set to 50 V the load effect on the d.c. capacitor at each level is effectively doubled. The frequency of the harmonic current absorbed by the capacitors is halved. Therefore, the same amount of harmonic current will cause twice as much voltage ripple across the capacitors. In the following, the system harmonic performance is investigated under normal 3-level SHEM VSI operating conditions, as it was observed that the above phenomenon was characteristic to the multi-level VSI.

The output phase voltage and line current produced by the system operated at 25Hz are shown in Figure 8.18. The resultant line voltage waveform and its harmonic spectrum are shown in Figure 8.19. Observation of the phase and line voltage waveforms shows a large distortion in comparison to the ideal theoretical waveforms. This is also apparent when observing the residual low-order harmonic components in the resultant spectrum. The effect of the increased load upon the d.c. capacitor ripple is illustrated in Figure 8.20. As shown, the magnitude of the ripple component in both the upper and lower capacitors has almost doubled, as compared to Figure 8.14. The resultant capacitor currents are given in Figure 8.21 for $+i_{cap}$ and $-i_{cap}$. Significant 3^{rd} harmonics are observed.

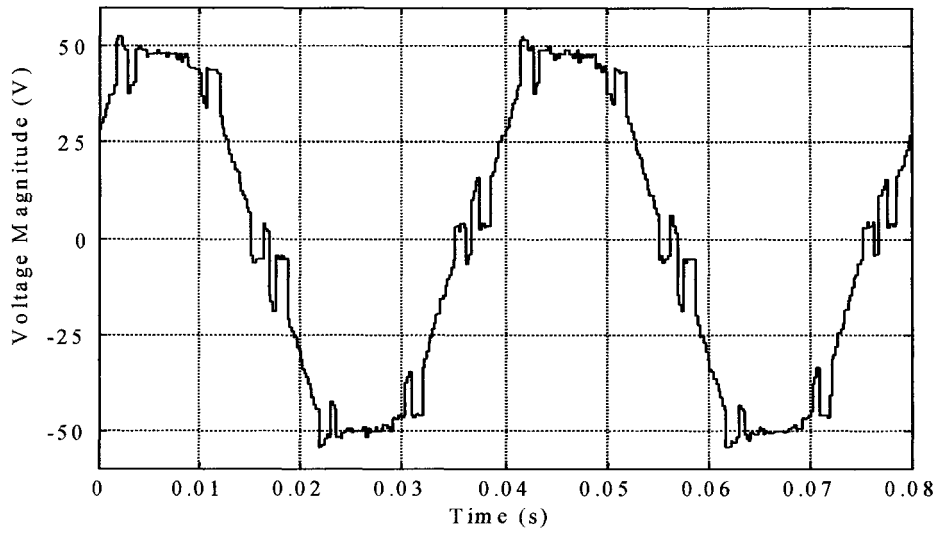


(a) – 3-level SHEM output phase voltage

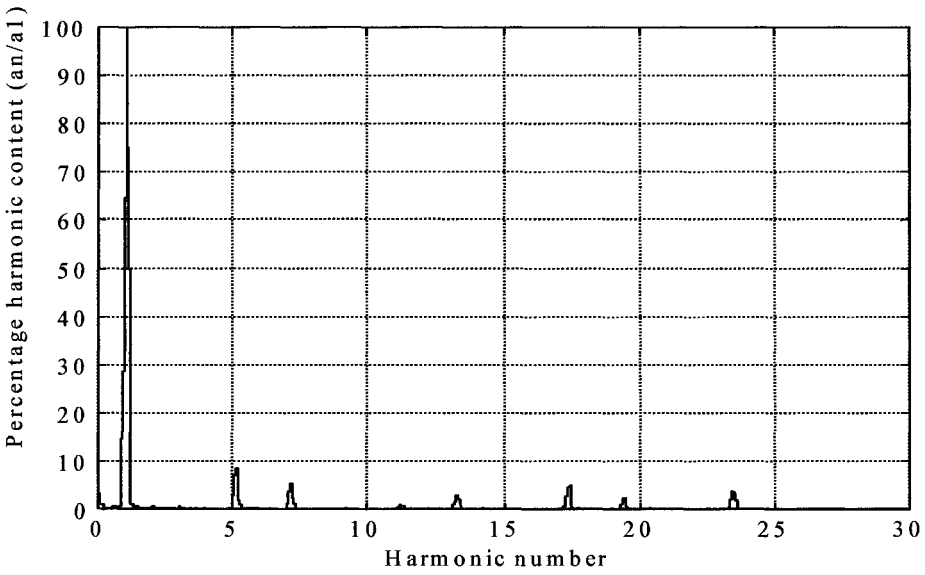


(b) – 3-level SHEM output line current

Figure 8.18 – Waveforms for 3-level SHEM VSI operated at 25 Hz

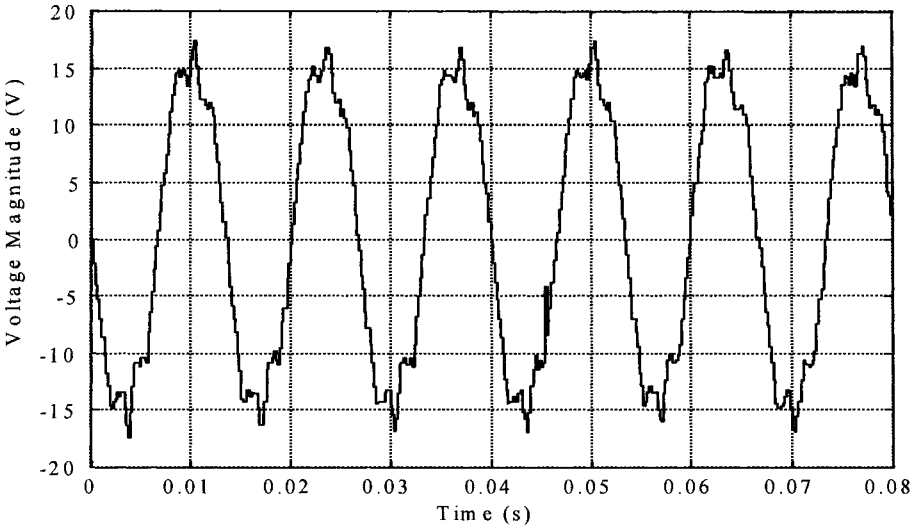


(a) – 3-level SHEM output line voltage

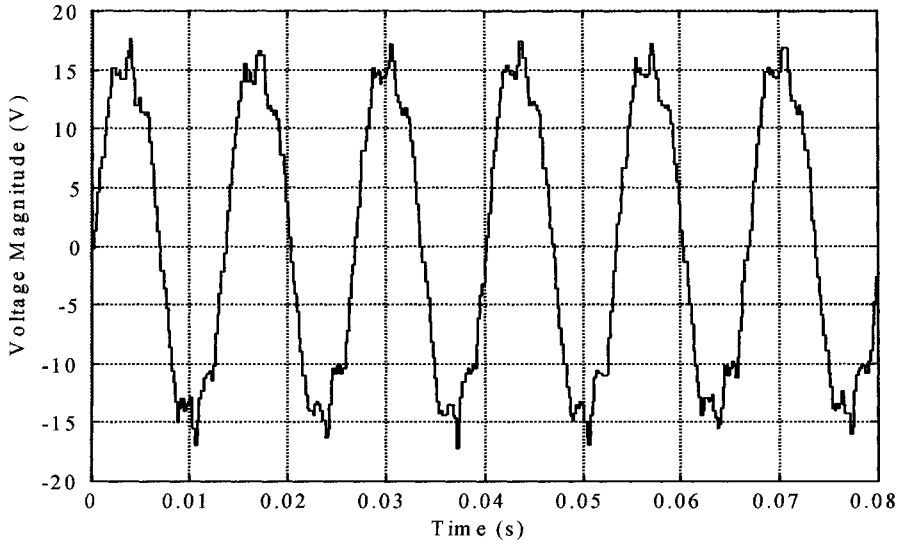


(b) – 3-level SHEM output line voltage Harmonic Spectrum

Figure 8.19 – Waveforms for 3-level SHEM VSI operated at 25 Hz

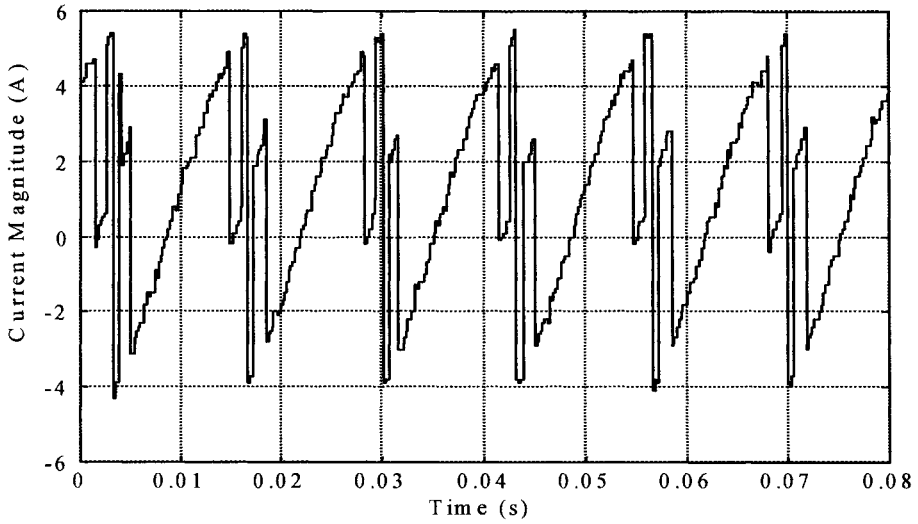


(a) – DC voltage ripple on upper capacitor ($+v_{cap}$)

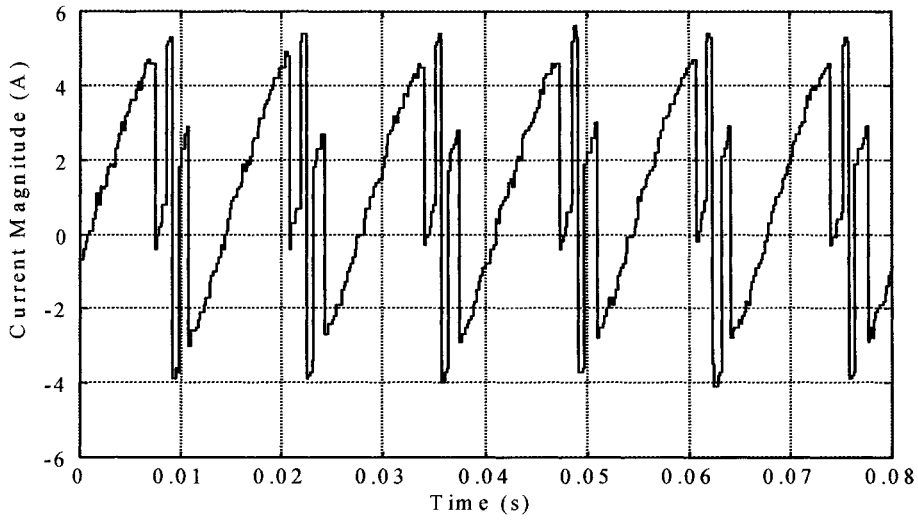


(b) – DC voltage ripple on lower capacitor ($-v_{cap}$)

Figure 8.20 – Waveforms for 3-level SHEM VSI operated at 25 Hz



(a) – Capacitor current ($+i_{cap}$)



(b) – Capacitor current ($-i_{cap}$)

Figure 8.21 – Waveforms for 3-level SHEM VSI operated at 25 Hz

With the 3-level VSI operated at 50 Hz and 25 Hz the percentage values of the harmonic component are calculated and presented in Table 8.2. The results illustrate the failure to eliminate the low-order harmonic components targeted by the 3-level SHEM strategy. Observation of the table shows a decline in the harmonic performance of the system as the load increases. The mechanism will be further analysed and solutions provided in the next Chapter

Harmonic Number	**3-level SHEM (Lab model – 50Hz)**	**3-level SHEM (Lab model – 25Hz)**	**3-level SHEM (Theoretical)**
1	100	100	100
5	2.22	8.611	0
7	1.38	5.55	0
11	0.9	1	0
13	6.319	3.11	7.64

Table 8.2 – Line Voltage Harmonic Component % Values – Inductive Load

8.3 Operating Performance of the 3-level DPPSC-MLI based ASVC (Test 2)

As the 3-level DPPSC-MLI experimental model was developed with an open-loop adaptive switching controller, the conventional method of operating it as an ASVC cannot be implemented. Typically, the ASVC system would be developed with a phase locked loop (PLL) where the voltage reference is derived from the power network. Also a closed loop reactive power PI controller is required to provide phase angle control of the reference signal, dependant upon the reactive compensation requirements. Referring back to basic operational principles of the ASVC, reactive power flow (in either direction) is produced through magnitude control of the inverter output voltages with respect to their corresponding a.c. system voltages. However, for this flow of reactive power to occur the inverter output voltages must be controlled to be in phase with the a.c. system voltages.

The digital controller of the experimental model generates a high accuracy interpolated reference sinewave for the SHEM angles. As a PLL was not implemented into the control scheme, a different test procedure was implemented to observe the reactive power compensation. Again referring back to the operational characteristics of the ASVC, the VSI implementation of the reactive power compensation is a solid-state equivalent of the synchronous condenser. Therefore, reactive power compensation is demonstrated by using the 3-level VSI experimental model to drive a three-phase synchronous machine.

The ASVC operation was demonstrated using a generalised machine demonstration set operated as a synchronous machine, which was connected to the adaptive 3-level inverter as shown in Figure 8.22. The machine could be synchronised to the output voltage frequency of the 3-level VSI hardware model. The flow of reactive power in both directions could be produced by over and under excitation of the synchronous machine. Therefore, although the characteristic flow of reactive power would be reversed, compared to the standard ASVC operation, the leading and lagging modes of compensation can be demonstrated. Initially, the internal dynamic reactance characteristics of the

machine were tested to ensure suitability of the excitation procedure. In order to demonstrate the flow of ±1.2 kVAr, the windings of the machine must provide a suitably low inductance such that the varying excitation can be demonstrated whilst maintaining the machine in a stable operation. The dynamic tests indicated an inductive reactance of 12 Ω; therefore to obtain a reactive current flow of ±3 A the machine must be over-excited to 266 V and under-excited to 194 V.

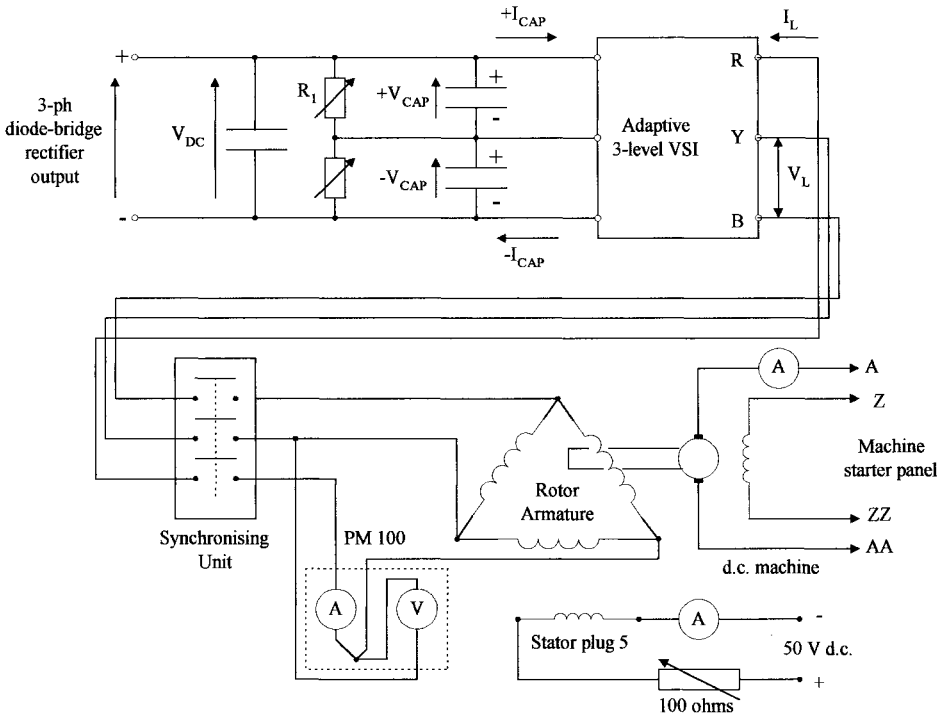
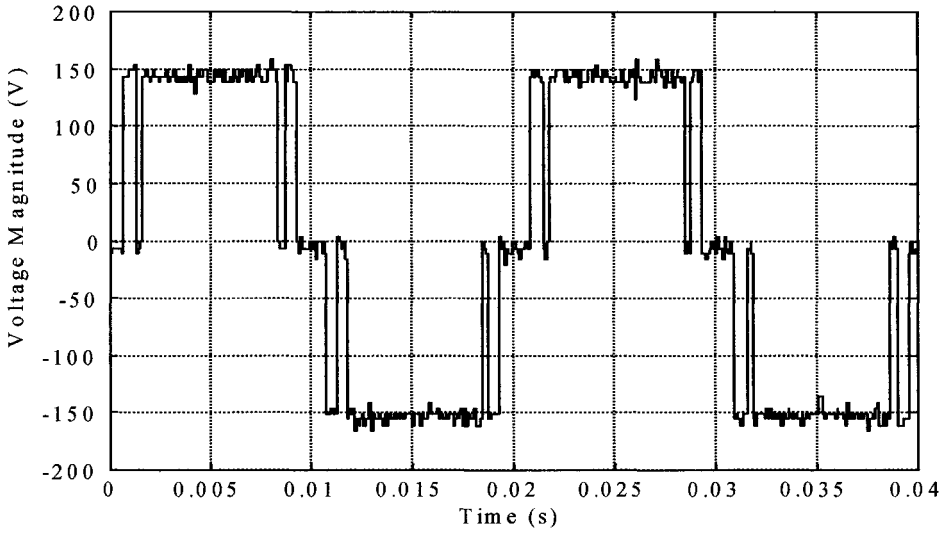
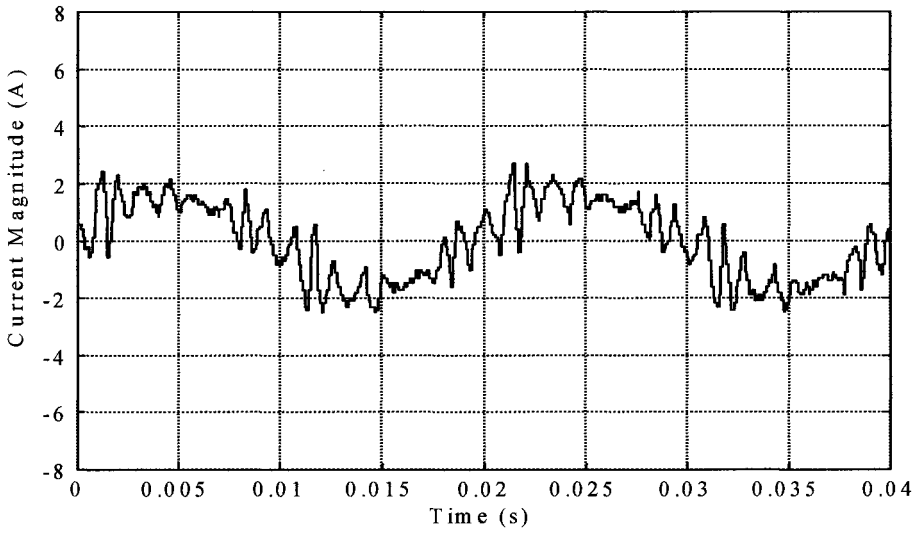


Figure 8.22 – Test Circuit for Generalised Machine and Adaptive VSI system

With the 3-level VSI output line voltage set at 230 V at 50 Hz, the synchronous machine was driven by a d.c. machine at 3000 rev/min and synchronised to the output voltage of the experimental ASVC model. Utilising a SHEM switching strategy the characteristic operation of an ASVC was observed with the 3-level VSI. The system was tested to demonstrate 'floating' conditions, lagging and leading modes of ASVC operation. The results obtained are shown for output phase voltage and line currents in Figures 8.23, 8.24 and 8.25 respectively. Observation of the d.c. voltage on the upper capacitor, shown in Figure 8.26, illustrates the characteristic of increasing the capacitor voltage for the ASVC in leading mode of operation.

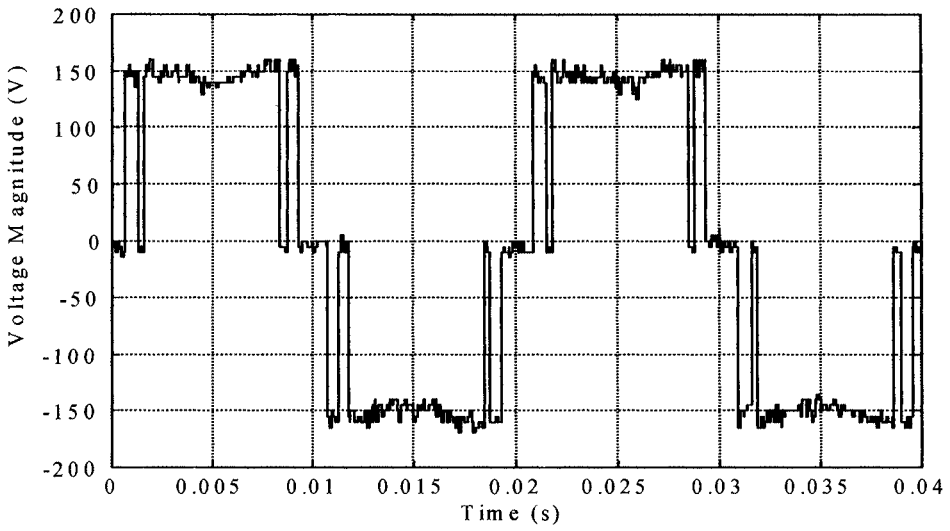


(a) – ASVC output phase voltage

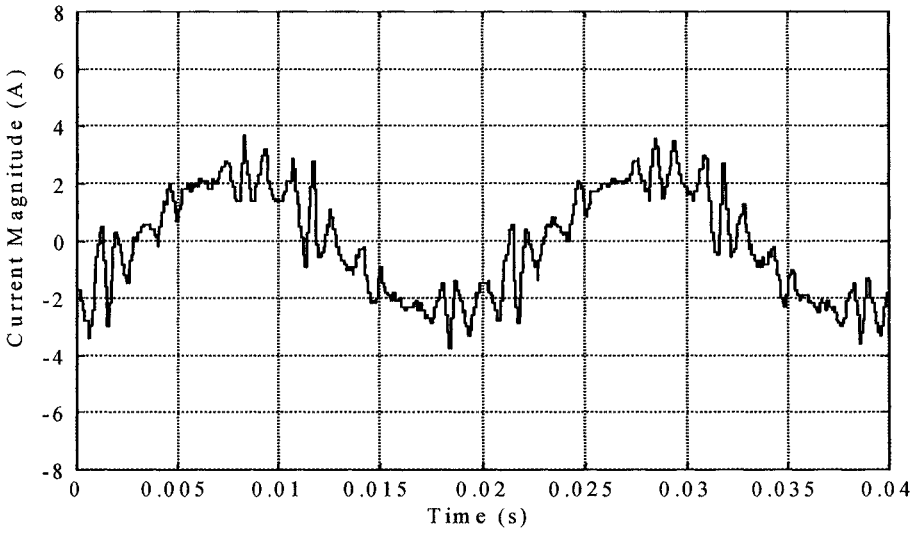


(b) – ASVC output line current

Figure 8.23 – Waveforms for floating operation of the ASVC

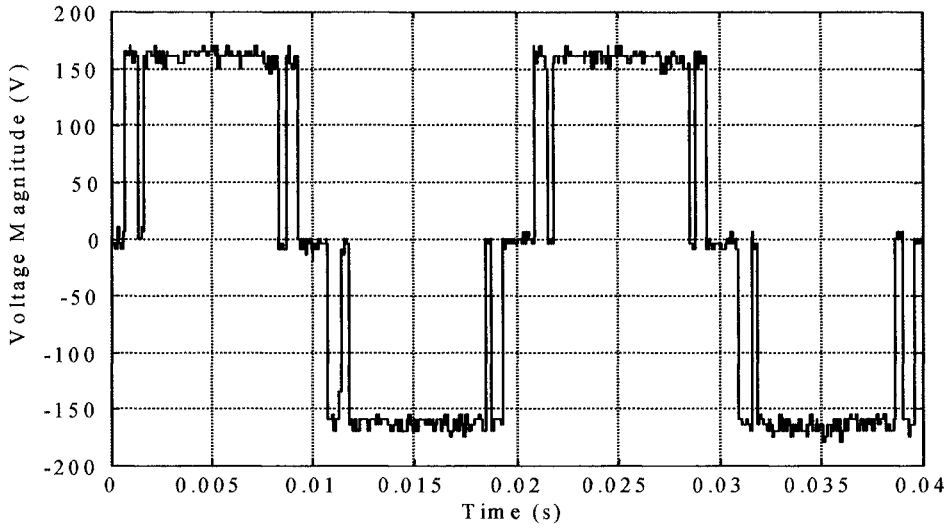


(a) – ASVC output phase voltage – lagging mode

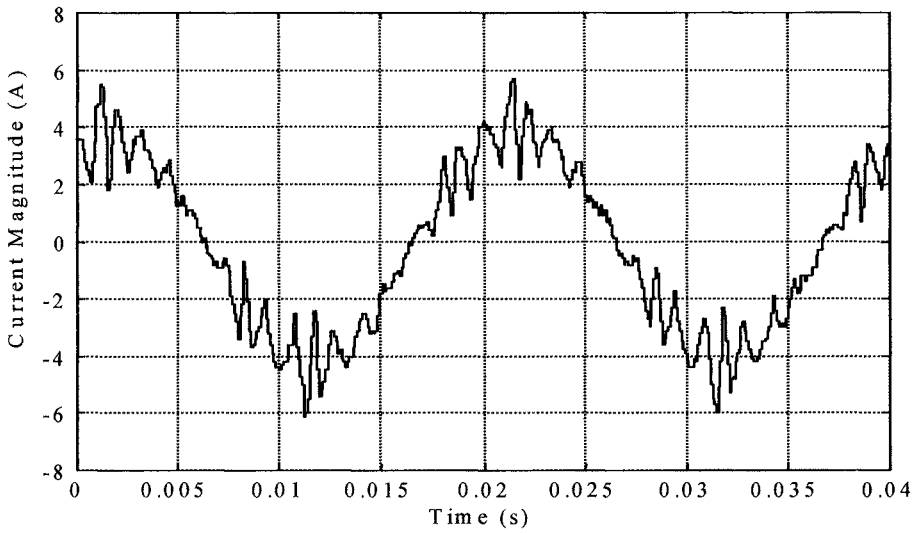


(b) – ASVC output line current – lagging mode

Figure 8.24 – Waveforms for lagging operation of the ASVC

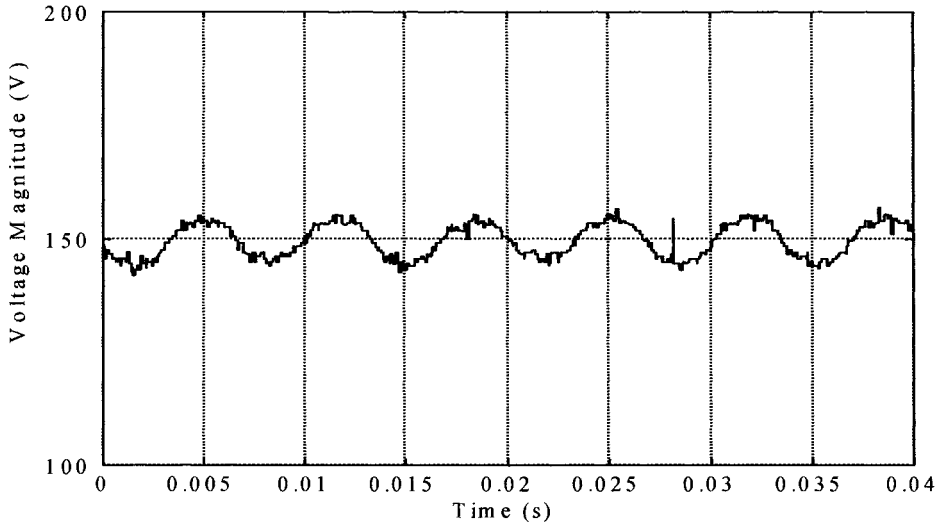


(a) – ASVC output phase voltage – leading mode

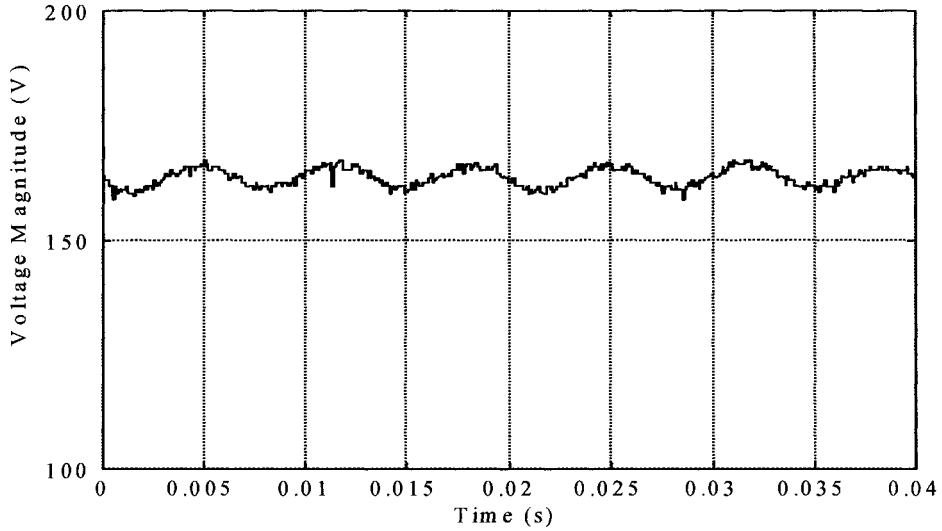


(b) – ASVC output line current – leading mode

Figure 8.25 – Waveforms for leading operation of the ASVC



(a) – DC capacitor voltage ($+v_{cap}$) – lagging mode



(b) – DC capacitor voltage ($+v_{cap}$) – leading mode

Figure 8.26 – Waveforms for floating operation ASVC

8.4 SUMMARY OF THE EXPERIMENTAL MODEL PERFORMANCE

The adaptive 3-level VSI experimental model was used to investigate the real-time performance of the proposed topology. Utilising the adaptive DPPS digital control scheme implementing a 3-level to 2-level SHEM switching strategy the system was analysed with respect to improved inverter robustness, in the event of a short-circuit device fault, and suitability for the Advanced Static VAr Compensation application.

A no-load test was implemented to observe the harmonic performance of the SHEM strategy implemented into the digital controller. The results obtained indicate a suitable accurate system performance. Therefore the use of a highly interpolated digitally generated sinewave for angular reference in the DSP switching controller proves to be a methodology suitable for the ASVC application.

Maintaining no-load operation conditions, the improved robustness of the proposed adaptive 3-level DPPSC-MLI topology was demonstrated. Figure 8.4 illustrates the switching controller adapting to a 2-level SHEM strategy in the event of a short-circuit fault to device S_{R1}. Observation of the output line voltage spectra, given in Figure 8.5, for normal (3-level SHEM) and abnormal (2-level SHEM) operation, shows a good low-order harmonic elimination in both operational modes. Thus, providing a fair system harmonic performance to maintain continual operation.

To investigate the sequential DPPS control strategy, a short-circuit fault was applied to device S_{R2}. It should be noted that with the conventional 3-level DCMLI topology a fault of this type would result in a system shutdown. However, the adaptive 3-level VSI and adaptive DPPS controller proposed in this work provide an uninterrupted 3-level SHEM scheme throughout the fault. The experimental observations on the resultant voltage stresses on devices in the phase-limb operating with a device faulty were as predicted.

As a 3-level topology is presented, maintaining continual operation in the event of a fault results in twice the voltage stress applied across the device remaining in the upper or lower phase-limb. This is true for both adaptive control cases. Implementation of the DPPS scheme into higher-level VSI topologies would result in relatively less increases in voltage stresses across the devices in the event of implementing an adaptive scheme due to device faults.

The operation of the system with an inductive load was then tested. Obtaining results as specified in the experimental layout given in Figure 8.2, the hardware model represented an ASVC operating in the steady-state leading mode of compensation. Observation of the output phase voltage and current, Figures 8.11a and 8.11b respectively, illustrate that the 3-level is providing leading reactive power to the system load.

However, observation of the phase and line voltages shows a large distortion with respect to the ideal no-load voltage waveforms. This is also shown in the line voltage harmonic spectrum where the 5^{th} and 7^{th} harmonic components, measured at 2.22% and 1.38% with respect to the fundamental, are no longer eliminated. Measurements of the upper and lower capacitor voltages show clearly that a 3^{rd} harmonic voltage ripple component is generated when the 3-level VSI is being operated under load conditions. This ripple is resultant from large excursion due to harmonic absorption for the capacitor voltage at the upper and lower levels.

To further investigate the effect of the loading operating point on the harmonic performance of the system, operating the 3-level VSI at a reference frequency of 25 Hz effectively doubled the inductive load. The results obtained for these tests, shown in section 8.2.3, illustrate that doubling the load increases the voltage waveform distortion due to increased magnitude of ripple in the capacitor voltages. Observation of the line voltage spectra shows the 5^{th} at 8.6% and 7^{th} at 5.5%, with respect to the fundamental, illustrating the detrimental effect the load has upon the system harmonic performance. This clearly needs further investigation and 3-level modulation analysis focussing upon the a.c. to d.c. side harmonic interaction has been carried out and is given in Chapter 9.

To demonstrate the suitability of the new adaptive 3-level VSI topology for the ASVC application a further test procedure was developed. Utilising a generalised machine to synchronise to the 3-level VSI output voltage, the operational characteristics of a 3-level VSI based ASVC were obtained. Although various switching strategies were implemented for analysis, only the 3-level SHEM operation is presented in this thesis. The ASVC output phase voltage and current waveforms for 'floating', lagging and leading modes of operation are presented in Figures 8.23, 8.24 and 8.25, respectively. As the experimental model VSI was constructed without implementing a.c. side harmonic filters the resultant current is very distorted resulting from the SHEM voltage waveforms. However, the operational output current phase-shift characteristics specific to the ASVC reactive power flow compensation are observed with respect to the phase voltage.

9 DYNAMIC SHEM (DSHEM) FOR A 3-LEVEL VSI BASED ADVANCED STATIC VAR COMPENSATOR

9.1 INTRODUCTION

In most FACTS devices currently being developed, one of the major concerns is the harmonic performance of the system [62]. This thesis has presented an Advanced Static VAr Compensator (ASVC) based upon a 3-level VSI, which converts its d.c. side voltage into a 3-phase a.c. voltage in phase with the system voltage to provide an exchange of reactive power [63]. The use of Selective Harmonic Elimination Modulation (SHEM) to remove the 5^{th}, 7^{th} and 11^{th} harmonics from the a.c. side output voltage spectra of the 3-level VSI has been demonstrated both theoretically (Chapter 5) and experimentally (Chapter 8). The use of 3-level SHEM for the ASVC application has been recommended by previous studies such that passive filters can be efficiently implemented [64]. However, it has been reported in [64] that the conventional SHEM scheme cannot always eliminate the target harmonics. This phenomenon has been demonstrated with the 3-level VSI experimental model results given in Chapter 8, where the 5^{th}, 7^{th} and 11^{th} harmonic components are clearly apparent in the ASVC output voltage spectrum. It has been clearly shown that such harmonics are dependant on the system load level.

As presented in Chapter 5, the theoretical analysis normally adopted for the VSI output voltage, assumes an ideal output phase voltage waveform. Therefore, the off-line calculated SHEM switching angles are predetermined assuming a constant capacitor voltage on the d.c. side. The experimental model results presented in Chapter 8 illustrate that the capacitor voltage contains a ripple component at the 3^{rd} harmonic frequency. Observation of the experimental ASVC a.c. side output voltages shows a distorted waveform, which is different from the ideal waveform used to calculate the switching angles. To minimise the capacitor voltage ripple component a large passive capacitive element may be utilised for the d.c. link. However, in order to reduce cost and improve the dynamic speed of

response, the d.c. side capacitance is often designed to a minimal value, giving rise to a relatively large voltage ripple.

Analysis of the harmonic interaction phenomena between the a.c. and d.c. sides of the 3-level VSI based ASVC is presented in this Chapter. Using a standard mathematical representation of the VSI based ASVC, expressions for the a.c. side harmonics are derived which include the effect of the capacitor voltage ripple. Results illustrate the output voltage harmonic spectrum is dependant upon the capacitance of the upper and lower sections of the d.c. link and the operating point of the ASVC. Based upon this derived knowledge, a dynamic SHEM (DSHEM) strategy is proposed where the switching angles are calculated corresponding to the actual operating point of the system. The proposed DSHEM scheme is verified using simulation and experimental 3-level VSI model.

9.2 SWITCHING FUNCTION MODELLING OF VSI BASED ASVC OPERATION

Previous research has shown that a mathematical model of the basic 3-level VSI based ASVC circuit, as shown in Figure 9.1, can be derived through coupling or switching functions [9, 52]. Assuming that the VSI is constructed with ideal switches (no on-state, off-state or switching losses), each phase limb can be represented by a 3-level switch. The principle of the switching function model is that any 'N' level VSI can be modelled from basic voltage waveform outputs. Therefore, any level VSI based ASVC can be represented by switching functions that relate the d.c. quantities to the a.c. quantities. This model technique is highly suitable for investigating the harmonic interaction between the d.c. and a.c. sides of the 3-level inverter.

The 3-position switch within each phase of the VSI, shown in Figure 9.1, allows each phase on the a.c. side to be switched to one of the three terminals on the d.c. side: positive, 'zero' or negative. A 3-angle SHEM switching function for phase R is shown in Figure 9.2. As with the switching state analysis presented in Chapter 4, the switching function is +1 when connected to the positive terminal of the d.c.

link, -1 when connected to the negative terminal and 0 (zero) when connected to the 'zero' or neutral point. As the switching functions are periodic, it's possible to apply Fourier series techniques to split them up into a fundamental and a number of harmonic components. The switching functions for phases Y and B are similar but time-shifted successively by 120° in terms of the fundamental frequency.

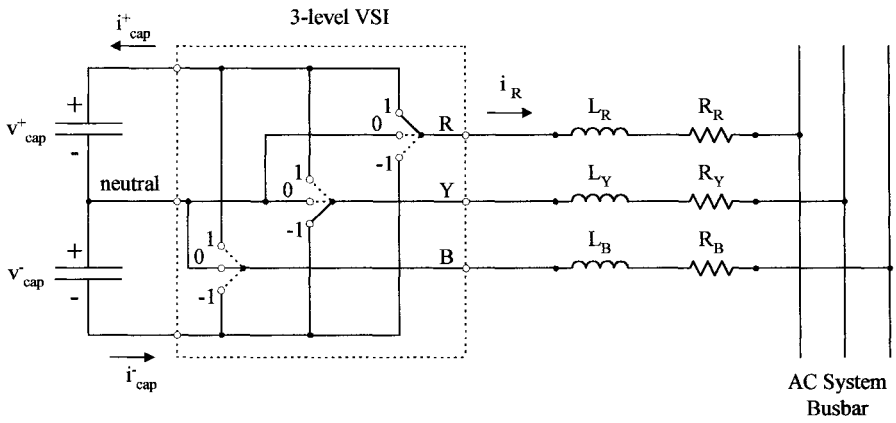


Figure 9.1 – Basic 3-level VSI based ASVC circuit, switch representation.

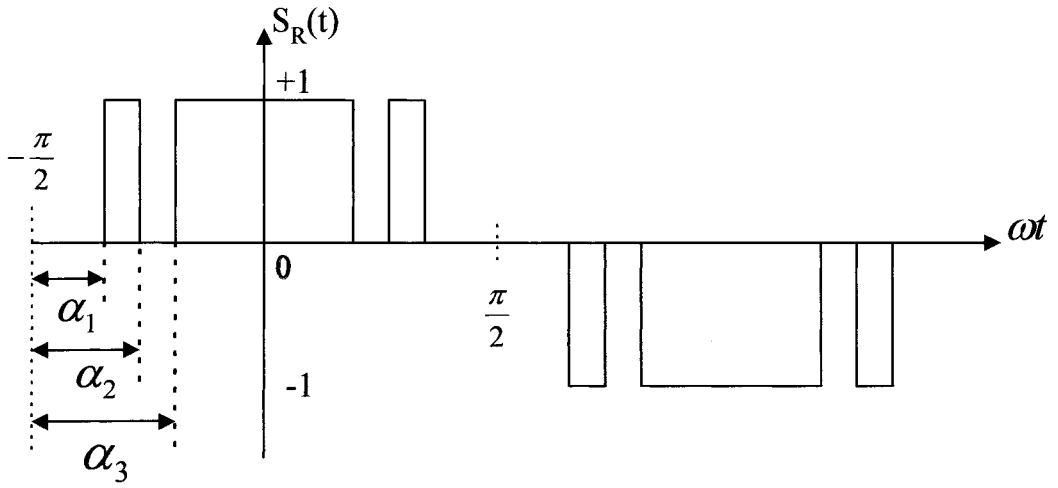
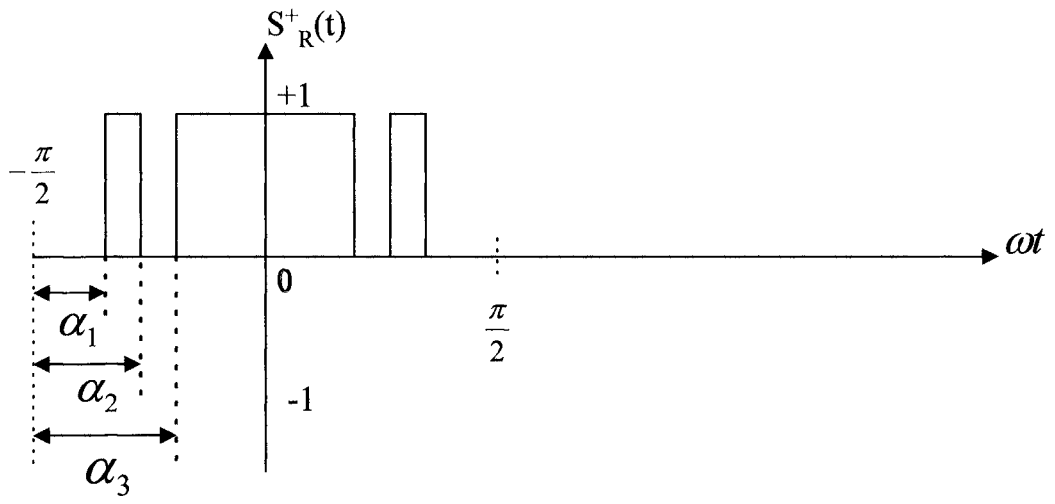
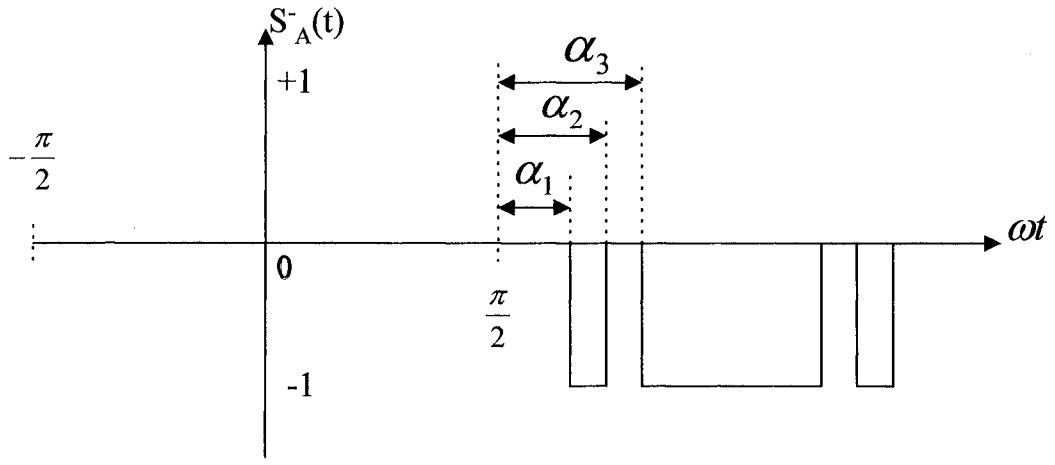


Figure 9.2 – SHEM Switching Function for Phase R

If the switching function is further decomposed into positive and negative halves, as shown in Figure 9.3, analysis can be performed on the effective voltage output associated with each capacitor (upper and lower) of the 3-level d.c. link.



(a) - Upper (positive) half of switching function



(b) – Lower (negative) half of switching function

Figure 9.3 – Decomposition of 3-level SHEM Switching Function

Using the decomposed switching function, the 3-level VSI based ASVC output phase voltages can then be obtained using the switching functions and the upper and lower d.c. side capacitor voltages as follows [9]:

$$\begin{bmatrix} V_R \\ V_Y \\ V_B \end{bmatrix} = \begin{bmatrix} S_R^+ S_R^- \\ S_Y^+ S_y^- \\ S_B^+ S_B^- \end{bmatrix} . \begin{bmatrix} v_{cap}^+ \\ v_{cap}^- \end{bmatrix} \tag{9.1}$$

Hence, phase R output voltage is given as:

$$V_R = S_R^+ . v_{cap}^+ + S_R^- . v_{cap}^- \tag{9.2}$$

Employing the modulation theory analysis presented in [65] the capacitor current for the upper and lower capacitor banks of the d.c. link, as illustrated in Figure 9.1, can then be related to the a.c. side current by:

$$i_{cap}^+ = -i_R(t)S_R^+(t) - i_Y(t)S_Y^+(t) - i_B(t)S_B^+(t) \tag{9.3}$$

$$i_{cap}^- = +i_R(t)S_R^-(t) + i_Y(t)S_Y^-(t) + i_B(t)S_B^-(t) \tag{9.4}$$

The polarities of the a.c. side currents are resultant from the reference direction of the phase current taken out of the inverter. The d.c. side currents can then be related to the capacitor voltages as:

$$i_{cap}^+ = C\frac{dv_{cap}^+}{dt} \tag{9.5}$$

$$i_{cap}^- = C\frac{dv_{cap}^-}{dt} \tag{9.6}$$

Where C is the value of the upper or lower d.c. side capacitance. Rearranging (9.5) and (9.6) in terms of d.c. side capacitor voltage and substitution of equations (9.3) and (9.4) gives:

$$v_{cap}^{+} = \frac{1}{C}\int\left(-i_R(t)S_R^{+}(t) - i_Y(t)S_Y^{+}(t) - i_B(t)S_B^{+}(t)\right)dt \tag{9.7}$$

$$v_{cap}^{-} = \frac{1}{C}\int\left(+i_R(t)S_R^{-}(t) + i_Y(t)S_Y^{-}(t) + i_B(t)S_B^{-}(t)\right)dt \tag{9.8}$$

If the d.c. capacitor voltage is assumed constant then clearly, from equation (9.2), the inverter phase voltage will exhibit the same shape as the switching function. However, the experimental results indicate that under loaded operating conditions the d.c. voltage comprises of a 3rd harmonic component. Therefore, further modulation analysis is required using the halved switching function methodology presented above.

9.3 3-LEVEL MODULATION ANALYSIS AND PROPOSAL OF DSHEM

As with the harmonic analysis of the ideal SHEM voltage waveform presented in Chapter 5, the switching function waveform shown in Figure 9.2 can be decomposed into Fourier series components. The relevant components required to eliminate the low-order harmonic spectra whilst maintaining a suitable fundamental are:

$$S_1 = \frac{4}{\pi}\left(\cos(\alpha_1) - \cos(\alpha_2) + \cos(\alpha_3)\right) \tag{9.9}$$

$$S_5 = \frac{4}{5\pi}\left(\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3)\right) \tag{9.10}$$

$$S_7 = -\frac{4}{7\pi}\left(\cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3)\right) \tag{9.11}$$

$$S_{11} = -\frac{4}{11\pi}\left(\cos(11\alpha_1) - \cos(11\alpha_2) + \cos(11\alpha_3)\right) \tag{9.12}$$

Where S_i represents the algebraic amplitude of the i^{th} harmonic component in the switching function. The negative sign in front of the expression implies that the component is opposite in phase with respect to the fundamental. As described in the harmonic analysis presented in Chapter 5, the SHEM switching angles α_1, α_2 and α_3 are calculated to maximise the fundamental whilst eliminating the 5^{th}, 7^{th} and 11^{th} harmonic components. Throughout this thesis the following angles have been implemented in the 3-level VSI simulation and experimental models:

$$\alpha_1 = 14.016°, \qquad \alpha_2 = 24.504° \quad \text{and} \quad \alpha_3 = 30.288°.$$

The harmonic analysis of ideal voltage waveforms illustrated the suitability of these switching angles, with respect to the elimination of the targeted harmonics. However, the experimental results obtained in this work indicated that the harmonic spectrum is affected by the system loading conditions.

As presented in Chapter 8, when testing the experimental model, it was observed that the harmonic performance deteriorates with increasing reactive load requirements. The experimental results illustrate that the output phase voltage is distorted due to a 3^{rd} harmonic ripple component on the d.c. link upper and lower capacitor voltages. Equation (9.2) shows that if the d.c. link capacitor voltage is not constant the resultant phase voltage will differ from the ideal switching function waveform from which the SHEM angles had been calculated. Equations (9.7) and (9.8) show that the d.c link capacitor voltage ripple is dependent upon the value of the capacitance and the switching function multiplied by the a.c. side current. A large value capacitor would therefore minimise any ripple component at specified harmonic frequencies. However, this would also restrict the dynamic performance of the ASVC.

Due to the coupling inductance between the ASVC and the a.c. system, resulting in the current waveform being much smoother than the inverter a.c. side voltage, the harmonics contained in the a.c. line current are ignored for this analysis. The case of the ASVC absorbing lagging reactive power, where the phase current lags

the phase voltage by 90° is initially considered. Assuming ideal phase balanced operation, the three-phase output currents can be denoted as follows:

$$i_R(t) = I_1 \cos\left(\omega t - \frac{\pi}{2}\right) \tag{9.13}$$

$$i_Y(t) = I_1 \cos\left(\omega t - \frac{\pi}{2} - \frac{2\pi}{3}\right) \tag{9.14}$$

$$i_B(t) = I_1 \cos\left(\omega t - \frac{\pi}{2} - \frac{4\pi}{3}\right) \tag{9.15}$$

Where I_1 is the peak value of the inverter output current.

Therefore assuming sinusoidal a.c. side currents, the SHEM switching function is analysed to investigate the mechanism effecting the harmonic elimination of the 3-level output voltage.

For the purpose of modulation analysis the Fourier coefficients of the switching function are maintained separate for positive and negative halves of the switching function, as shown in Figure 9.3. Using the decomposed SHEM switching functions, from Fourier analysis it can be shown that the respective Fourier coefficients for the positive half switching function (S^+_R) and the negative half switching function (S^-_R) contain both odd and even order harmonic components. Using the switching angles α_1, α_2 and α_3, the 2nd and 4th harmonics in the positive half of the switching function can be derived (Appendix F) as:

$$S_2^+ = \frac{2}{2\pi}\left[\sin(2\alpha_1) - \sin(2\alpha_2) + \sin(2\alpha_3)\right] \tag{9.16}$$

$$S_4^+ = \frac{2}{4\pi}\left[\sin(4\alpha_1) - \sin(4\alpha_2) + \sin(4\alpha_3)\right] \tag{9.17}$$

With respect to the time reference shown in Figure 9.3 the even harmonics are again cosine terms in the Fourier series. Note that, in the combined switching function output of the 3-level voltage waveform shown in Figure 9.2, the even order harmonics cancel.

Considering equation (9.3) for the upper capacitor current (i^{+}_{cap}), if the switching functions are replaced with the corresponding phase Fourier series and the respective trigonometric identity is applied to convert product into summation, it can be shown that some terms due to odd harmonics in the half switching functions will cancel between phases. However, others corresponding to current through the full d.c. link will cause voltage ripple at 12^{th} etc. harmonic frequencies. The amplitude will be relatively small as will be discussed later. Therefore, i^{+}_{cap} will be dominated with the contributions from the 2^{nd} and 4^{th} harmonic terms associated with the positive half of the switching function.

Using equation (9.3), the resultant harmonic current in the capacitor corresponding to the 2^{nd} order harmonic in the positive half of the switching function can be represented as:

$$i^{+2}_{cap3}(t) = -i_R(t)S_2^{+}\cos(2\omega t) - i_Y(t)S_2^{+}\cos\left(2\omega t - \frac{4\pi}{3}\right) - i_B(t)S_2^{+}\cos\left(2\omega t - \frac{8\pi}{3}\right) \tag{9.18}$$

Substituting for $i_R(t)$, $i_Y(t)$ and $i_B(t)$ from equations (9.13), (9.14) and (9.15) and simplifying yields:

$$i^{+2}_{cap3}(t) = -\frac{3}{2} I_1 S_2^{+} \sin(3\omega t) \tag{9.19}$$

This illustrates that the capacitor current mainly contains the 3^{rd} harmonic, which is dependant upon I_1, i.e. the load level of the ASVC. Using the above procedure to find the resultant 3^{rd} harmonic capacitor current due to both the 2^{nd} and the 4^{th} harmonic components associated with the positive half switching function, the

total 3rd harmonic current flowing into the upper d.c. capacitor can be shown (Appendix F) to be:

$$i_{cap3}^{+2,4}(t) = -\frac{3}{2} I_1 \left(S_2^+ - S_4^+ \right) \sin(3\omega t) \tag{9.20}$$

This capacitor current can be used to derive the 3rd harmonic voltage across the capacitor, as:

$$v_{cap3}^{+2,4}(t) = \frac{1}{C} \int i_{cap3}^{+2,4}(t) dt = \frac{1}{2\omega C} I_1 \left(S_2^+ - S_4^+ \right) \cos(3\omega t) \tag{9.21}$$

where C is the upper or lower capacitance.

A similar analysis can be applied to the lower d.c. side capacitor as the 2nd and 4th harmonics in the negative switching function half can be shown as:

$$S_2^- = -\frac{2}{2\pi} \left[\sin(2\alpha_1) - \sin(2\alpha_2) + \sin(2\alpha_3) \right] \tag{9.22}$$

$$S_4^- = -\frac{2}{4\pi} \left[\sin(4\alpha_1) - \sin(4\alpha_2) + \sin(4\alpha_3) \right] \tag{9.23}$$

Therefore, with the reference direction shown in Figure 9.1, the 3rd harmonic current and voltage for the lower d.c. side capacitor are opposite to those for the upper one. That is:

$$i_{cap3}^-(t) = -i_{cap3}^+(t) \qquad \text{and} \qquad v_{cap3}^-(t) = -v_{cap3}^+(t) .$$

This explains why the 3rd harmonic voltage is normally invisible across the full d.c. link. However, the 3rd harmonic in each capacitor voltage can be modulated back to the a.c. side by the 2nd and 4th harmonics in the positive and negative halves of the switching function. This will add to the 5th and 7th harmonic voltage

on the a.c. side. Taking into account the polarities of the capacitor voltage and switching function, the additional 5th harmonic in the a.c. side voltage (phase R) resulting from both the positive and negative halves of the d.c. link is calculated using equation (9.2) as:

$$\Delta v_{5th}^{\pm 2}(t) = v_{cap3}^{+}(t) S_2^{+} \cos(2\omega t) + v_{cap3}^{-}(t)\left[-S_2^{+} \cos(2\omega t)\right]$$

$$= 2\frac{1}{2\omega C} I_1 \left(S_2^{+} - S_4^{+}\right) \cos(3\omega t) S_2^{+} \cos(2\omega t)$$

$$= \frac{I_1}{2\omega C}\left(S_2^{+} - S_4^{+}\right) S_2^{+} \cos(5\omega t) + \frac{I_1}{2\omega C}\left(S_2^{+} - S_4^{+}\right) S_2^{+} \cos(\omega t) \qquad (9.24)$$

It is clear from this equation that additional fundamental and 5th harmonic components are generated. The total 5th harmonic component in the a.c. side phase voltage can now be found from equations (9.10) and (9.24) and may be expressed as below including both the constant component of the capacitor voltage and the 3rd harmonic ripple.

$$\frac{V_5}{V_{cap0}} = \frac{4}{5\pi}\left[\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3)\right] + \frac{I_1}{2\omega C V_{cap0}}\left(S_2^{+} - S_4^{+}\right) S_2^{+} \qquad (9.25)$$

The 5th harmonic voltage in the above equation is scaled according to the average d.c. capacitor voltage, V_{cap0}. The 3rd harmonic voltage of the capacitor will also be modulated by the 4th harmonic in the positive and negative halves of the switching function to give additional 7th harmonic on the a.c. side of the inverter. The 7th harmonic voltage can be similarly derived as:

$$\frac{V_7}{V_{cap0}} = \frac{4}{7\pi}\left[\cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3)\right] + \frac{I_1}{2\omega C V_{cap0}}\left(S_2^{+} - S_4^{+}\right) S_4^{+} \qquad (9.26)$$

Higher order harmonics in the a.c. side voltage such as the 11th will not be affected as much. However, the experimental results presented in Chapter 8

illustrate that there is some small error in the elimination of the 11^{th} harmonic component. The above analysis shows that a dynamic SHEM scheme is required in which the switching angles α_1, α_2 and α_3 are determined using equations (9.25), (9.26) and (9.9). As the 3^{rd} harmonic ripple of the capacitor voltage depends on the load level of the ASVC, the switching angles have to be adjusted to track the operating point. A flow chart describing the function of the controller is shown in Figure 9.4.

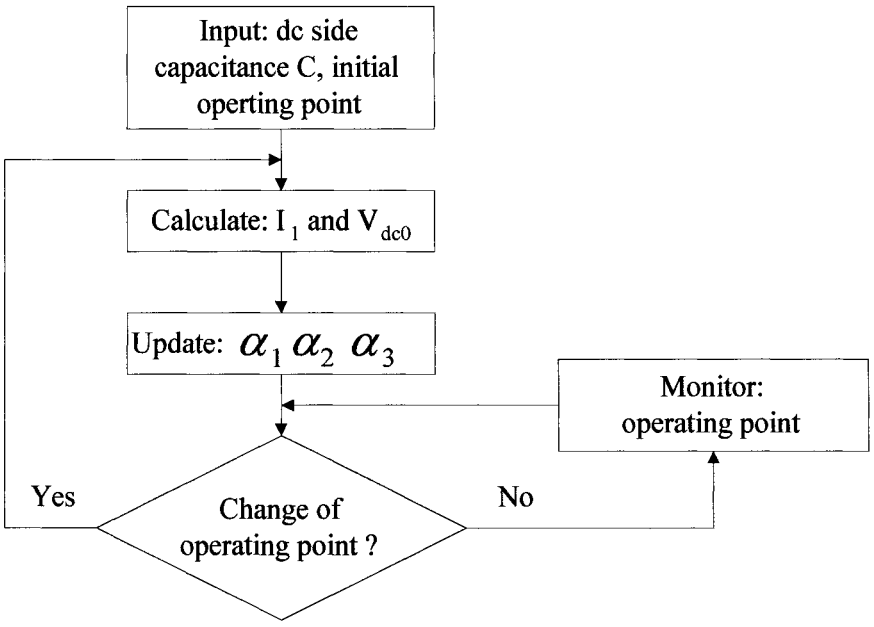


Figure 9.4 – Flow Chart illustrating Dynamic SHEM calculations

If I_1 and V_{dc0} are not directly measured, monitoring of the operating point can be achieved from the system bus voltage and the reactive power demand. Practically, the switching angles can be calculated off-line for different operating conditions and accuracy obtained through interpolation from a look-up table.

As the d.c. side ripple affects the fundamental of the output voltage the off-line calculation also need to be iterative to maintain the value of the fundamental

voltage constant. This may sometimes be more easily achieved with a new value of the average capacitor voltage.

When the ASVC generates leading reactive power, as illustrated in the experimental test 1 of Chapter 8, the interactions between the a.c. and d.c. sides of the 3-level inverter will also affect the harmonic characteristic on the a.c. side. Switching angles to remove the 5^{th}, 7^{th} and 11^{th} harmonics can be similarly determined using the dynamic SHEM approach. However, in this case, the phase relationship between the a.c. side voltage and the current is reversed; i.e. the current supplied by the inverter now leads the voltage by 90. As a results, I_1 should be changed to $-I_1$ in equations (9.25) and (9.26). The analysis of the dynamic SHEM can be extended to an inverter with higher number of levels provided that it operates in balanced conditions.

9.4 ASVC SIMULATION WITH CONVENTIONAL SHEM & DYNAMIC SHEM

Using the basic circuit shown in Figure 9.1, operation of the 3-level VSI based ASVC was simulated in the time domain using the SABER package. This package has excellent Fourier analysis tools, which were used to determine the harmonic spectrum of the output waveforms. Also, the simulation package allows switching instants, as specified from the SHEM switching functions, to be programmed into the control template, as they would be in a practical implementation of a switching controller.

Using switching angles computed from standard SHEM and dynamic SHEM schemes, an ASVC was simulated with the following parameters: Vs = 11 kV at 50 Hz, C = 40 μF/side, L = 60 mH/phase.

Using the angles (α_1 = 14.016°, α_2 = 24.504° and α_3 = 30.288°) as calculated for the conventional SHEM scheme the output voltage and current of the ASVC together with the spectrum of the line-line voltage obtained are shown in Figure 9.5. For the direction of current specified in Figure 9.1, the ASVC provides

3.166MVAr leading reactive power to the system. The simulation results correspond with the reactive load experimental results indicating that considerable 5^{th} and 7^{th} harmonics are present in the spectrum. Characteristically the coupling inductance between the ASVC and the a.c. system exhibits low impedance at relatively low harmonic orders. Therefore the 5^{th} and 7^{th} harmonics in the output voltage will cause large harmonic current to be injected into the system.

Using the same simulation parameters and hence, operating point, new switching angles using the DSHEM scheme are computed which reflect the 3^{rd} harmonic ripple in the capacitor voltage. The DSHEM switching angles for this leading mode ASVC operating point are:

$$\alpha_1 = 16.066°, \qquad \alpha_2 = 24.345° \quad \text{and} \quad \alpha_3 = 31.318°.$$

As illustrated in the results shown in Figure 9.6, the ASVC provides the same reactive power, whilst maintaining an improved harmonic performance. The 5^{th} and 7^{th} harmonics on the inverter a.c. side voltage are now reduced by 76% and 85%, respectively. This improvement is also reflected in the current waveshape.

To illustrate the overall performance improvements possible with the DSHEM angles implemented for the ASVC, the lagging mode of operation was also simulated. As the operating point has now changed, and the angles are dependent upon the operating point, new switching angles using the DSHEM scheme are derived as:

$$\alpha_1 = 11.431°, \qquad \alpha_2 = 25.921° \quad \text{and} \quad \alpha_3 = 29.834°.$$

The simulation results shown in Figure 9.7 illustrate how the 5^{th}, 7^{th} and 11^{th} harmonics are dynamically eliminated in the inverter a.c. side voltage.

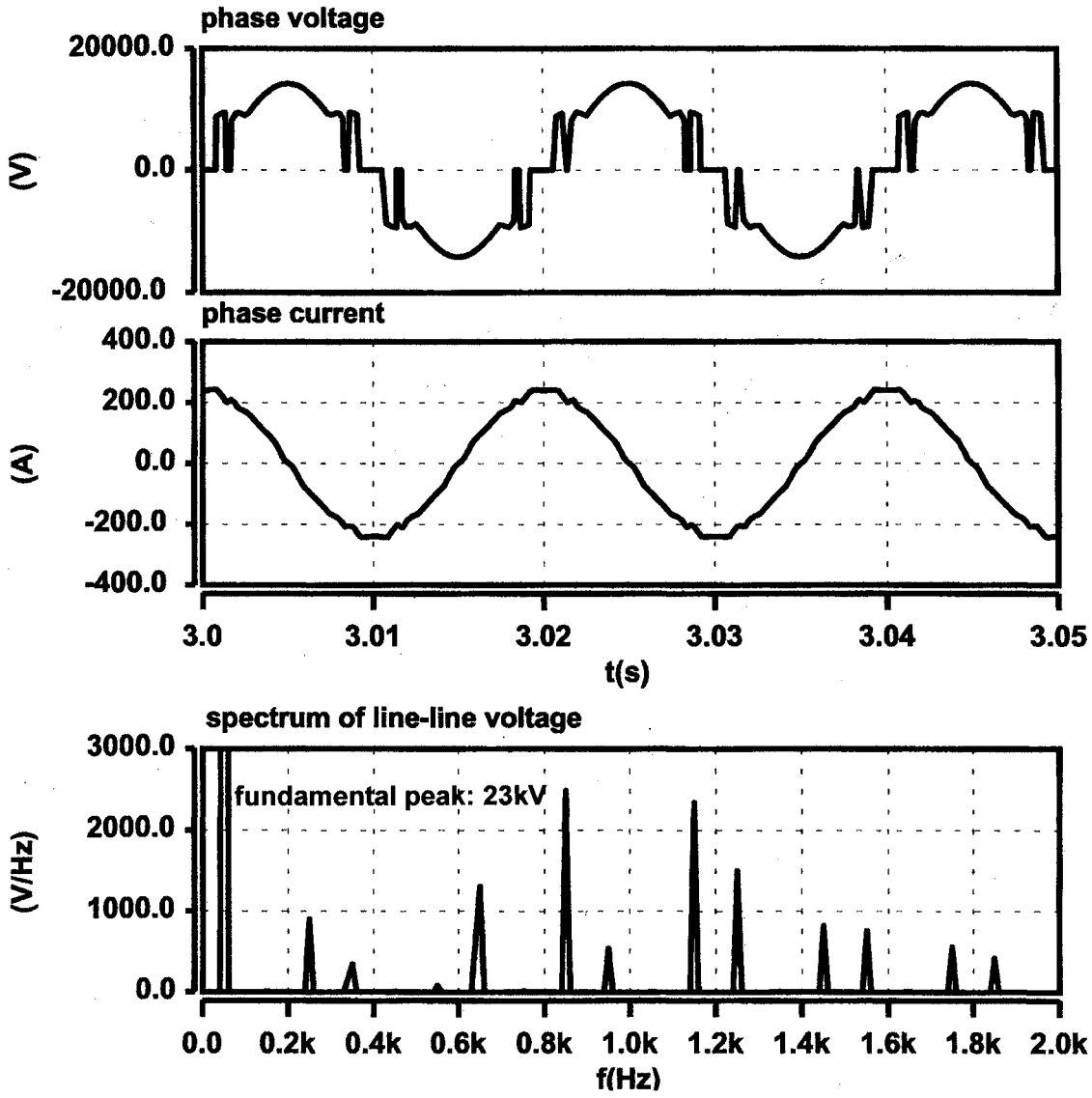


Figure 9.5 – Simulation Results with Conventional SHEM – leading mode

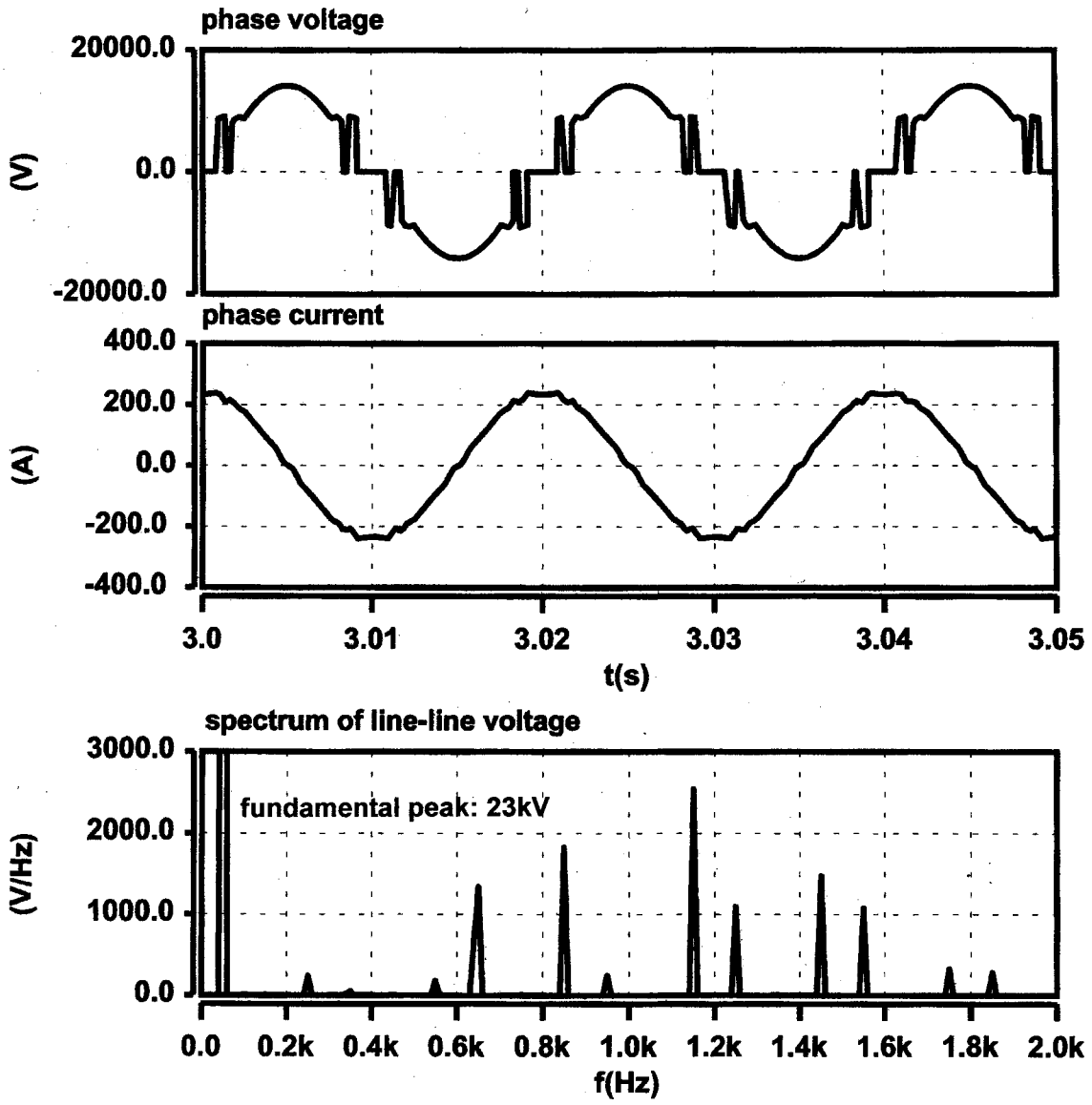


Figure 9.6 – Simulation Results with Dynamic SHEM – leading mode

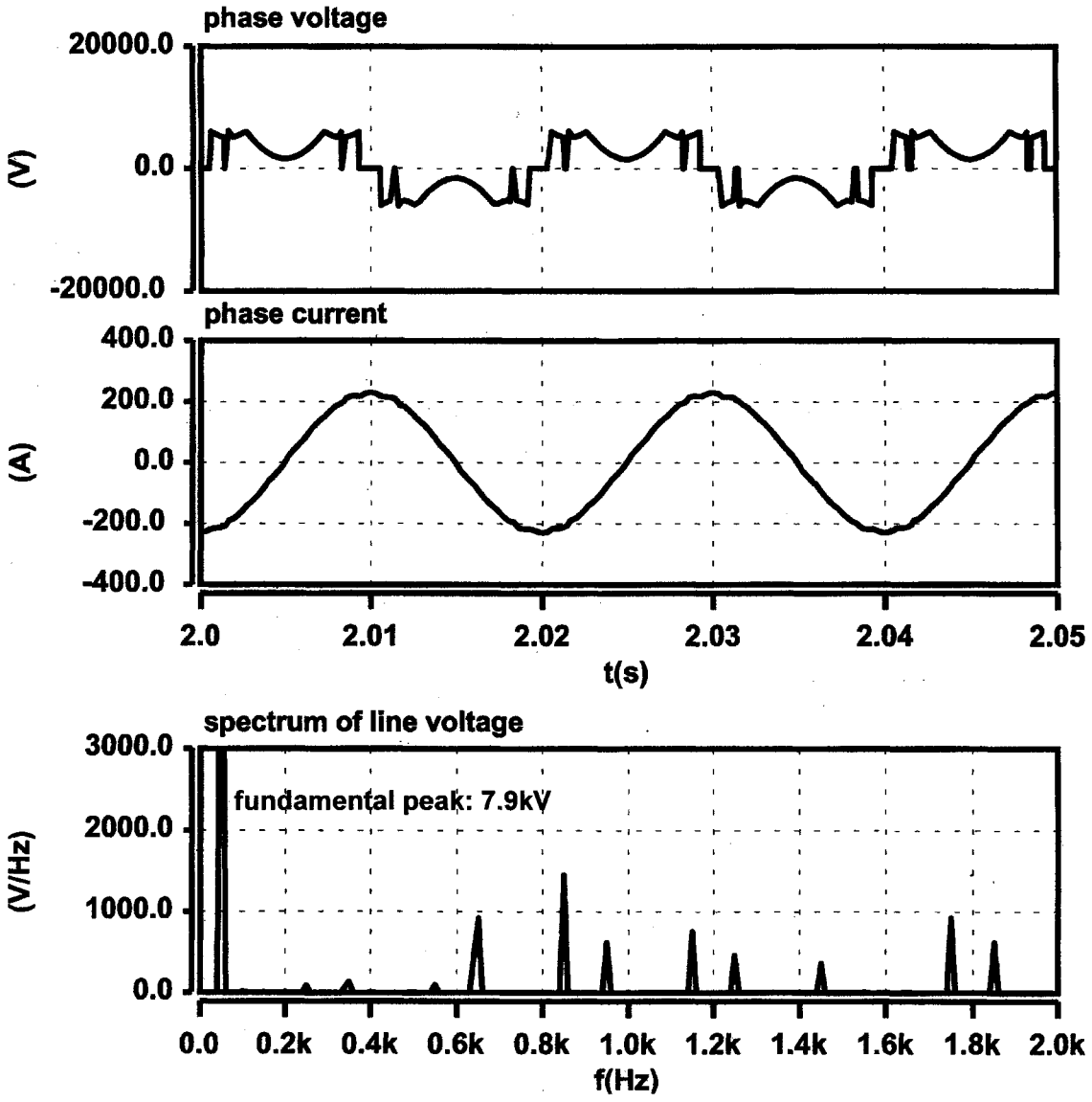


Figure 9.7 – Simulation Results with Dynamic SHEM – lagging mode

9.5 EXPERIMENTAL VERIFICATION OF 3-LEVEL DSHEM

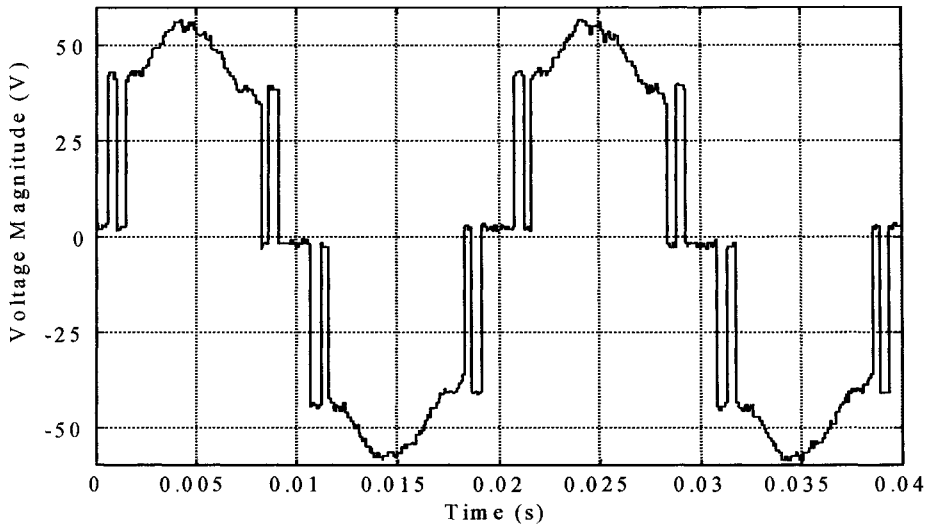
The proposed dynamic SHEM scheme was further verified using the laboratory model of the 3-level VSI. The inductive load experimental test presented in Chapter 8 was used for investigating the system harmonic performance. As the DSHEM switching angles are calculated dependant upon operating point of the system, precise laboratory model parameters were measured. The d.c. capacitance at each level is 333 μF. The full d.c. link voltage is precharged to 96.7 V and the system side voltage was adjusted such that the ASVC provides a 4.078 A (rms) leading reactive current. The large inductive load bank maintained the assumption that the a.c. side current was sinusoidal.

The new DSHEM switching angles corresponding to the 3-level VSI based ASVC experimental model parameters as:

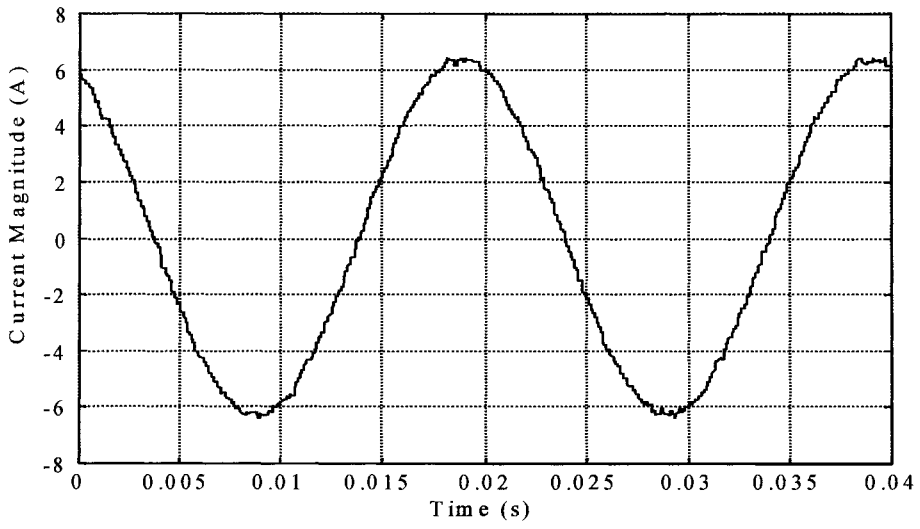
$$\alpha_1 = 14.491°, \qquad \alpha_2 = 24.21° \quad \text{and} \quad \alpha_3 = 30.42°.$$

Using the procedure presented in Chapter 7, the new switching angles were implemented into the TMS320F240 DSP digital controller. The output phase voltage and current results obtained from the experimental tests implementing the DSHEM angles are shown in Figure 9.8. The output line voltage and corresponding harmonic spectrum produced with the DSHEM scheme are given in Figure 9.9.

Observation of the capacitor voltage ripple for the upper and lower capacitors, given in Figure 9.10, re-confirms that the ripple is dominated by the 3rd harmonic component. The 3rd harmonic ripple on the d.c. side is still reflected in the phase and line output voltages. However since the new switching angles are determined including the modulating interaction, the 5th and 7th are now absent from the line voltage spectrum (see Figures 9.9b and 8.12b). Table 9.1 compares the low-order spectra for the conventional and dynamic SHEM scheme with the same operating point.

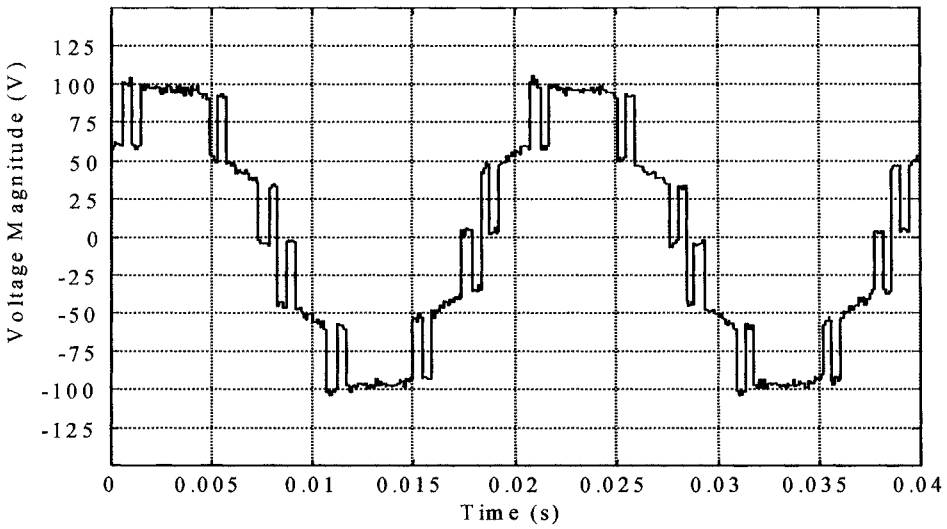


(a) – 3-level DSHEM output phase voltage

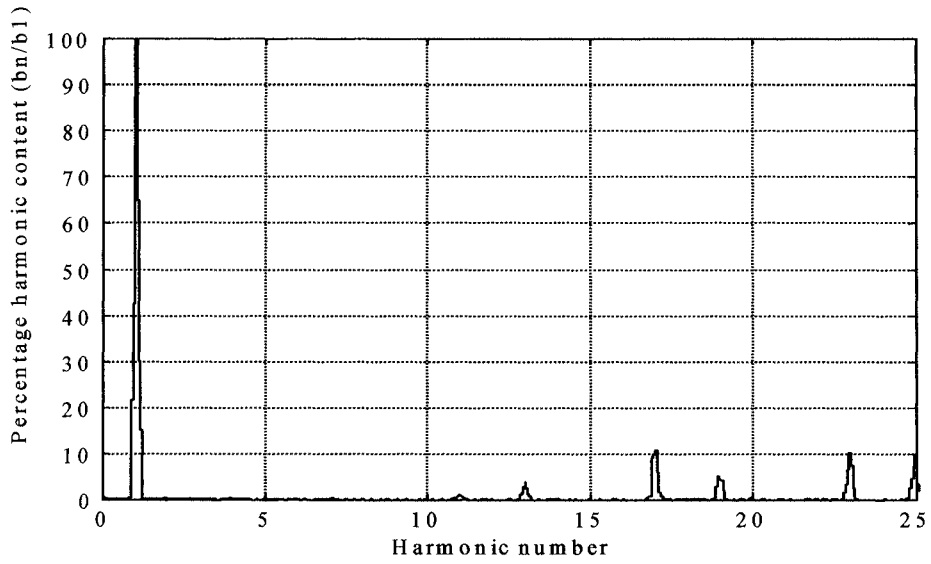


(b) – 3-level DSHEM output current

Figure 9.8 – Waveforms for 3-level DSHEM VSI with an inductive load

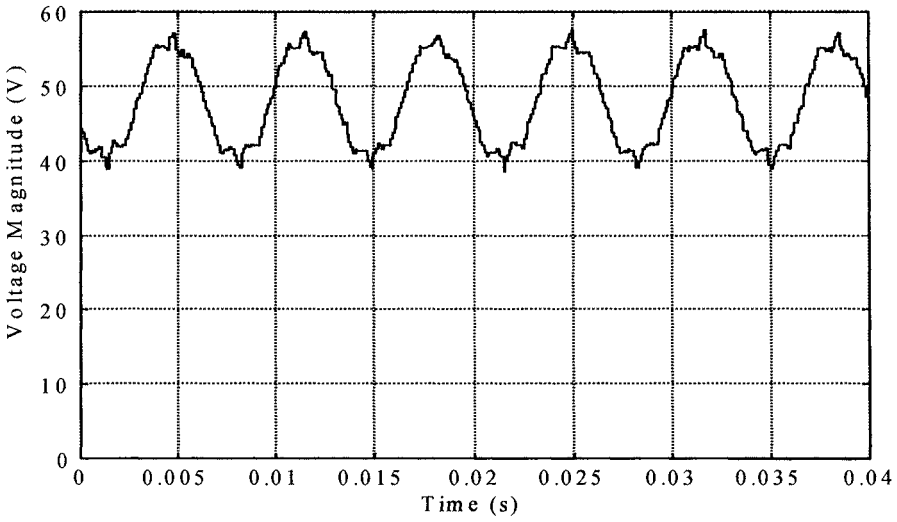


(a) – 3-level DSHEM output line voltage

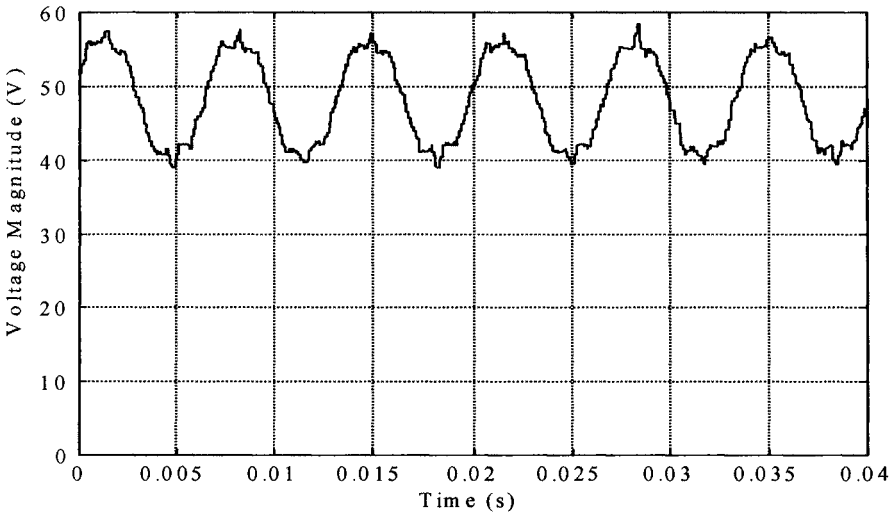


(b) – 3-level DSHEM output line voltage Harmonic Spectra

Figure 9.9 – Waveforms for 3-level DSHEM VSI with inductive load



(a) – DC voltage on upper capacitor



(b) – DC voltage on lower capacitor

Figure 9.10 – Waveforms for 3-level DSHEM VSI with inductive load

Harmonic Number	3-level SHEM (Lab model)	3-level DSHEM (Lab model)	3-level SHEM (Theoretical)
1	100	100	100
5	2.22	0	0
7	1.38	0	0
11	0.9	1.1	0
13	6.319	4.2	7.64

Table 9.1 – Line Voltage Harmonic Component % Values – Inductive Load

9.6 DISCUSSIONS OF DSHEM PERFORMANCE

The experimental results, presented in Chapter 8, indicated that when the 3-level VSI was loaded, the target low-order harmonics were not completely eliminated by the conventional SHEM scheme. Observation of the 3rd harmonic ripple in the upper and lower capacitor voltages indicated that the 5th and 7th harmonics were being modulated back to the a.c. side of the inverter.

The harmonic interaction between the a.c. and d.c. side currents and voltages has been investigated. Using equation sets dependant upon the system operating point for the switching angles, a Dynamic Selective Harmonic Elimination Modulation (DSHEM) scheme is proposed. The improved performance of the 3-level DSHEM VSI based ASVC has been verified using simulation and an experimental results. Table 9.1 illustrates the improved elimination of the targeted 5th and 7th harmonics in the 3-level output line voltage. There is still some errors in the 11th harmonic as the DSHEM switching angles computed for this analysis were optimised on the 5th and 7th harmonic components of the output voltage spectrum.

10 CONCLUSIONS

This thesis reports the project investigations into the inherent robustness and harmonic performance of a high power multi-level voltage source inverter (VSI) based Advanced Static VAr Compensator (ASVC). A new adaptive 3-level inverter topology and switching control scheme for the ASVC application have been proposed. A computer model and a laboratory model of the proposed system have been designed, constructed and tested. The results obtained have illustrated the improved operational robustness of the adaptive VSI, whilst maintaining suitable operating characteristics to provide the required reactive power (VAr) compensation. Although the experimental study focussed on a 3-level system, it was illustrated that the proposed adaptive topology and switching control can be applied to higher-level systems where more benefit can be achieved. The harmonic interaction between the a.c. and d.c. sides of the 3-level VSI based ASVC has been analysed and a dynamic modulation scheme has been proposed to reduce this interaction. As detailed discussions have been provided at the end of each Chapter throughout the thesis, a summary of the knowledge amassed during this research is given in this Chapter. Suggestions for further research are also given.

The preliminary Chapters of this thesis presented the necessity for reliable Flexible AC Transmission System (FACTS) controllers with particular focus upon shunt connected reactive power (VAr) compensators. Conventional and modern shunt compensation topologies have been compared to illustrate the progressive developments and increasing performance requirements necessary for today's complex transmission systems. Identifying the voltage source inverter (VSI) based Advanced Static VAr Compensator as the system to be further investigated, basic operating principles of the ASVC have been presented to specify the requirements of a suitable topology.

The VSI topologies proposed in the literature as suitable for the ASVC application include the six-pulse bridge, implemented in multi-phase arrangements, and a number of various multi-level configurations. A comparison of suitable VSI

topologies discussing relative advantages with respect to the harmonic performance and complexities of control and configuration has been presented.

10.1 Robustness and Inherent Redundancy Investigations for the Diode-Clamped Multi-level VSI

A study into the VSI topology robustness and inherent redundancy in the event of a device fault has been conducted, with particular emphasis on the diode-clamped multi-level inverter (DCMLI). Using a space vector nodal representation, the inverter topology structure was analysed to observe the possibility of continual system performance under abnormal conditions. The investigations conducted illustrated that the conventional DCMLI topology offers a very limited inherent redundancy to maintain continual operation. Therefore, designers tend to provide generous series back-up devices.

The redundancy analysis illustrated that in the event of certain device failures the system could revert to a 2-level (bi-polar) strategy. The possibility of recovering the normal (3-level) harmonic performance during abnormal (2-level) operation has been investigated. The results of this investigation illustrates that the ASVC performance can be maintained if an adaptive bi-polar Selective Harmonic Elimination Modulation (SHEM) scheme is applied. However, the robustness of the 3-level topology is still very limited. Investigations of higher-level topologies showed similar inherent redundancy limitations to device failures.

10.2 The Adaptive DPPSC-MLI Topology

Based on the results of the redundancy and harmonic analysis of the DCMLI topology, a new adaptive discharge path protection switch clamped multi-level inverter (DPPSC-MLI) topology has been proposed. A new adaptive 3-level DPPS control scheme that maintains uninterrupted operation during device failure has been designed and implemented. The proposed scheme maintains 3-level SHEM harmonic performance or reverts to a 2-level SHEM scheme, dependant upon the positioning of the device failure within the phase-limb. Therefore,

maintaining acceptable continual performance throughout normal and abnormal operating conditions.

The structural properties of the proposed adaptive multi-level topology and the effect of the adaptive switching controller upon the overall switching frequency have been investigated. Initially considering the structural properties, the analysis illustrates that, in the event of a device failure, the magnitude of the increased voltage stress across the healthy devices reduces as the topology level increases. The effect of the adaptive DPPS controller upon switching frequency is presented by considering the 3-level to 2-level adaptive SHEM strategy. The analysis illustrates that the harmonic spectrum of the system can be recovered under abnormal operating conditions with an acceptable increase in switching frequency.

The suitability of the adaptive 3-level DPPSC-MLI topology for the ASVC application is verified using a computer model in the Matlab/Simulink environment. Faults are simulated to specific devices to observe the improved robustness and harmonic performance of the proposed VSI system.

10.3 Development of ASVC Laboratory Model

To verify the theoretical and simulation results, an experimental laboratory model of the adaptive 3-level VSI has been designed, built and tested. The power circuit was designed such that the conventional DCMLI and proposed DPPSC-MLI topologies could be investigated. The experimental control scheme was developed using a TMS320F240 DSP to provide a real time digital controller. Throughout the work various low frequency modulation schemes were implemented and tested on the laboratory model. The adaptive switching controller for the 3-level to 2-level SHEM schemes has been implemented in this work.

As the accuracy of setting the SHEM switching angles is essential, an angular reference sinewave was digitally generated on the DSP using interpolation routines off a look-up table. The accuracy obtained from the 'F240 DSP for the SHEM angles appeared almost ideal when the produced harmonic spectrum was

compared to the theoretical harmonic analysis. Slight errors were introduced due to performance tolerances of the IGBT drivers used between inverter phase-limbs. A serial communication link was developed between the digital controller and a Pentium PC such that a user terminal was available for real time interaction to the hardware model. As an open-loop controller was implemented, another phase-shifted reference sinewave was also generated from interpolation of a look-up table. The resultant system reference frequency was controlled to an accuracy of ±0.2 Hz, which was considered suitable for the experimental study.

10.4 Performance Analysis of the Proposed System

The real-time performance of the proposed system has been tested by using two experimental procedures. Operation of the adaptive 3-level VSI topology for the ASVC application was realized by using a synchronous machine. The reactive power flow in both leading and lagging modes of operation was demonstrated. The performance of the proposed topology under normal operating conditions was demonstrated to be identical to the conventional 3-level DCMLI structure.

To investigate the improved robustness of the proposed adaptive topology and control scheme, an inductive load test procedure was used. Experimental results for both no-load and loaded operating conditions illustrated the continual performance of the 3-level VSI during abnormal operating conditions. For no-load conditions, the harmonic spectrum obtained for the output line voltage under abnormal operating conditions was maintained similar to that for normal conditions. The 5^{th}, 7^{th} and 11^{th} harmonic components, targeted by the modulation controller, were eliminated using 3-level SHEM and 2-level SHEM for normal and abnormal operating conditions, respectively.

To observe the improved robustness of the proposed adaptive 3-level VSI topology, short-circuit device faults to devices S_{R1} and S_{R2} were analysed. Under inductive load conditions, the system was observed to revert to a 2-level VSI topology and adapt a bi-polar SHEM switching strategy in the event of S_{R1}. In the case of S_{R2} failing short-circuit, the system maintained uninterrupted continual 3-level SHEM operation utilising the sequential DPPS control scheme.

10.5 THE DYNAMIC SHEM SCHEME

From previous research studies it was predicted that under loaded conditions the ASVC harmonic performance would differ from the ideal theoretical line voltage spectrum. The output voltage spectrum obtained from the experimental ASVC shows that the targeted 5^{th}, 7^{th} and 11^{th} harmonics are not eliminated by the SHEM scheme under loaded conditions. Harmonic analysis conducted in this work showed that with conventional SHEM schemes, the 5^{th} and 7^{th} harmonics are modulated back to the a.c. side of the inverter. This is due to the 3^{rd} harmonic ripple in the d.c. capacitor voltage.

The harmonic performance of the 3-level VSI based ASVC resulting from system operating point is analysed and a dynamic Selective Harmonic Elimination Modulation (DSHEM) scheme is proposed. The proposed DSHEM was verified using the 3-level laboratory model where the switching angles were determined based on the operating point of the ASVC. The results obtained illustrate an improvement in the harmonic performance over the conventional SHEM scheme.

10.6 SUGGESTIONS FOR FURTHER RESEARCH

The research work described in this thesis has developed an adaptive topology and controller suitable for the ASVC application. Within the limited time available for the research, a basic 3-level VSI hardware model has been constructed to demonstrate the proposed techniques. To investigate the full potential of the adaptive schemes and dynamic modulation techniques further work is required. The following sections identify possible further research that may be conducted:

1. The laboratory model demonstrated the adaptive DPPS topology and control scheme for a 3-level VSI. Preliminary work carried out showed the suitability of the DPPS scheme for higher-level inverters. For example, the harmonic performance of the 5-level FFM topology can be recovered through adaptive 3-level SHEM schemes. Implementations of higher-level VSI configurations need to be further investigated. Also to investigate the possibility of designing a criterion to predict lost switching states resulting

from a device failure and a technique to automatically detect device failure to instigate the adaptive topology/control.

2. The results obtained from this work illustrate that under abnormal operating conditions, maintaining continual operation results in increased voltage stresses on the remaining 'healthy' devices in the same phase limb. This need further investigation with particular focus upon operating procedures, with respect to the device ratings, and the resultant stresses if the adaptive scheme is applied to higher-level VSI topologies.

3. As the thesis focussed upon high power applications, low-frequency modulation schemes were investigated. The possibility of implementing self-tuning space vector modulation (SVM) schemes, for low to medium power drive applications, to recover the harmonic performance with on-line measurement techniques needs investigation.

4. The results of the proposed performance recovery scheme illustrate increased magnitudes of high frequency harmonic components. Further work may be carried out to develop suitable filter arrangements (passive or active) for the adaptive modulation schemes.

5. An open-loop control scheme was implemented throughout this thesis. This needs developing into a complete closed-loop controller such that the VSI based ASVC hardware model can be further investigated for dynamic performance and improved robustness throughout varying system operating conditions.

6. The DSHEM scheme proposed to improve the ASVC harmonic performance at different operating points needs further development to investigate the possible accuracy of the modulation scheme over continually changing operating conditions.

7. Observations of the 3^{rd} harmonic ripple on the upper and lower capacitor voltages and the modulation analysis presented in Chapter 9 illustrate that modulation schemes to remove the 2^{nd} and 4^{th} harmonics from the halved switching functions need further investigation to minimise the ripple.

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APPENDIX A

POWER FLOWS AND REACTIVE POWER COMPENSATION

It is fundamentally known that the power flow in a transmission line depends upon three main parameters: the line impedance, the voltages at the two line ends and the phase angle between the two line end voltages. By modification of these parameters the power transmission capability of the lines can be increased and brought closer to its thermal limit. FACTS devices can be utilised to control any one, or more, of these parameters. The amplitude of the voltage at a selected terminal of the transmission line can be controlled by the application of static VAr compensators. The power flow through a transmission line and the use of shunt compensators to provide reactive power compensation is described in this Appendix.

A.1 POWER FLOW THROUGH A TRANSMISSION LINE

It is usual practise in power systems to represent part of a transmission network by its Thevenin equivalent circuit. The Thevenin circuit comprises a voltage source (sending-end voltage of the line) and a series impedance (impedance of the line R+jX), with the transmission line capacitance ignored, as illustrated in Figure A.1.

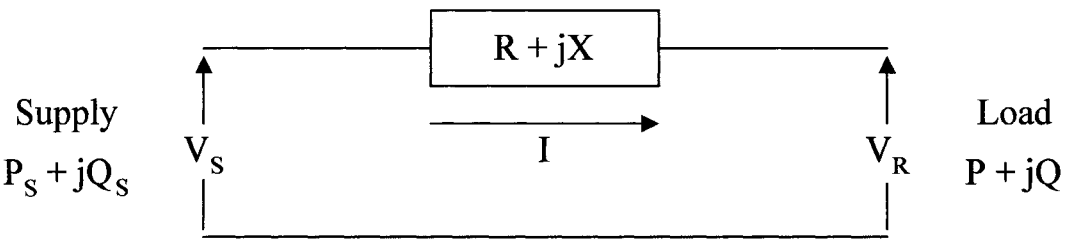


Figure A.1

If it is assumed that the receiving-end voltage $\overline{V}_R$ is the reference phasor, i.e. $\overline{V}_R = V_R \angle 0°$, the line current is given as:

$$I = \frac{V_s \angle \delta - V_R \angle 0}{Z \angle \psi} = \frac{V_S \angle (\delta - \psi) - V_R \angle (-\psi)}{Z} \tag{A.1}$$

Where $\psi = \tan^{-1}\left(\frac{X}{R}\right)$ is the line impedance angle.

Converting into Cartesian form the line current can be shown as:

$$I = \frac{V_S \cos(\delta - \psi) - V_R \cos\psi}{Z} + j\frac{V_S \sin(\delta - \psi) + V_R \sin\psi}{Z} \tag{A.2}$$

The apparent power at the receiving-end may be found as:

$$S = P + jQ = V_R I^* \tag{A.3}$$

$$S = V_R\left[\frac{V_S \cos(\delta - \psi) - V_R \cos\psi}{Z} - j\frac{V_S \sin(\delta - \psi) + V_R \sin\psi}{Z}\right] \tag{A.4}$$

The active power flow of the network can then be obtained by observing the real part of equation (A.4) as:

$$P = \frac{V_S V_R}{Z}\cos(\delta - \psi) - \frac{V_R^2}{Z}\cos\psi \tag{A.5}$$

For a particular line, ψ is constant, and hence P_{max} occurs when $\delta = \psi$.

$$P_{\max} = \frac{V_S V_R}{Z} - \frac{V_R^2}{Z}\cos\psi \tag{A.6}$$

Also, in transmission systems, the X/R ratio is normally high, hence the effect of the line resistance is small and may be neglected. Therefore $\psi = 90°$ and equation (A.5) gives:

$$P = \frac{V_S V_R}{X} \sin\delta \tag{A.7}$$

The reactive power flow can be obtained from the imaginary part of equation (A.4) as:

$$Q = -\left[\frac{V_S V_R}{Z} \sin(\delta - \psi) + \frac{V_R^2}{Z} \sin\psi\right] \tag{A.8}$$

Again neglecting the resistance for a transmission line the reactive power flow can be given as:

$$Q = -\left[\frac{V_S V_R}{X}(-\cos\delta) + \frac{V_R^2}{X}\right] = \frac{V_S V_R}{X}\cos\delta - \frac{V_R^2}{X} \tag{A.9}$$

$$Q = \frac{V_R[V_S \cos\delta - V_R]}{X} \tag{A.10}$$

If the reactive power flow is considered for very small angles, i.e. $\cos\delta = 1$, then we can show the reactive power as:

$$Q = \frac{V_R[V_S - V_R]}{X} \tag{A.11}$$

From equations (A.7) and (A.11) we can see that active power flow (P) and angle (δ) are closely coupled, as are reactive power flow (Q) and voltage (V). Also, we can see that reactive power transmission depends largely upon the voltage magnitude and flows from the highest voltage to the lowest voltage.

By considering the e.m.f. phasor diagram show in Figure (A.2), which corresponds to the line given in Figure (A.1), the voltage drop across a transmission line may be found. An approximate value of the voltage drop may be found as:

$$\Delta V = V_S - V_R \approx IR\cos\phi + IX\sin\phi \tag{A.12}$$

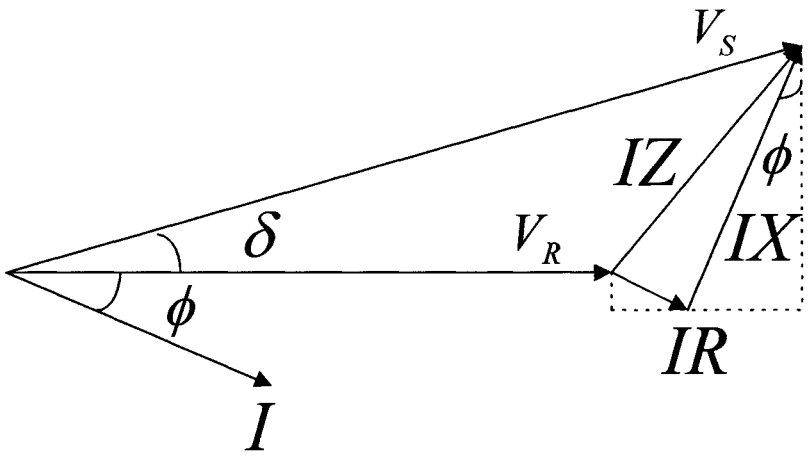


Figure A.2

Substituting $I\cos\phi = \frac{P}{V_R}$ and $I\sin\phi = \frac{Q}{V_R}$ into equation (A.12) yields:

$$\Delta V \approx \frac{RP + XQ}{V_R} \tag{A.13}$$

If the effect of resistance is neglected, equation (A.13) reduces to:

$$\Delta V \approx \frac{XQ}{V_R} \tag{A.14}$$

Using equation (A.14), the relative voltage drop across the line of Figure A.1 may be expressed as:

$$\frac{\Delta V}{V_R} \approx \frac{XQ}{V_R^2} \tag{A.15}$$

If a reactive power (VAr) compensator is employed to control the voltage at the receiving-end, equation (A.15) is modified to:

$$\frac{\Delta V}{V_R} \approx \frac{X(Q-Q_C)}{V_R^2} \tag{A.16}$$

Where Q_C is the reactive power supplied by the VAr compensator. This equation illustrates that by controlling the VAr compensator output (Q_C), it is possible to limit or even eliminate the voltage drop due to variation not only in Q but also P.

A.2 THE GENERATION AND ABSORPTION OF REACTIVE POWER

The technique of shunt VAr compensation can be explained by first considering some basic facts. Overhead lines absorb reactive power when fully loaded. A line with a current I A and a line reactance of X_L /phase absorbs $I^2 X_L$ VArs/phase. On light loads, the shunt capacitance of a long line may become predominant and the line becomes a VAr generator producing V^2/X_C VArs/phase. The shunt capacitance of a cable is very large as compared to that of an overhead line. Consequently they are not used for long a.c. transmission.

Shunt capacitors absorb leading VArs whereas reactors are used to absorb lagging VArs. The number of these elements connected to the system may be controlled in order to supply the required VAr demand to maintain a specified value of voltage.

The voltage at the mid point of a transmission line can be maintained constant by using a dynamic shunt VAr compensator connected at this point. This can be illustrated by considering equation (A.16). This means that the line is sectioned

into two 'independent' equal halves. Thus, assuming $V_S = V_R = V_M$ (mid-point voltage) = V, the power equation for each half, using equation (A.7) may be written as:

$$P = \frac{V^2}{\frac{X}{2}} \sin\frac{\delta}{2} = 2\frac{V^2}{X}\sin\frac{\delta}{2} \qquad \text{(A.17)}$$

This gives $P_{max} = \frac{2V^2}{X}$ which is twice the amount as without compensation. Therefore, the maximum transmissible power is doubled.

APPENDIX B

4-LEVEL AND 5-LEVEL VSI TOPOLOGY REDUNDANCY INVESTIGATION

The redundancy investigations presented in Chapter 4 illustrate the device failure analysis applied to the 2, 3 and 6-level VSI topologies. The phase limbs, output phase voltages and space vector nodal planes for the 4 and 5-level topologies, also investigated throughout the project, are given below in Figures B.1-B.3 and B.4-B.6 respectively. Conventional DCMLI switching strategies are illustrated in Table B.1 for the 4-level VSI and Table B.4 for the 5-level VSI. As with the redundancy analysis presented in Chapter 4, the switching states 'lost' due to short-circuit or open-circuit device faults are given in Tables B.2-B.3 and B.5-B.6 for the 4 and 5-level topologies respectively.

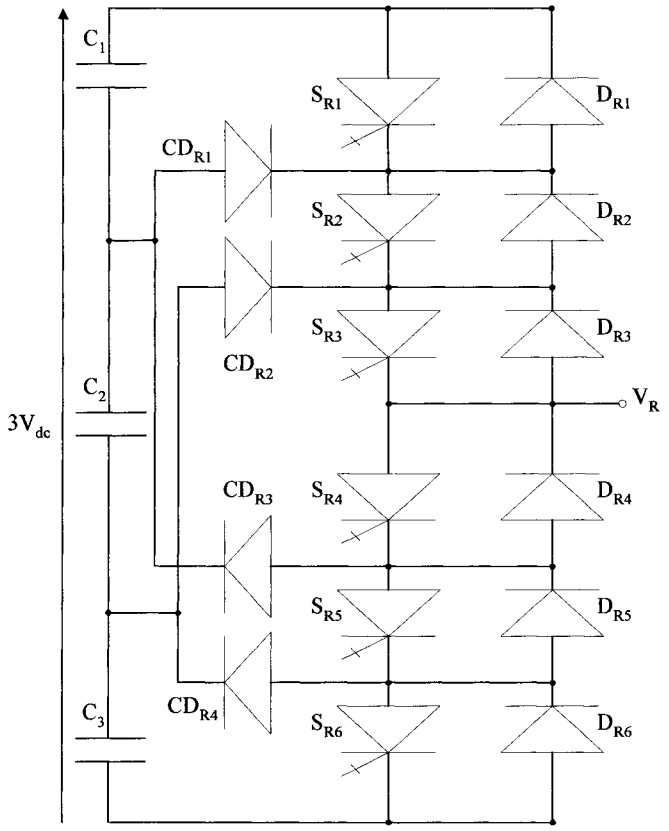


Figure B.1 – Four-level VSI phase limb

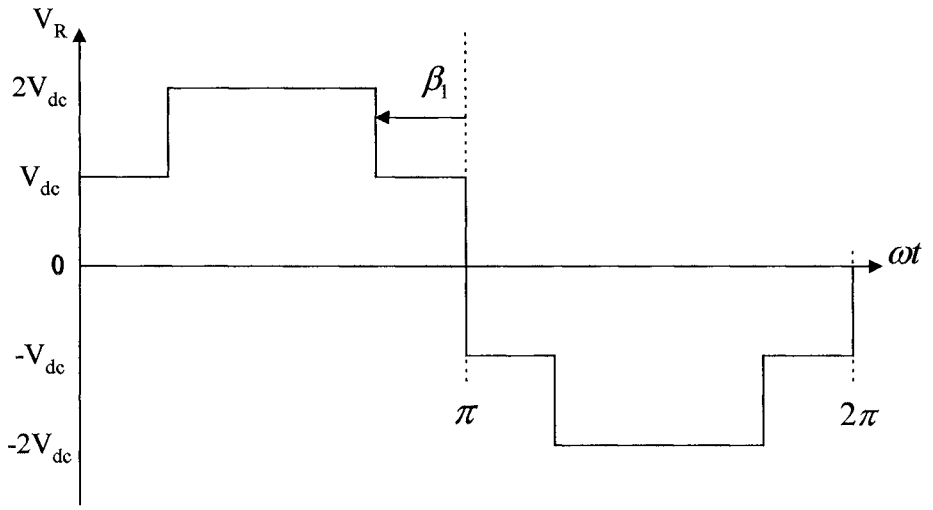


Figure B.2 – Four-level output phase voltage

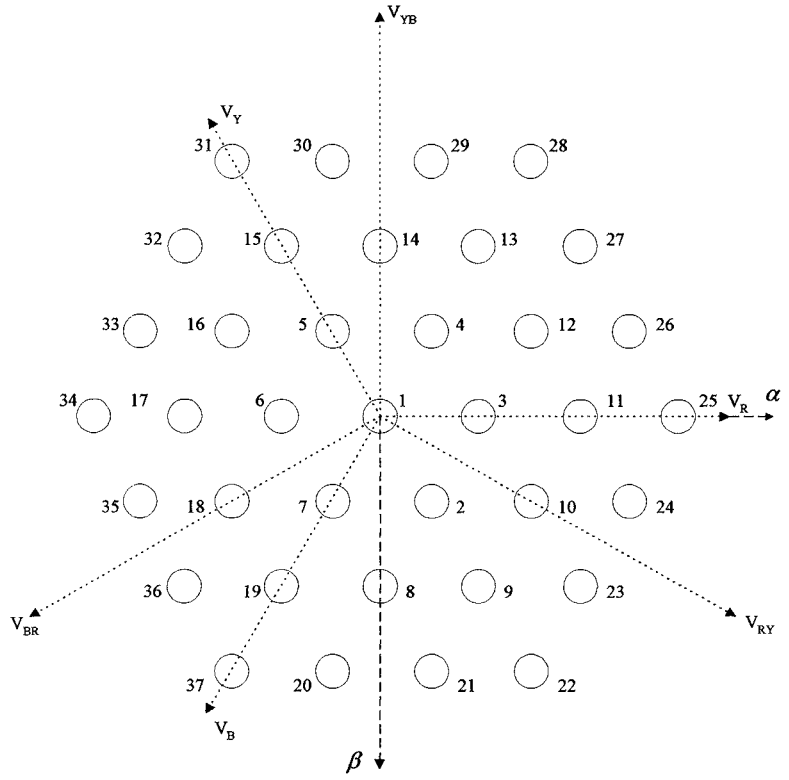


Figure B.3 – Four-level Space Vector Nodal Plane

Switching State (1 = on, 0 = off)						Output Voltage Level
S_{R1}	S_{R2}	S_{R3}	S_{R4}	S_{R5}	S_{R6}	V_{RN}
1	1	1	0	0	0	$+2\ V_{dc}$
0	1	1	1	0	0	$+\ V_{dc}$
0	0	1	1	1	0	$-\ V_{dc}$
0	0	0	1	1	1	$-2\ V_{dc}$

Table B.1 – Standard switching scheme for 4-level DCMLI

Device	Number of states lost	Number of active vectors lost	Lost states of form
S_{R1}, S_{R5}	16	2	(1XX)
S_{R2}, S_{R6}	16	2	(-1XX)
S_{R3}, CD_{R4}	16	7	(-2XX)
S_{R4}, CD_{R1}	16	7	(2XX)
CD_{R2}	32	14	(2XX), (1XX)
CD_{R3}	32	14	(-2XX), (-1XX)

Table B.2 - States lost due to short-circuit device failures (4-level VSI)

Device	Number of states lost	Number of active vectors lost	Lost states of form
S_{R1}	16	7	(2XX)
S_{R2}	32	14	(2XX), (1XX)
S_{R3}	48	23	(2XX), (1XX), (-1XX)
S_{R4}	48	23	(-2XX), (-1XX), (1XX)
S_{R5}	32	14	(-2XX), (-1XX)
S_{R6}	16	7	(-2XX)
CD_{R1}, CD_{R3}	16	2	(1XX)
CD_{R2}, CD_{R4}	16	2	(-1XX)

Table B.3 - States lost due to open-circuit device failures (4-level VSI)

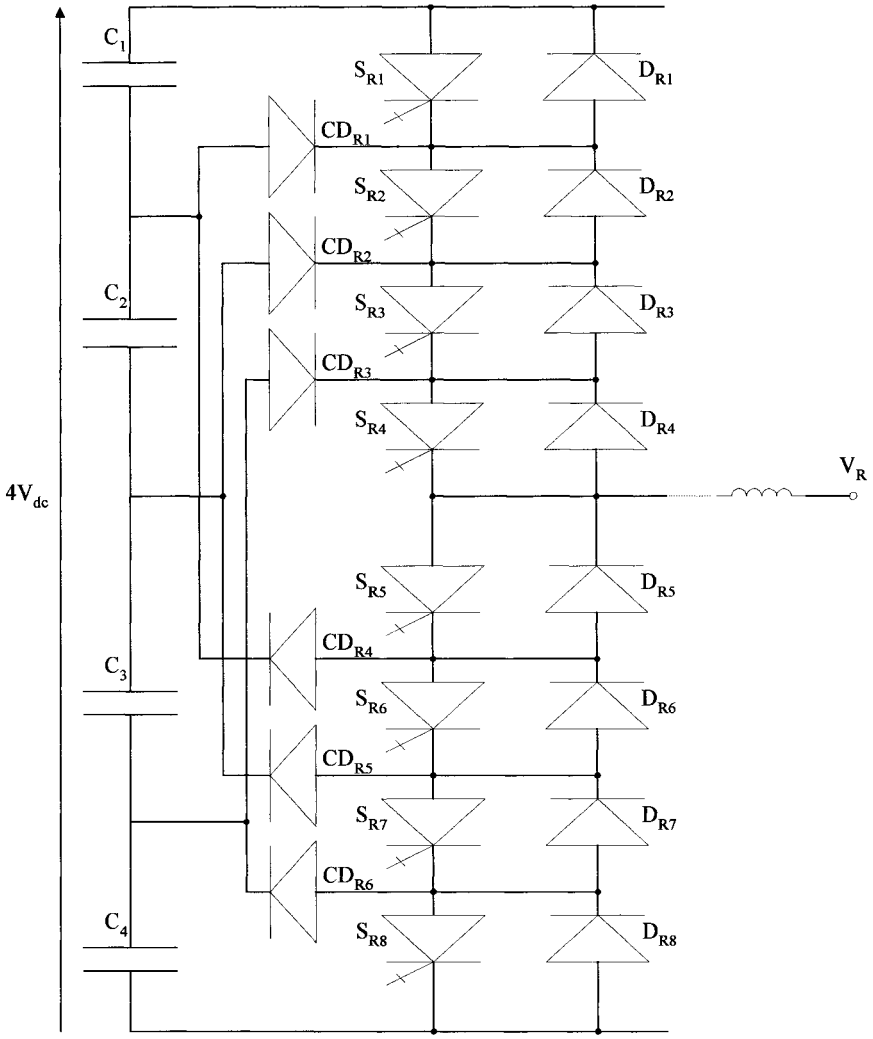


Figure B.4 – Five-level VSI phase limb

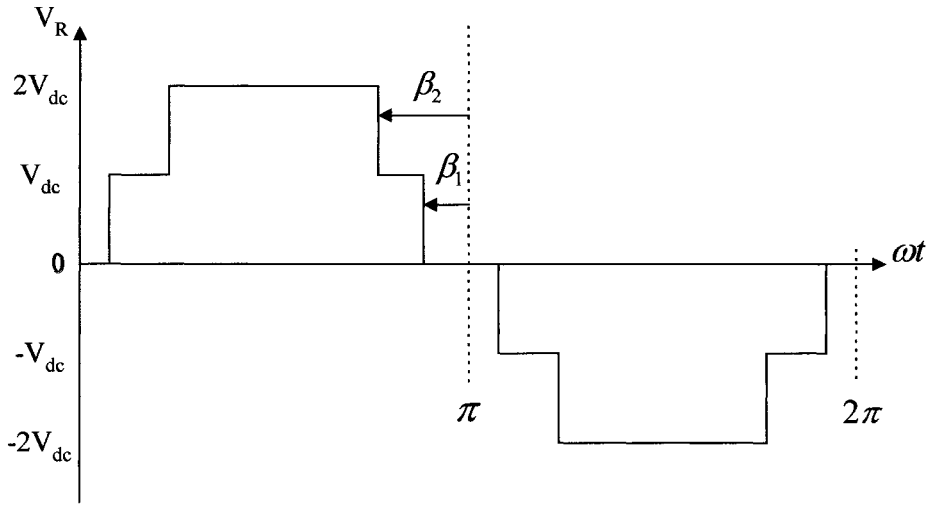


Figure B.5 – Five-level output phase voltage

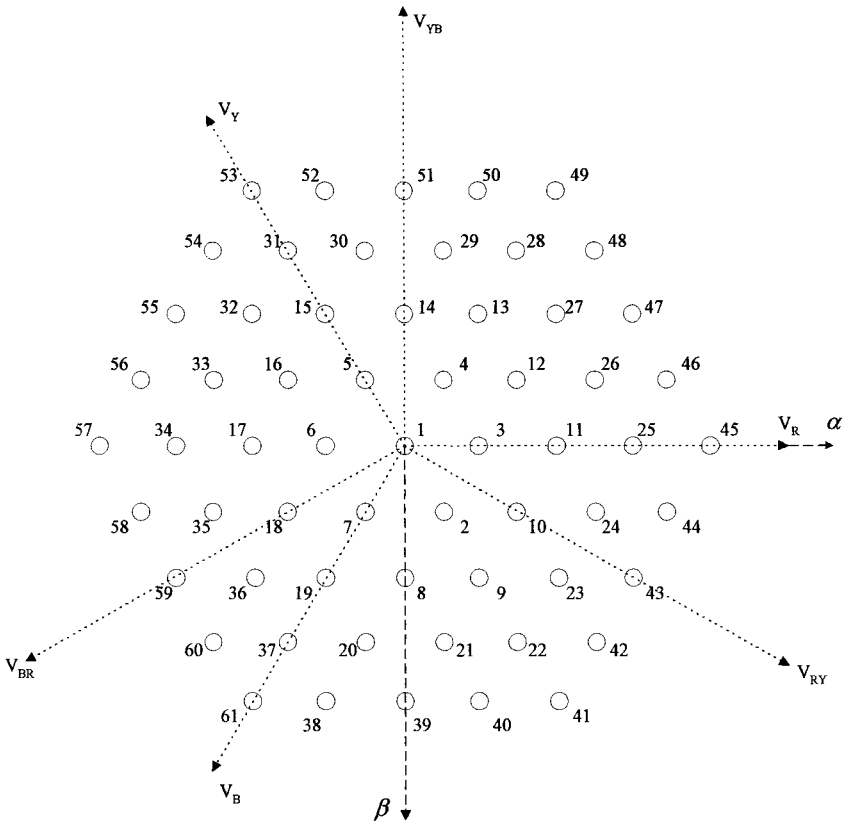


Figure B.6 – Five-level Space Vector Nodal Plane

Switching State (1 = on, 0 = off)								Output Voltage Level
S_{R1}	S_{R2}	S_{R3}	S_{R4}	S_{R5}	S_{R6}	S_{R7}	S_{R8}	V_{RN}
1	1	1	1	0	0	0	0	$+2V_{dc}$
0	1	1	1	1	0	0	0	$+V_{dc}$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_{dc}$
0	0	0	0	1	1	1	1	$-2V_{dc}$

Table B.4 – Standard switching scheme for 5-level DCMLI

Device	Number of states lost	Number of active vectors lost	Lost states of form
S_{R1}, S_{R6}	25	2	(1XX)
S_{R2}, S_{R7}	25	2	(0XX)
S_{R3}, S_{R8}	25	2	(-1XX)
S_{R4}, CD_{R6}	25	9	(-2XX)
S_{R5}, CD_{R1}	25	9	(2XX)
CD_{R2}	50	18	(2XX), (1XX)
CD_{R3}	75	27	(2XX), (1XX), (0XX)
CD_{R4}	75	27	(-2XX), (-1XX), (0XX)
CD_{R5}	50	18	(-2XX), (-1XX)

Table B.5 - States lost due to short-circuit device failures (5-level VSI)

Device	Number of states lost	Number of active vectors lost	Lost states of form
S_{R1}	25	9	(2XX)
S_{R2}	50	18	(2XX), (1XX)
S_{R3}	75	27	(2XX), (1XX), (0XX)
S_{R4}	100	36	(2XX), (1XX), (0XX), (-1XX)
S_{R5}	100	36	(-2XX), (-1XX), (0XX), (1XX)
S_{R6}	75	27	(-2XX), (-1XX), (0XX)
S_{R7}	50	18	(-2XX), (-1XX)
S_{R8}	25	9	(-2XX)
CD_{R1}, CD_{R4}	25	2	(1XX)
CD_{R2}, CD_{R5}	25	2	(0XX)
CD_{R3}, CD_{R6}	25	2	(-1XX)

Table B.6 - States lost due to open-circuit device failures (5-level VSI)

APPENDIX C

FOURIER ANALYSIS FOR VSI VOLTAGE WAVEFORMS

The Fourier series can be defined in the form:

$$f(x) = \frac{1}{2}a_0 + \sum_{n=1}^{\infty}\{a_n \cos n(x) + b_n \sin n(x)\} \tag{C.1}$$

Where n = a positive integer.

The Fourier coefficients can then be expressed as:

$$a_0 = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x)dx \tag{C.2}$$

$$a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x)\cos n(x)dx \tag{C.3}$$

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x)\sin n(x)dx \tag{C.4}$$

Using the above Fourier coefficients a Fourier series can be obtained to represent a periodic function of period 2π. It should be noted that full coefficient derivation can be a long process and can be greatly simplified by observation of the function $f(x)$. This technique of mathematical simplification is presented below.

Considering the 3-level FFM waveform shown in Figure C.1, the derivation of the Fourier series for the phase voltage waveform (VRN) can be simplified by observation of the periodic function.

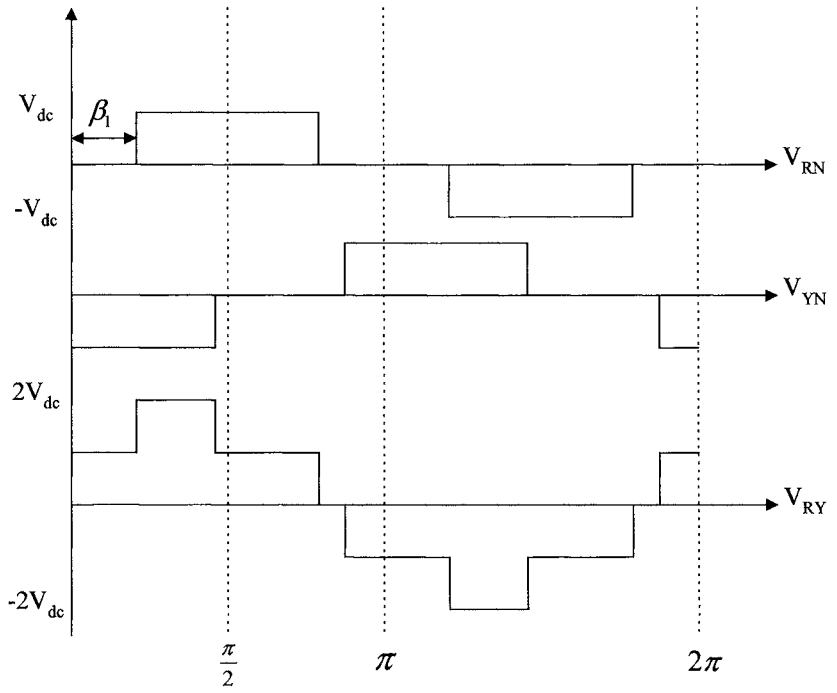


Figure C.1 – Phase and Line voltage for the 3-level VSI (FFM)

The waveform exhibits symmetry about π and therefore also the origin. This can be illustrated as:

$$f(-x) = -f(x) \tag{C.5}$$

Therefore the waveshape is an odd function and contains sine terms only. Also as no d.c. shift appears in the function the Fourier coefficients can be defined as:

$$a_0 = 0, \qquad a_n = 0 \tag{C.6}$$

Observing that the waveshape function exhibits ¼ cycle symmetry, a ¼ - range series analysis can be performed using:

$$b_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} f(x)\sin n(x)dx \tag{C.7}$$

Using Figure C.1, the b_n coefficient for the 3-level FFM phase voltage waveform can then be derived as:

$$b_n = \frac{4}{\pi} \cdot \left\{ \int_0^{\beta_1} 0.\sin n(x)dx + \int_{\beta_1}^{\frac{\pi}{2}} V_{dc} \sin n(x)dx \right\} \tag{C.8}$$

$$b_n = \frac{4}{\pi} \cdot \left\{ \left[\frac{-V_{dc} \cos n(x)}{n} \right]_{\beta_1}^{\frac{\pi}{2}} \right\} \tag{C.9}$$

$$b_n = \frac{4 \cdot V_{dc}}{\pi \cdot n} \cdot \left\{ \cos n\left(\frac{\pi}{2}\right) + \cos n(\beta_1) \right\} \tag{C.10}$$

Which simplifies to:

$$b_n = \frac{4 \cdot V_{dc}}{\pi \cdot n} \cdot \cos n(\beta_1) \qquad \text{for odd n} \tag{C.11}$$

and $$|b_n| = 0 \qquad \text{for even n} \tag{C.12}$$

The 3-level FFM phase voltage for the Red phase can then be written as:

$$V_{RN}(\omega t) = \frac{4 \cdot V_{dc}}{\pi} \cdot \sum_{n=1}^{\infty} \frac{1}{n} \left[\cos n(\beta_1) \right] \cdot \sin n(\omega t) \tag{C.13}$$

$$V_{RN}(\omega t) = \frac{4 \cdot V_{dc}}{\pi} \cdot \left\{ \cos(\beta_1) \cdot \sin(\omega t) + \frac{1}{3} \cos 3(\beta_1) \cdot \sin 3(\omega t) + ... \right.$$
$$\left. + \frac{1}{5} \cos 5(\beta_1) \cdot \sin 5(\omega t) + \frac{1}{7} \cos 7(\beta_1) \cdot \sin 7(\omega t) + ... \right\} \tag{C.14}$$

The line voltage of the 3-level VSI FFM can also be derived from Fourier analysis as:

$$V_{RN} = \sum_{n=1}^{\infty} b_n \sin(n\omega t) \tag{C.15}$$

$$V_{YN} = \sum_{n=1}^{\infty} b_n \sin n\left(\omega t - \frac{2\pi}{3}\right) \tag{C.16}$$

Using b_n as derived in equation C.11, the line-line voltage can be written as:

$$V_{RY} = \frac{4 \cdot V_{dc}}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} .\cos(n\beta_1)\left[\sin(n\omega t) - \sin n\left(\omega t - \frac{2\pi}{3}\right)\right] \tag{C.17}$$

$$V_{RY} = \frac{4 \cdot V_{dc} \cdot \sqrt{3}}{\pi} \cdot \left[\cos\beta_1 \cos\left(\omega t - \frac{\pi}{3}\right) - \frac{1}{5}\cos 5\beta_1 \cos 5\left(\omega t - \frac{\pi}{3}\right) + \frac{1}{7}\cos 7\beta_1 \cos 7\left(\omega t - \frac{\pi}{3}\right) - \frac{1}{11}\cos 11\beta_1 \cos 11\left(\omega t - \frac{\pi}{3}\right) + ...\right] \tag{C.18}$$

$$V_{RY} = \frac{4 \cdot V_{dc} \cdot \sqrt{3}}{\pi} \cdot \left[\cos\beta_1 \sin\left(\omega t + \frac{\pi}{6}\right) - \frac{1}{5}\cos 5\beta_1 \sin 5\left(\omega t + \frac{\pi}{6}\right) + \frac{1}{7}\cos 7\beta_1 \sin 7\left(\omega t + \frac{\pi}{6}\right) + \frac{1}{11}\cos 11\beta_1 \sin 11\left(\omega t + \frac{\pi}{6}\right) + ...\right] \tag{C.19}$$

Similarly for the 2-level VSI (FFM) phase and line voltage waveforms shown in Figure C.2, we can observe an odd function with ¼ - cycle symmetry.

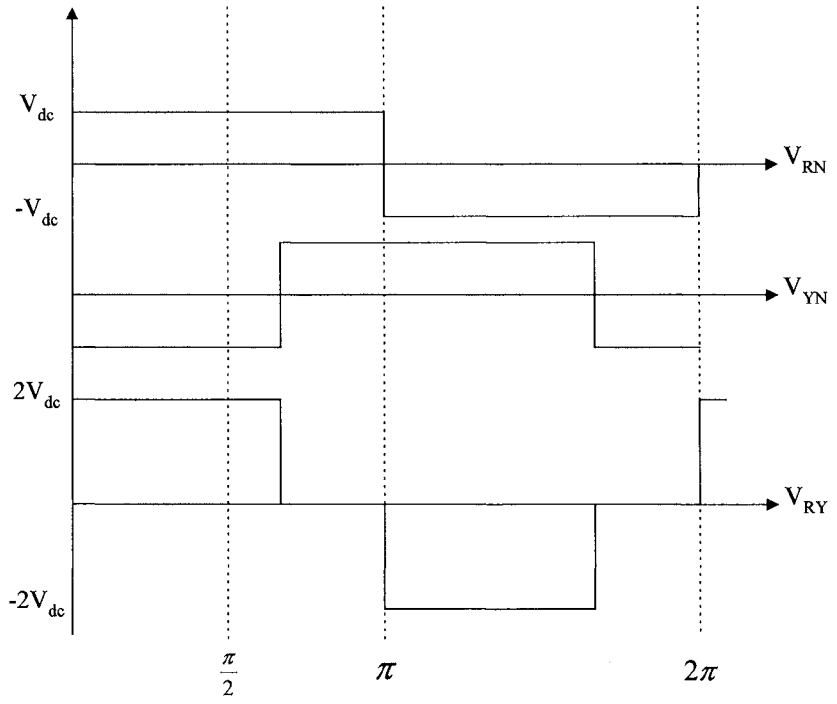


Figure C.2 – Phase and Line voltage for the 2-level VSI (FFM)

Therefore, from Fourier analysis:

$$a_0 = 0\,, \qquad a_n = 0 \tag{C.20}$$

$$b_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} f(x)\sin n(x)dx \tag{C.21}$$

Using Figure C.2, the b_n coefficient for the 2-level FFM phase voltage waveform can then be derived as:

$$b_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} V_{dc}\sin n(x)dx \tag{C.22}$$

$$b_n = \frac{4}{\pi} \cdot \left\{ \left[\frac{-V_{dc} \cos n(x)}{n} \right]_0^{\frac{\pi}{2}} \right\} \tag{C.23}$$

$$b_n = \frac{4 \cdot V_{dc}}{\pi \cdot n} \cdot \left\{ -\cos n\left(\frac{\pi}{2}\right) + \cos n(0) \right\} \tag{C.24}$$

Which simplifies to:

$$b_n = \frac{4 \cdot V_{dc}}{\pi \cdot n} \qquad \text{for odd n} \tag{C.25}$$

and $|b_n| = 0$ for even n (C.26)

Substituting this coefficient into the Fourier expression, the 2-level FFM phase voltage for the Red phase can then be written as:

$$V_{RN}(\omega t) = \frac{4 \cdot V_{dc}}{\pi} \cdot \left\{ \sin(\omega t) + \frac{1}{3}\sin 3(\omega t) + \frac{1}{5}\sin 5(\omega t) + \frac{1}{7}\sin 7(\omega t) + ... \right\} \tag{C.27}$$

The line voltage of the 2-level VSI FFM can be derived from Fourier analysis as:

$$V_{RN} = \frac{4 \cdot V_{dc}}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \cdot \sin(n\omega t) \tag{C.28}$$

$$V_{YN} = \frac{4 \cdot V_{dc}}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \cdot \sin n\left(\omega t - \frac{2\pi}{3}\right) \tag{C.29}$$

Initially considering the fundamental component, the line-line voltage can be derived as:

$$V_{RY(1)} = \frac{4 \cdot V_{dc}}{\pi}\left\{\sin(\omega t) - \sin\left(\omega t - \frac{2\pi}{3}\right)\right\} \tag{C.30}$$

Then using the following trigonometric identity:

$$\sin A - \sin B = 2\cos\frac{(A+B)}{2} \cdot \sin\frac{(A-B)}{2} \tag{C.31}$$

We can derive:

$$V_{RY(1)} = \frac{4 \cdot V_{dc}}{\pi}\left\{2\cos\frac{\left(\omega t + \omega t - \frac{2\pi}{3}\right)}{2} \cdot \sin\frac{\left(\omega t + \omega t - \frac{2\pi}{3}\right)}{2}\right\} \tag{C.32}$$

Which simplifies to:

$$V_{RY(1)} = \frac{4 \cdot V_{dc}}{\pi}\left\{2\cos\left(\omega t - \frac{\pi}{3}\right) \cdot \sin\left(\frac{\pi}{3}\right)\right\} \tag{C.33}$$

and using the relationships:

$$\sin\left(\frac{\pi}{3}\right) = \cos\left(\frac{\pi}{6}\right) \tag{C.34}$$

$$\cos\left(\omega t - \frac{\pi}{3}\right) = \sin\left(\omega t + \frac{\pi}{6}\right) \tag{C.35}$$

The fundamental component of the 2-level (FFM) line-line voltage can be given as:

$$V_{RY(1)} = \frac{4 \cdot V_{dc}}{\pi}\left\{2\cos\left(\frac{\pi}{6}\right) \cdot \sin\left(\omega t + \frac{\pi}{6}\right)\right\} \tag{C.36}$$

Where, $$2\cos\left(\frac{\pi}{6}\right) = \sqrt{3} \tag{C.37}$$

Therefore, the simplified fundamental component can be given as:

$$V_{RY(1)} = \frac{4 \cdot V_{dc} \cdot \sqrt{3}}{\pi} \cdot \sin\left(\omega t + \frac{\pi}{6}\right) \tag{C.38}$$

The full Fourier series for the line-line voltage can then be shown as:

$$V_{RY} = \frac{4 \cdot V_{dc}}{\pi \cdot n} \cdot \sum_{n=1}^{\infty} \cos n\left(\frac{\pi}{6}\right) \cdot \sin n\left(\omega t + \frac{\pi}{6}\right) \tag{C.39}$$

APPENDIX D

EXPERIMENTAL MODEL DESIGN AND CONSTRUCTION

D.1 DESIGN OF SINGLE IGBT DRIVER CIRCUIT

As presented in Chapter 7 the SEMIKRON SKHI 21 hybrid double driver unit was not suitable for demonstrating the adaptive topology due to an inherent interlocking protection facility. To overcome this difficulty in implementing the adaptive strategy, a single IGBT driver based on standard discrete components was utilised. A brief overview of the design is illustrated below.

By using two transformers the gate drive circuit provides isolation between the control signal and the IGBT. One transformer transmits power from the low-side circuit and the second transformer transmits the gate-drive signal. A block diagram of the main operational components of the driver is shown in Figure D.1.

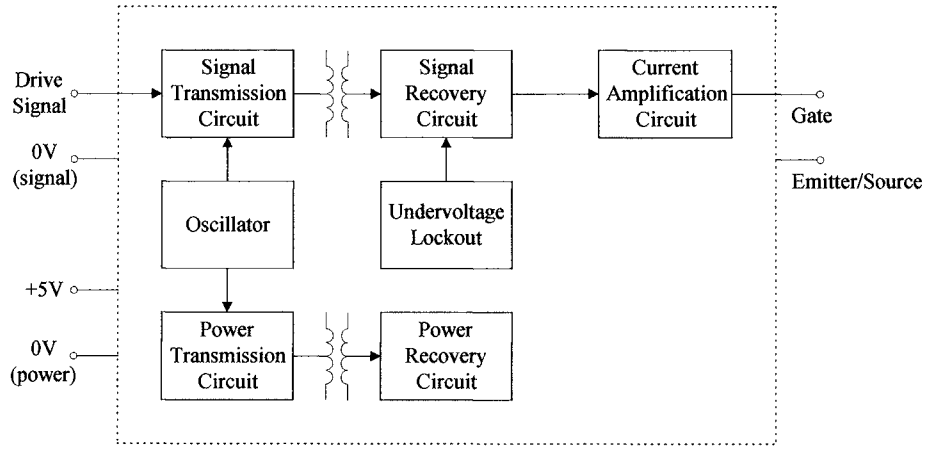


Figure D.1 – Block Diagram of the Single IGBT Gate Drive Circuit

The six required drivers for the red phase switching devices and DPPS devices were mounted on one PCB, as illustrated in the digital image of the completed power circuit shown in Chapter 7, Figure 7.3. This minimises the stray inductance associated with the wiring between the driver and the device and also assists in

reducing the switching noise problem. Both forms of driver boards and associated drivers were mounted on the side channels of the SEMIKRON P3 heatsinks. Again this was to develop a modular system, as each phase now had full power circuit device components and associated drivers mounted on the same 'phase' heatsink. Each phase was therefore an integral part of the three-phase system, but could be utilised as an independent single-phase 3-level inverter bridge.

D.2 IGBT AND DRIVER CIRCUIT TESTING

Before the full inverter was constructed a test circuit was required for the IGBT modules, IGBT discretes, SKHI 21 dual driver units and the constructed single IGBT drivers. As a number of the components to be used have been selected due to their current availability and the limited project resources for hardware, it was essential that these were tested for functionality before the full system was constructed. A simple test circuit was constructed as shown in Figure D.2. Each IGBT device, module and single, was tested together with the driver to be used for that particular device.

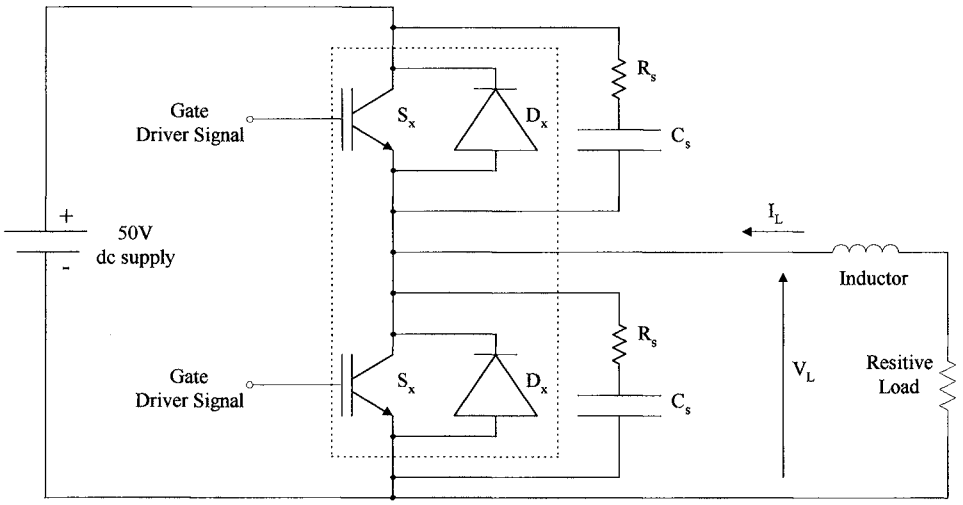


Figure D.2 – IGBT operation testing

D.3 THE DC LINK AND ASSOCIATED '3-LEVEL' CAPACITOR BANK

The layout of the d.c. link, illustrating the 3-phase variac and diode bridge with series 25 mH inductor and 2000 μF capacitor, is shown in Figure D.3. The capacitors used for the d.c. link and for the 3-level capacitor unit were rated at 1000 μF and 1000 V. The dc link output capacitance was constructed from two 1000 μF capacitors in parallel, $C_{Total} = C_1 + C_2$.

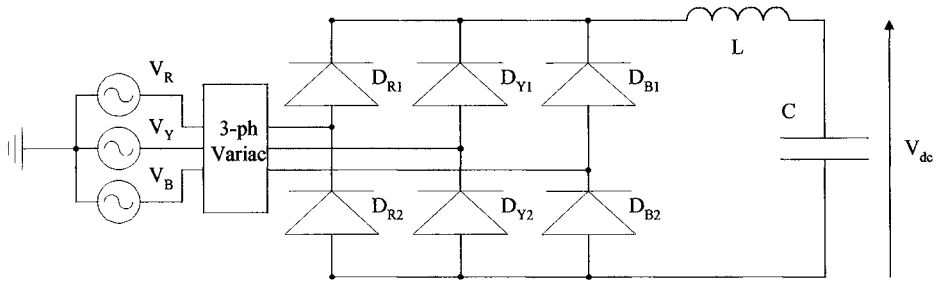


Figure D.3 – D.C. link constructed from 3-ph diode bridge

The 3-level capacitor bank unit is constructed of two groups of capacitors, upper and lower, connected in series with tee-off points providing the required positive, zero and negative voltage nodes. The input and output connections for the complete capacitor unit are shown in Figure D.4. The interconnection of the three upper and three lower series connected capacitors offers a value of 333 μF of each level for the hardware model. This corresponds to the capacitor values used for the software model simulations of the system.

The complete capacitor unit was mounted on a SEMIKRON P3 heatsink as shown in Figure D.5. The modular connections of the upper and lower sections of the 3-level capacitor bank enabled a variable capacitance for the experimental procedures to observe the effect of the capacitance upon the performance.

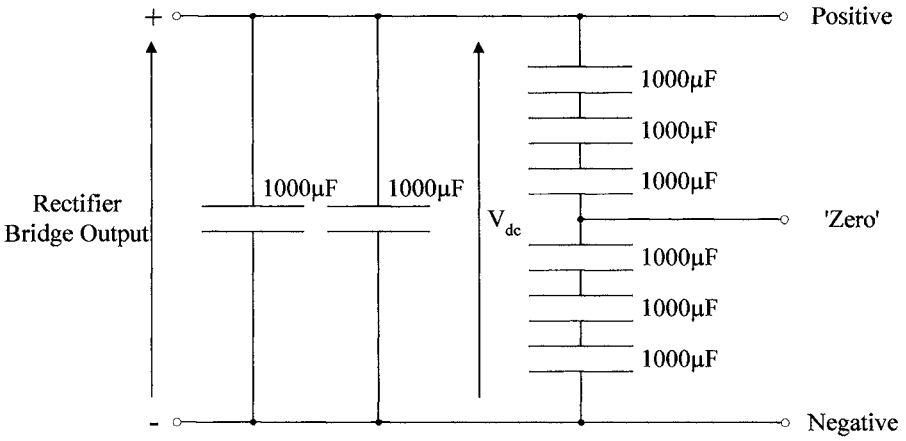


Figure D.4 – The complete d.c. link and 3-level capacitor unit

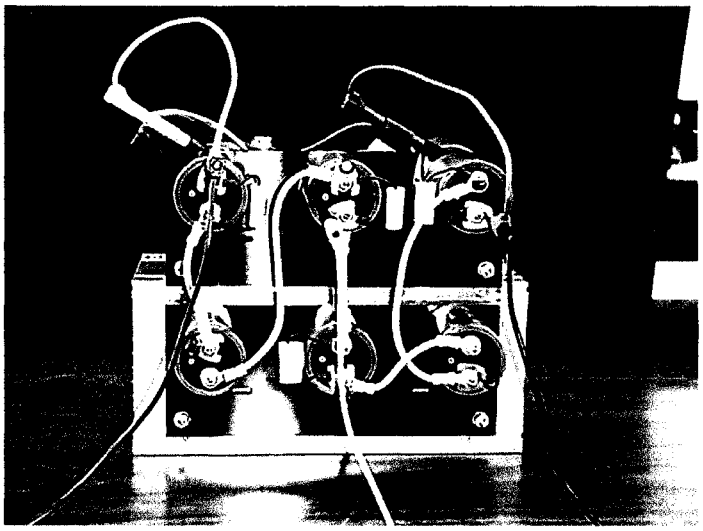


Figure D.5 – Digital image of the Complete Capacitor Unit

APPENDIX E

IMPLEMENTING THE ADAPTIVE DPPS CONTROL ON THE TMS320F240 DSP

As presented in Chapter 7 the adaptive DPPS control switching strategy for the 3-level VSI was implemented on a TMS320F240 digital signal processor (DSP) evaluation module (EVM). The adaptive controller mainly consists of reference sinewaves (generated from interpolated lookup tables) and the 3-level to 2-level adaptive DPPS switching control scheme implementing a SHEM scheme. This Appendix briefly describes the software routines required for the experimental implementation of the adaptive DPPS scheme. Further details on initialisation and programming the TMS320F240 DSP can be found in the Texas software application notes [61].

E.1 GENERATING THE REFERENCE SINEWAVE

As presented in Chapter 7 the experimental model was implemented with no phase-locked loop (PLL) and therefore required some form of angular reference for the 3-phases of the 3-level VSI. As illustrated in the development of the experimental model a methodology of '3-phase' timing diagrams was adopted such that only one reference sinewave was required. It should be noted that this technique would only be suitable for an assumed ideally balanced system. The generated sinewave was output using the DAC's provided on the EVM board. This enabled debugging of the firing signals before the DSP controller was implemented to the main power circuit.

To illustrate the implementation of a highly interpolated sinewave, to provide a precise angular reference for the SHEM switching angles, an example of the code is given below. Code is also provided to illustrate the mechanism of outputting the sinewave through the digital to analogue converters (DAC's) provided on the EVM board. The lookup table is truncated to the first 90° of the generated sinewave and for full implementation would need extending to 360°.

E.1.1 Section of assembly language code for generating sinewave

```
SINE        LDP #0
            LACC MODREG1        ;ACC loaded with the counting register
            ADD FREQSTEP1       ;Counting Register increased by specific step
            SACL MODREG1        ;Store the updated counter value
            LACC MODREG1,8      ;Reload the new ctr value but shift left by 8 bits
            SACH TABLE          ;Store the high bit pointer to lookup table
            SFR                 ;Shift the value to the right convert to Q15
            AND #07FFFh         ;Make sure the Q15 value is positive
            SACL REMAINDER      ;Store the fractional value of the counting register
            LACC TABLE          ;Load the accumulator with the proper index value
            ADD TOPTABLE        ;Displace the ACC with the starting address
            TBLR VALUE          ;Read the value from the table and store into VALUE
            ADD #1              ;Increment the ACC to the next address
            TBLR NEXTVALUE      ;Read the next value from the table and
            LACC NEXTVALUE      ;Load the ACC with NEXTVALUE
            SUB VALUE           ;Subtract the previous value
            SACL DIFFERENCE     ;Store the difference between the values
            LT DIFFERENCE       ;Load the TREG with DIFFERENCE
            MPY REMAINDER       ;Multiply the DIFFERENCE with REMAINDER
            PAC                 ;Move the product to the ACC
            SACH REMAINDER,1    ;Store the upper byte and shift left by 1, Q15
            LACC REMAINDER      ;Load ACC with new REMAINDER
            ADD VALUE           ;Add VALUE to get the new interpolated value
            SACL VALUE          ;Store the interpolated value into VALUE
            LT VALUE            ;Load the TREG with the new interpolated VALUE
            MPY MAG1            ;Multiply VALUE by a magnitude
            PAC                 ;Move the product to ACC
            SACH DAC0VAL,1      ;Store the new value, shift to get Q15

;=============================================================================

            LDP #0              ;This section outputs the SINE wave to the DAC
            LACC DAC0VAL        ;ACC = DAC0VAL - entry from the lookup table
            ADD #8000h          ;Displace the value half the maximum
            SFR                 ;Shift over 4 places since the DAC is 12bits
            SFR                 ;
            SFR
            SFR
            SACL DAC0VAL        ;Store the new 12 bit value into DAC0VAL
            OUT DAC0VAL,DAC0    ;Stores the 12 bit value into DAC0 register
            OUT DAC0VAL,DACUPDATE   ;Causes the DAC to output the value


;=============================================================================
                                ; Lookup table for angular reference.

        ;SINVAL      ; Index  Angle   Sin(Angle)
STABLE
        .word 0      ; 0      0       0.0000
        .word 804    ; 1      1.41    0.0245
        .word 1608   ; 2      2.81    0.0491
        .word 2410   ; 3      4.22    0.0736
        .word 3212   ; 4      5.63    0.0980
        .word 4011   ; 5      7.03    0.1224
        .word 4808   ; 6      8.44    0.1467
        .word 5602   ; 7      9.84    0.1710
        .word 6393   ; 8      11.25   0.1951
```

```
.word 7179      ; 9     12.66   0.2191
.word 7962      ; 10    14.06   0.2430
.word 8739      ; 11    15.47   0.2667
.word 9512      ; 12    16.88   0.2903
.word 10278     ; 13    18.28   0.3137
.word 11039     ; 14    19.69   0.3369
.word 11793     ; 15    21.09   0.3599
.word 12539     ; 16    22.50   0.3827
.word 13279     ; 17    23.91   0.4052
.word 14010     ; 18    25.31   0.4276
.word 14732     ; 19    26.72   0.4496
.word 15446     ; 20    28.13   0.4714
.word 16151     ; 21    29.53   0.4929
.word 16846     ; 22    30.94   0.5141
.word 17530     ; 23    32.34   0.5350
.word 18204     ; 24    33.75   0.5556
.word 18868     ; 25    35.16   0.5758
.word 19519     ; 26    36.56   0.5957
.word 20159     ; 27    37.97   0.6152
.word 20787     ; 28    39.38   0.6344
.word 21403     ; 29    40.78   0.6532
.word 22005     ; 30    42.19   0.6716
.word 22594     ; 31    43.59   0.6895
.word 23170     ; 32    45.00   0.7071
.word 23731     ; 33    46.41   0.7242
.word 24279     ; 34    47.81   0.7410
.word 24811     ; 35    49.22   0.7572
.word 25329     ; 36    50.63   0.7730
.word 25832     ; 37    52.03   0.7883
.word 26319     ; 38    53.44   0.8032
.word 26790     ; 39    54.84   0.8176
.word 27245     ; 40    56.25   0.8315
.word 27683     ; 41    57.66   0.8449
.word 28105     ; 42    59.06   0.8577
.word 28510     ; 43    60.47   0.8701
.word 28898     ; 44    61.88   0.8819
.word 29268     ; 45    63.28   0.8932
.word 29621     ; 46    64.69   0.9040
.word 29956     ; 47    66.09   0.9142
.word 30273     ; 48    67.50   0.9239
.word 30571     ; 49    68.91   0.9330
.word 30852     ; 50    70.31   0.9415
.word 31113     ; 51    71.72   0.9495
.word 31356     ; 52    73.13   0.9569
.word 31580     ; 53    74.53   0.9638
.word 31785     ; 54    75.94   0.9700
.word 31971     ; 55    77.34   0.9757
.word 32137     ; 56    78.75   0.9808
.word 32285     ; 57    80.16   0.9853
.word 32412     ;58     81.56   0.9892
.word 32521     ;59     82.97   0.9925
.word 32609     ; 60    84.38   0.9952
.word 32678     ; 61    85.78   0.9973
.word 32728     ; 62    87.19   0.9988
.word 32757     ; 63    88.59   0.9997
.word 32767     ; 64    90.00   1.0000
```

E.2 DEVELOPING THE ADAPTIVE DPPS CODE FOR A 3-LEVEL SHEM TO 2-LEVEL SHEM SWITCHING STRATEGY

Adaptive switching control algorithms were developed for various FFM and SHEM strategies for both the 3-level and 2-level operation of the inverter. Code is presented below to demonstrate how the adaptive 3-level SHEM strategy was coded and implemented to provide firing signals.

E.2.1 Initialisation of switching strategy gradients

As shown in Figures 7.8 and 7.9, the required periodic cycle for the 3-phase timing diagrams to provide a 3-level SHEM angle was immediately split into the positive (0°-90°) and negative (0°-180°) halves. These were then split into positive and negative gradients by checking the generated sinewave angle with respect to the last angle. Flags were initialised to prevent repetitions of firing signals to the inverter devices. A section of the gradient and positive negative half cycle code is given below.

```
grad:     ldp    #0          ; check for positive or
                             ; negative gradient
          lacl   DAC0VAL     ; load current value of sinewave
          sub    lastvalue   ; subtract last value of sinewave
          blz    ng          ; if less than branch to negative gradient
pg:       ldp    #0          ; set up positive gradient
          splk   #01h, gflag ; initialize flag
          b      update      ; branch to update
ng:       ldp    #0          ; set up negative gradient
          splk   #00h, gflag ; initialize flag
update:   ldp    #0          ; load data page
          lacl   DAC0VAL     ; load current value of sinewave
          sacl   lastvalue   ; subtract last value of sinewave
pn:       ldp    #0          ; check if input sinusiod is
                             ; in positive of negative half cycle
          lacl   DAC0VAL     ; load current value of sinewave
          sub    #32767      ; subtract hex value equivalent to 180°
          bgz    nc          ; if greater than zero branch to negative
                             ; cycle of switching routine
pc:       ldp    #0          ; positive cycle routine
          bit    gflag3,15   ; initialize deadband flags
          bcnd   q1,TC       ; branch to quadrant 1 if positive gradient
          bit    gflag,15    ; initialize flags
          bcnd   q2,NTC      ; branch to quadrant 2 if negative gradient
```

E.2.2 Implementation of the adaptive 3-level SHEM strategy

The code for implementing the 3-level SHEM over the full 360° is very large and repetitive. Therefore, to demonstrate how the switching strategy is implemented a section of code in the positive half cycle and positive gradient is considered. Figure E.1 shows another step towards designing the code for the DSP implementation. The 'angular' sections are now labeled from a-h, which covers the first 90°. The methodology behind the design is to compare the current value of the generated sinewave to the specified angular value. The firing signals are determined as hexadecimal values representing the required 3-phase combinations and then output to the I/O ports of the DSP EVM. Deadbands are implemented within the code as delays to prevent shoot-through of the devices. The code illustrating the first four sections and the first three angles is provided below.

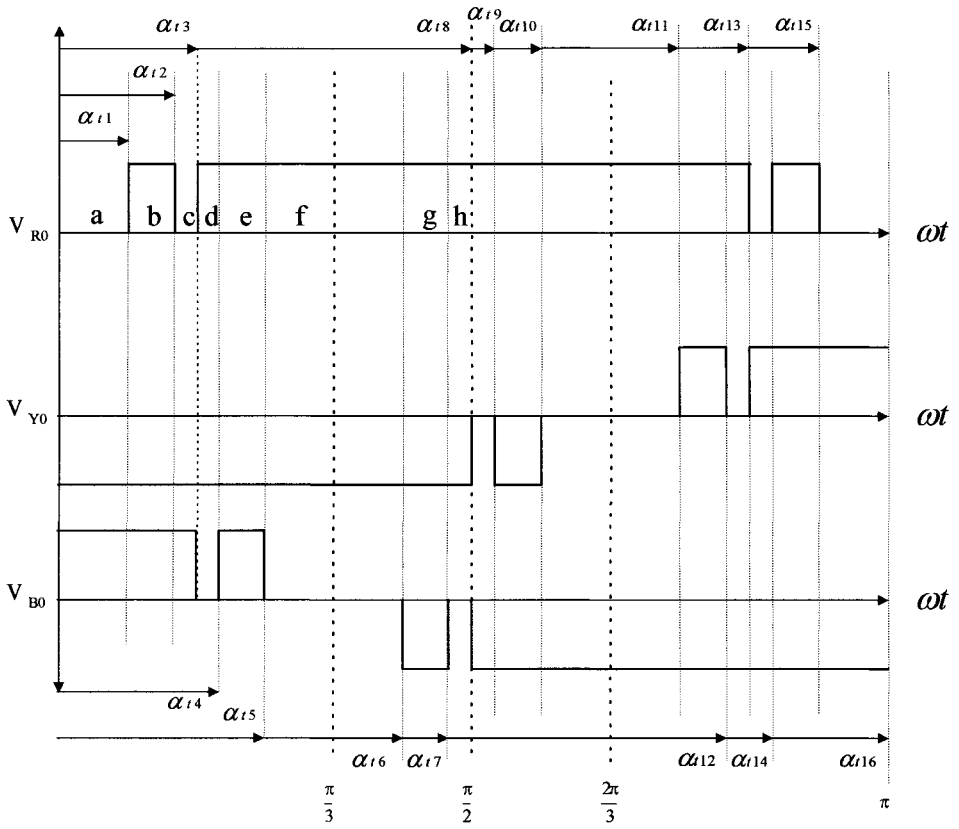


Figure E.1 - 3-level SHEM 'timing'/ switching diagram

```
q1:     ldp     #0              ; Quadrant 1, positive gradient
        splk    #00h,gflag3     ; 0° - 90°
        lacl    DAC0VAL         ; load current angle of sinewave
        sub     #7937           ; subtract hex value of 14.016°
        bgez    q1b             ; branch to section b

q1a:    ldp     #0e1h           ; load data page
        splk    #0f06h, PADATDIR ; output hex value of required switch
        splk    #0ff3ch, PBDATDIR ; combination for all 3 phases, for section
                                ; 'a' of switching/timing diagram
        b       cont            ; branch to continue ref. sinewave

q1b:    ldp     #0              ; load data page
        lacl    DAC0VAL         ; load current angle of sinewave
        sub     #13589          ; subtract hex value of 24.504°
        bgez    q1c             ; if greater than zero branch to section c

        ldp     #0              ; load data page
        bit     dbf,15          ; check deadband flag
        bcnd cont,TC            ; branch to continue to already sequenced
        splk    #01h, dbf       ; set deadband flag
        ldp     #0e1h           ; load data page
        splk    #0f02h, PADATDIR ; output hex value of switch combination
        call    deadb           ; call deadband routine

qq1b:   ldp     #0e1h           ; load data page
        splk    #0f03h, PADATDIR ; output hex value of switch combination
        splk    #0ff3ch, PBDATDIR ; output hex value of switch combination
        b       cont            ; branch to continue ref. sinewave

q1c:    ldp     #0              ; load data page
        lacl    DAC0VAL         ; load current angle of sinewave
        sub     #16383          ; subtract hex value of 30°
        bgez    q1d             ; if greater than zero branch to section d

        ldp     #0              ; load data page
        bit     dbf,14          ; check deadband flag
        bcnd    cont,TC         ; branch to continue to already sequenced
        splk    #02h, dbf       ; set deadband flag
        ldp     #0e1h           ; load data page
        splk    #0f02h, PADATDIR ; output hex value of switch combination
        call    deadb           ; call deadband routine

qq1c    ldp     #0e1h           ; load data page
        splk    #0f06h, PADATDIR ; output hex value of switch combination
        splk    #0ff3ch, PBDATDIR ; output hex value of switch combination
        b       cont            ; branch to continue ref. sinewave


deadb:  ldp     #0              ; load data page
        rpt     delay           ; repeat the number of times equal
        nop                     ; to delay, this variable sets up the
        ret                     ; device deadband time
```

E.2.3 Implementation of the 2-level SHEM strategy

Under abnormal operating conditions the adaptive 3-level scheme will revert to a 2-level SHEM switching strategy to 'recover' the harmonic performance. This switching scheme is implemented identically to the 3-level SHEM code provided in section E.2.2. However, for completeness a section of the code to show the first two switching angles of quadrant 1 is given below. For angular reference refer to Figure 7.10 in Chapter 7.

```
fq1:    ldp   #0                ; value is positive half cycle & positive
        splk  #00h,gflag3       ; gradient
        lacl  DAC0VAL           ; load current angle of sinewave
        sub   #4978             ; subtract hex value of 8.74°
        bgez  fq1b              ; if greater than zero branch to section b
fq1a:   ldp   #0                ; load data page
        bit   dbf,15            ; check deadband flag
        bcnd  cont,TC           ; branch to continue to already sequenced
        splk  #01h, dbf         ; set deadband flag
        ldp   #0e1h             ; load data page
        splk  #0f00h, PADATDIR  ; output hex value of switch combination
        call  deadb             ; call deadband routine
ffq1a:  ldp   #0e1h             ; load data page
        splk  #0f0ch, PADATDIR  ; output hex value of switch combination
        splk  #0ff3Ch, PBDATDIR ; output hex value of switch combination
        b     cont              ; branch to continue ref. sinewave
fq1b:   ldp   #0                ; load data page
        lacl  DAC0VAL           ; load current angle of sinewave
        sub   #13540            ; subtract hex value of 24.397°
        bgez  fq1c              ; if greater than zero branch to section c
        ldp   #0                ; load data page
        bit   dbf,14            ; check deadband flag
        bcnd  cont,TC           ; branch to continue to already sequenced
        splk  #02h, dbf         ; set deadband flag
        ldp   #0e1h             ; load data page
        splk  #0f00h, PADATDIR  ; output hex value of switch combination
        call  deadb             ; call deadband routine
ffq1b:  ldp   #0e1h             ; load data page
        splk  #0f03h, PADATDIR  ; output hex value of switch combination
        splk  #0ff3Ch, PBDATDIR ; output hex value of switch combination
        b     cont              ; branch to continue ref. sinewave
```

APPENDIX F: THREE-LEVEL VSI (SHEM) SWITCHING FUNCTION AND MODULATION ANALYSIS

Chapter 9 illustrates the phenomena of 3rd harmonic ripple on the upper and lower capacitors of the 3-level VSI. The switching function and harmonic interaction analysis for the 3-level SHEM VSI is derived below. A switch representation model of the 3-level VSI based ASVC circuit is shown in Figure F.1. As presented in Chapter 9 the inverter can by represented by switching functions that relate the a.c. quantities to the d.c. quantities. The switching function corresponding to the Red phase voltage with a 3-level SHEM strategy is shown in Figure F.2.

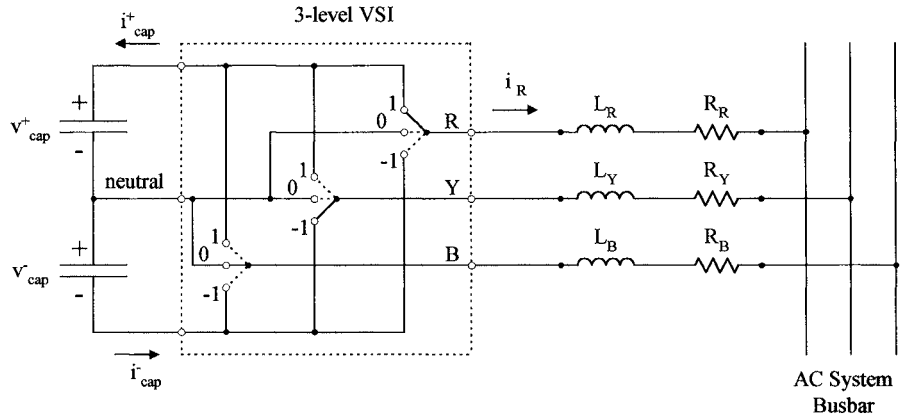


Figure F.1 – Basic 3-level VSI based ASVC circuit, switch representation.

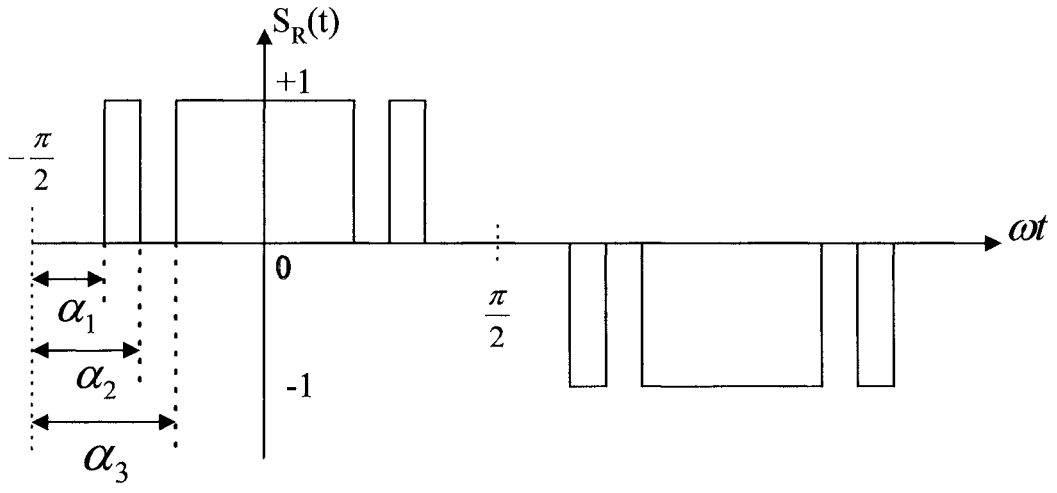
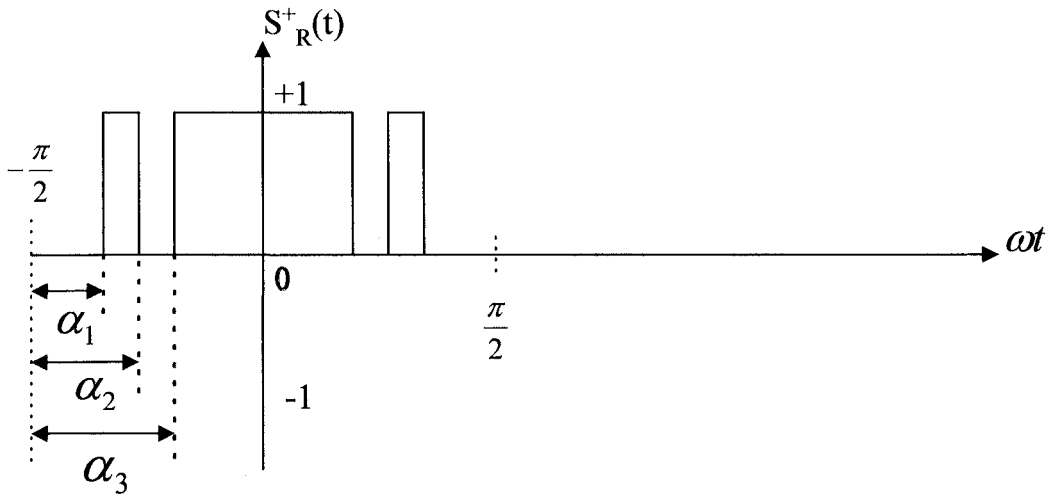
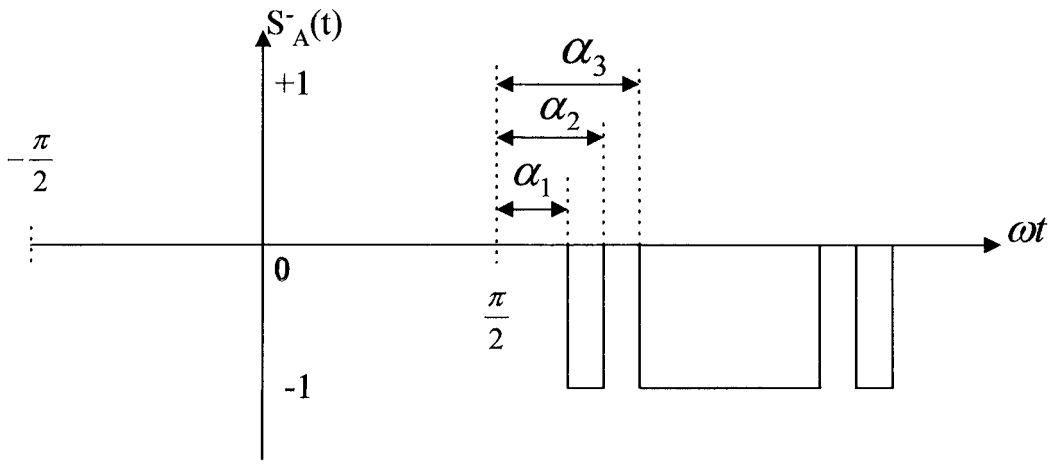


Figure F.2 – SHEM Switching Function for Phase R

If the switching function is further decomposed into positive and negative halves as shown in Figure F.3, analysis can be performed on the effective voltage output of each capacitor (upper and lower) of the 3-level d.c. link. As the functions are periodic, Fourier series techniques can be applied to split them up into the fundamental and harmonic components. The respective Fourier coefficients for the positive half switching function (S^{+}_{R}) and the negative half switching function (S^{-}_{R}) will contain odd and even order harmonic components. This is shown from Fourier analysis below.



(a) - Upper positive half of switching function



(b) – Lower negative half of switching function

Figure F.3 – Decomposition of 3-level SHEM Switching Function

The Fourier series for the positive half switching function can be shown as:

$$S_R^+(t) = \frac{1}{2}a_0 + \sum_{n=1}^{\infty} a_n \cos n(\omega t) + \sum_{n=1}^{\infty} b_n \sin n(\omega t) \tag{F.1}$$

Taking Figure F.3 (a) as the reference waveform, the coefficients a_0, a_n and b_0 can be found as:

$$a_0 = \frac{1}{\pi}\int_{-\pi}^{\pi} S_R^+(t)\, d(\omega t) \tag{F.2}$$

$$a_0 = \frac{1}{\pi}\left\{\int_{-\frac{\pi}{2}+\alpha_1}^{-\frac{\pi}{2}+\alpha_2} 1 \cdot d(\omega t) + \int_{-\frac{\pi}{2}+\alpha_3}^{\frac{\pi}{2}-\alpha_3} 1 \cdot d(\omega t) + \int_{\frac{\pi}{2}-\alpha_2}^{\frac{\pi}{2}-\alpha_1} 1 \cdot d(\omega t)\right\} \tag{F.3}$$

$$a_0 = \frac{1}{\pi}\left\{\left[\omega t\right]_{-\frac{\pi}{2}+\alpha_1}^{-\frac{\pi}{2}+\alpha_2} + \left[\omega t\right]_{-\frac{\pi}{2}+\alpha_3}^{\frac{\pi}{2}-\alpha_3} + \left[\omega t\right]_{\frac{\pi}{2}-\alpha_2}^{\frac{\pi}{2}-\alpha_1}\right\} \tag{F.4}$$

$$a_0 = \frac{1}{\pi}\left\{-2\alpha_1 + 2\alpha_2 - 2\alpha_3\right\} \tag{F.5}$$

$$a_0 = 1 - \frac{2\alpha_1}{\pi} + \frac{2\alpha_2}{\pi} - \frac{2\alpha_3}{\pi} \tag{F.6}$$

$$a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} S_R^+(t)\cos n(\omega t)\, d(\omega t) \tag{F.7}$$

$$a_n = \frac{1}{\pi}\left\{\int_{-\frac{\pi}{2}+\alpha_1}^{-\frac{\pi}{2}+\alpha_2} \cos n(\omega t)\, d(\omega t) + \int_{-\frac{\pi}{2}+\alpha_3}^{\frac{\pi}{2}-\alpha_2} \cos n(\omega t)\, d(\omega t) + \int_{\frac{\pi}{2}-\alpha_2}^{\frac{\pi}{2}-\alpha_1} \cos n(\omega t)\, d(\omega t)\right\} \tag{F.8}$$

$$a_n = \frac{1}{\pi}\left\{\left[\frac{\sin n(\omega t)}{n}\right]_{\left(-\frac{\pi}{2}+\alpha_1\right)}^{\left(-\frac{\pi}{2}+\alpha_2\right)} + \left[\frac{\sin n(\omega t)}{n}\right]_{\left(-\frac{\pi}{2}+\alpha_3\right)}^{\left(\frac{\pi}{2}-\alpha_3\right)} + \left[\frac{\sin n(\omega t)}{n}\right]_{\left(\frac{\pi}{2}-\alpha_2\right)}^{\left(\frac{\pi}{2}-\alpha_1\right)}\right\} \quad \text{(F.9)}$$

$$a_n = \frac{1}{\pi \cdot n}\left\{\left[\sin n\left(\frac{\pi}{2}-\alpha_1\right) - \sin n\left(-\frac{\pi}{2}+\alpha_1\right)\right] - \left[\sin n\left(\frac{\pi}{2}-\alpha_2\right) - \sin n\left(-\frac{\pi}{2}+\alpha_2\right)\right]\right.$$

$$\left. + \left[\sin n\left(\frac{\pi}{2}-\alpha_3\right) - \sin n\left(-\frac{\pi}{2}+\alpha_3\right)\right]\right\} \quad \text{(F.10)}$$

$$a_n = \frac{2}{\pi \cdot n}\left\{\sin n\left(\frac{\pi}{2}-\alpha_1\right) - \sin n\left(\frac{\pi}{2}-\alpha_2\right) + \sin n\left(\frac{\pi}{2}-\alpha_3\right)\right\} \quad \text{(F.11)}$$

Therefore,

$$a_n = \frac{2}{\pi \cdot n}\left[(-1)^{(n-2)/2}\left[\sin n(\alpha_1) - \sin n(\alpha_2) + \sin n(\alpha_3)\right]\right] \qquad \text{for even n} \qquad \text{(F.12)}$$

$$a_n = \frac{2}{\pi \cdot n}\left[(-1)^{(n-1)/2}\left[\cos n(\alpha_1) - \cos n(\alpha_2) + \cos n(\alpha_3)\right]\right] \qquad \text{for odd n} \qquad \text{(F.13)}$$

The remaining coefficient can be found by:

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} S_R^+(t)\sin n(\omega t)d(\omega t) \quad \text{(F.14)}$$

$$b_n = \frac{1}{\pi}\left\{\int_{-\frac{\pi}{2}+\alpha_1}^{-\frac{\pi}{2}+\alpha_2} \sin n(\omega t)d(\omega t) + \int_{-\frac{\pi}{2}+\alpha_3}^{\frac{\pi}{2}-\alpha_2} \sin n(\omega t)d(\omega t) + \int_{\frac{\pi}{2}-\alpha_2}^{\frac{\pi}{2}-\alpha_1} \sin n(\omega t)d(\omega t)\right\} \quad \text{(F.15)}$$

$$b_n = \frac{1}{\pi}\left\{\left[\frac{-\cos n(\omega t)}{n}\right]_{\left(-\frac{\pi}{2}+\alpha_1\right)}^{\left(-\frac{\pi}{2}+\alpha_2\right)} + \left[\frac{-\cos n(\omega t)}{n}\right]_{\left(-\frac{\pi}{2}+\alpha_3\right)}^{\left(\frac{\pi}{2}-\alpha_3\right)} + \left[\frac{-\cos n(\omega t)}{n}\right]_{\left(\frac{\pi}{2}-\alpha_2\right)}^{\left(\frac{\pi}{2}-\alpha_1\right)}\right\} \quad \text{(F.16)}$$

$$b_n = \frac{1}{\pi \cdot n}\left\{\left[-\cos n\left(\frac{\pi}{2}-\alpha_1\right)+\cos n\left(-\frac{\pi}{2}+\alpha_1\right)\right]+\left[\cos n\left(\frac{\pi}{2}-\alpha_2\right)-\cos n\left(-\frac{\pi}{2}+\alpha_2\right)\right]\right.$$

$$\left.+\left[-\cos n\left(\frac{\pi}{2}-\alpha_3\right)+\cos n\left(-\frac{\pi}{2}+\alpha_3\right)\right]\right\} \qquad \text{(F.17)}$$

$$b_n = \frac{2}{\pi \cdot n}\left\{-\cos n\left(\frac{\pi}{2}-\alpha_1\right)+\cos n\left(\frac{\pi}{2}-\alpha_2\right)-\cos n\left(\frac{\pi}{2}-\alpha_3\right)\right\} \qquad \text{(F.18)}$$

Therefore,

$$b_n = \frac{2}{\pi \cdot n}\left[(-1)^{(n-1)/2}\left[\cos n(\alpha_1)-\cos n(\alpha_2)+\cos n(\alpha_3)\right]\right] \qquad \text{for odd n} \qquad \text{(F.19)}$$

$$b_n = \frac{2}{\pi \cdot n}\left[(-1)^{(n-2)/2}\left[\sin n(\alpha_1)-\sin n(\alpha_2)+\sin n(\alpha_3)\right]\right] \qquad \text{for even n} \qquad \text{(F.20)}$$

If functions of α are defined for the derived coefficients as follows:

$$f_1(\alpha) = \frac{1}{2}-\frac{\alpha_1}{\pi}+\frac{\alpha_2}{\pi}-\frac{\alpha_3}{\pi} \qquad \text{(F.21)}$$

$$f_2(\alpha) = \cos n(\alpha_1)-\cos n(\alpha_2)+\cos n(\alpha_3) \qquad \text{for odd n} \qquad \text{(F.22)}$$

$$f_3(\alpha) = \sin n(\alpha_1)-\sin n(\alpha_2)+\sin n(\alpha_3) \qquad \text{for even n} \qquad \text{(F.23)}$$

Then if coefficient equations (F.6), (F.12)-(F.13) and (F.19)-(F.20) are substituted into equation (F.1), using the functions defined above it is possible to show generalised a switching function as below:

$$S_R^+(t) = f_1(\alpha)+\frac{2}{\pi \cdot n}\sum_{n=1}^{\infty}\begin{bmatrix}(-1)^{(n-1)/2} f_2(\alpha)\cos n(\omega t) & for & odd & n\\ (-1)^{(n-2)/2} f_3(\alpha)\cos n(\omega t) & for & even & n\end{bmatrix} \qquad \text{(F.24)}$$

Similarly this can be shown for the negative half switching function and for the remaining yellow and blue phases.

$$S_R^-(t) = f_1(\alpha) + \frac{2}{\pi \cdot n}\sum_{n=1}^{\infty}\begin{bmatrix}(-1)^{(n+1)/2} f_2(\alpha)\cos n(\omega t) & for \quad odd \quad n \\ (-1)^{(n-2)/2} f_3(\alpha)\cos n(\omega t) & for \quad even \quad n\end{bmatrix} \tag{F.25}$$

$$S_Y^+(t) = f_1(\alpha) + \frac{2}{\pi \cdot n}\sum_{n=1}^{\infty}\begin{bmatrix}(-1)^{(n-1)/2} f_2(\alpha)\cos n\left(\omega t - \frac{2\pi}{3}\right) & for \quad odd \quad n \\ (-1)^{(n-2)/2} f_3(\alpha)\cos n\left(\omega t - \frac{2\pi}{3}\right) & for \quad even \quad n\end{bmatrix} \tag{F.26}$$

$$S_Y^-(t) = f_1(\alpha) + \frac{2}{\pi \cdot n}\sum_{n=1}^{\infty}\begin{bmatrix}(-1)^{(n+1)/2} f_2(\alpha)\cos n\left(\omega t - \frac{2\pi}{3}\right) & for \quad odd \quad n \\ (-1)^{(n-2)/2} f_3(\alpha)\cos n\left(\omega t - \frac{2\pi}{3}\right) & for \quad even \quad n\end{bmatrix} \tag{F.27}$$

$$S_B^+(t) = f_1(\alpha) + \frac{2}{\pi \cdot n}\sum_{n=1}^{\infty}\begin{bmatrix}(-1)^{(n-1)/2} f_2(\alpha)\cos n\left(\omega t - \frac{4\pi}{3}\right) & for \quad odd \quad n \\ (-1)^{(n-2)/2} f_3(\alpha)\cos n\left(\omega t - \frac{4\pi}{3}\right) & for \quad even \quad n\end{bmatrix} \tag{F.28}$$

$$S_B^-(t) = f_1(\alpha) + \frac{2}{\pi \cdot n}\sum_{n=1}^{\infty}\begin{bmatrix}(-1)^{(n+1)/2} f_2(\alpha)\cos n\left(\omega t - \frac{4\pi}{3}\right) & for \quad odd \quad n \\ (-1)^{(n-2)/2} f_3(\alpha)\cos n\left(\omega t - \frac{4\pi}{3}\right) & for \quad even \quad n\end{bmatrix} \tag{F.29}$$

From the derived coefficients above, the 2nd and 4th harmonics in the positive half switching function can be shown as:

$$S_2^+ = \frac{2}{2\pi}\left[\sin(2\alpha_1) - \sin(2\alpha_2) + \sin(2\alpha_3)\right] \tag{F.30}$$

$$S_4^+ = \frac{2}{4\pi}\left[\sin(4\alpha_1) - \sin(4\alpha_2) + \sin(4\alpha_3)\right] \tag{F.31}$$

Considering the equation below for the upper capacitor current (i^{+}_{cap}):

$$i^{+}_{cap} = -i_R(t)S^{+}_R(t) - i_Y(t)S^{+}_Y(t) - i_B(t)S^{+}_B(t) \tag{F.32}$$

It can be shown that the upper capacitor current (i^{+}_{cap}) will be dominated with the 2nd and 4th harmonic terms associated with the positive half of the switching function. Using equation (F.32) the 3rd harmonic current corresponding to the 2nd order harmonic can be represented as:

$$i^{+2}_{cap3}(t) = -i_R(t)S^{+}_2\cos(2\omega t) - i_Y(t)S^{+}_2\cos\left(2\omega t - \frac{4\pi}{3}\right) - i_B(t)S^{+}_2\cos\left(2\omega t - \frac{8\pi}{3}\right) \tag{F.33}$$

Where the ASVC phase output currents are:

$$i_R(t) = I_1\cos\left(\omega t - \frac{\pi}{2}\right) \tag{F.34}$$

$$i_Y(t) = I_1\cos\left(\omega t - \frac{\pi}{2} - \frac{2\pi}{3}\right) \tag{F.35}$$

$$i_B(t) = I_1\cos\left(\omega t - \frac{\pi}{2} - \frac{4\pi}{3}\right) \tag{F.36}$$

If these equations are substituted into equation (F.33) and we first consider the 3rd harmonic contribution due to the 2nd harmonic in the Red phase we can show:

$$i^{+2}_{cap3,R} = -I_1S^{+}_2\cos\left(\omega t - \frac{\pi}{2}\right)\cos(2\omega t) \tag{F.37}$$

$$i^{+2}_{cap3,R} = -I_1S^{+}_2\sin(\omega t)\cos(2\omega t) \tag{F.38}$$

$$i^{+2}_{cap3,R} = -\frac{1}{2}I_1S^{+}_2[\sin(3\omega t) - \sin(\omega t)] \tag{F.39}$$

Similarly for the Yellow phase:

$$i_{cap3,Y}^{+2} = -I_1 S_2^{+} \cos\left(\omega t - \frac{\pi}{2} - \frac{2\pi}{3}\right)\cos\left(2\omega t - \frac{4\pi}{3}\right) \tag{F.40}$$

$$i_{cap3,Y}^{+2} = -I_1 S_2^{+} \sin\left(\omega t - \frac{2\pi}{3}\right)\cos\left(2\omega t - \frac{4\pi}{3}\right) \tag{F.41}$$

$$i_{cap3,Y}^{+2} = -\frac{1}{2} I_1 S_2^{+}\left[\sin(3\omega t) - \sin\left(\omega t + \frac{2\pi}{3}\right)\right] \tag{F.42}$$

Finally, considering the Blue phase:

$$i_{cap3,B}^{+2} = -I_1 S_2^{+} \cos\left(\omega t - \frac{\pi}{2} - \frac{4\pi}{3}\right)\cos\left(2\omega t - \frac{8\pi}{3}\right) \tag{F.43}$$

$$i_{cap3,B}^{+2} = -I_1 S_2^{+} \sin\left(\omega t - \frac{4\pi}{3}\right)\cos\left(2\omega t - \frac{8\pi}{3}\right) \tag{F.44}$$

$$i_{cap3,B}^{+2} = -\frac{1}{2} I_1 S_2^{+}\left[\sin(3\omega t) - \sin\left(\omega t + \frac{4\pi}{3}\right)\right] \tag{F.45}$$

Therefore, the total 3rd harmonic contribution, due to the 2nd harmonic content of the phase currents can be shown as:

$$i_{cap3}^{+2} = i_{cap3,R}^{+2} + i_{cap3,Y}^{+2} + i_{cap3,B}^{+2} \tag{F.46}$$

$$i_{cap3}^{+2} = -\frac{3}{2} I_1 S_2^{+}\left[\sin(3\omega t) - \left(\sin(\omega t) + \sin\left(\omega t + \frac{2\pi}{3}\right) + \sin\left(\omega t + \frac{4\pi}{3}\right)\right)\right] \tag{F.47}$$

If the system is balanced then:

$$i_{cap3}^{+2} = -\frac{3}{2} I_1 S_2^+ \sin(3\omega t) \tag{F.48}$$

If the system is unbalanced then the summation will equate to a constant.

Similarly the contribution of the 4th harmonic in the switching function to the 3rd harmonic ripple in the upper capacitor current can be shown as:

$$i_{cap3}^{+4}(t) = -i_R(t) S_4^+ \cos(4\omega t) - i_Y(t) S_4^+ \cos\left(4\omega t - \frac{8\pi}{3}\right) - i_B(t) S_4^+ \cos\left(4\omega t - \frac{16\pi}{3}\right) \tag{F.49}$$

Again substituting equations (F.34), (F.35) and (F.36) into this equation, if we first consider the harmonic contribution if the upper capacitor current due to the 4th harmonic in the Red phase we can show:

$$i_{cap,R}^{+4}(t) = -I_1 S_4^+ \cos\left(\omega t - \frac{\pi}{2}\right)\cos(4\omega t) \tag{F.50}$$

$$i_{cap,R}^{+4}(t) = -I_1 S_4^+ \sin(\omega t)\cos(4\omega t) \tag{F.51}$$

$$i_{cap,R}^{+4}(t) = -\frac{1}{2} I_1 S_4^+ [\sin(5\omega t) - \sin(3\omega t)] \tag{F.52}$$

Similarly for the Yellow and Blue phases:

$$i_{cap,Y}^{+4}(t) = -\frac{1}{2} I_1 S_4^+ \left[\sin\left(5\omega t - \frac{10\pi}{3}\right) - \sin(3\omega t)\right] \tag{F.53}$$

$$i_{cap,B}^{+4}(t) = -\frac{1}{2} I_1 S_4^+ \left[\sin\left(5\omega t - \frac{20\pi}{3}\right) - \sin(3\omega t)\right] \tag{F.54}$$

Therefore, the 3rd harmonic in the upper capacitor current due to the 2nd and 4th harmonic components associated with the positive half switching function can be shown as:

$$i_{cap3}^{+2,4}(t) = -\frac{3}{2} I_1 \left(S_2^+ - S_4^+ \right) \sin(3\omega t) \tag{F.55}$$

This illustrates that the capacitor current mainly contains the 3rd harmonic, which is dependant upon the load level of the 3-level ASVC. Substituting equation (F.55) into equation (F.56), the 3rd harmonic voltage across the capacitor can be shown as in equation (F.57).

$$v_{cap}^+ = \frac{1}{C} \int \left(-i_R(t) S_R^+(t) - i_Y(t) S_Y^+(t) - i_B(t) S_B^+(t) \right) dt \tag{F.56}$$

$$v_{cap3}^{+2,4}(t) = \frac{1}{C} \int i_{cap3}^{+2,4}(t) dt = \frac{1}{2\omega C} I_1 \left(S_2^+ - S_4^+ \right) \cos(3\omega t) \tag{F.57}$$

Similar derivation can be shown for the negative half switching function. Taking into account the 2nd and 4th harmonics in the positive and negative halves of the SHEM switching function the 3rd harmonic in the capacitor voltage can be modulated back to the a.c. side.

The additional 5th harmonic in the a.c. side voltage (phase R) resulting from both the positive and negative halves of the d.c. link is calculated as below:

$$\Delta v_{5th}^{\pm 2}(t) = v_{cap3}^+(t) S_2^+ \cos(2\omega t) + v_{cap3}^-(t) \left[-S_2^+ \cos(2\omega t) \right]$$

$$= 2 \frac{1}{2\omega C} I_1 \left(S_2^+ - S_4^+ \right) \cos(3\omega t) S_2^+ \cos(2\omega t)$$

$$= \frac{I_1}{2\omega C} \left(S_2^+ - S_4^+ \right) S_2^+ \cos(5\omega t) + \frac{I_1}{2\omega C} \left(S_2^+ - S_4^+ \right) S_2^+ \cos(\omega t) \tag{F.58}$$

Equation (F.58) illustrates that due to the 3rd harmonic voltage ripple across the upper and lower capacitors, the 2nd harmonic component in the half switching function modulates a 5th harmonic of magnitude dependant upon the size of the capacitor and the ASVC output current.

The total 5th harmonic component in the a.c. side phase voltage can now be found from equations (F.58) and (F.59) and may be expressed including both the constant component of the capacitor voltage and the 3rd harmonic ripple, shown in equation (F.60).

$$S_5 = \frac{4}{5\pi}\left(\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3)\right) \tag{F.59}$$

$$\frac{V_5}{V_{cap0}} = \frac{4}{5\pi}\left[\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3)\right] + \frac{I_1}{2\omega C V_{cap0}}\left(S_2^+ - S_4^+\right)S_2^+ \tag{F.60}$$

The 5th harmonic voltage in the above equation is scaled according to the average d.c. capacitor voltage, V_{cap0}. The 3rd harmonic voltage of the capacitor will also be modulated by the 4th harmonic in the positive and negative halves of the switching function to give additional 7th harmonic on the a.c. side of the inverter. The 7th harmonic voltage can be similarly derived as:

$$\frac{V_7}{V_{cap0}} = \frac{4}{7\pi}\left[\cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3)\right] + \frac{I_1}{2\omega C V_{cap0}}\left(S_2^+ - S_4^+\right)S_4^+ \tag{F.61}$$