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ORIGINAL RESEARCH

An integral backstepping controller design for compensated distribution networks with rapid earth fault current limiters in bushfire prone areas

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Abstract

This paper presents a nonlinear integral backstepping controller (I-BSC) design scheme for a T-type residual current compensation (RCC) inverter used in compensated distribution networks with rapid earth fault current limiters (REFCLs). The major control task for the proposed scheme is to reduce the fault current to a value suitable for the mitigation of powerline bushfires due to single phase-to-ground faults in compensated distribution networks. The key distinct feature of the proposed I-BSC over the traditional backstepping controller (T-BSC) is that it introduces an integral action for analyzing the dynamic of the tracking error which minimizes its steady-state value and ensures better dynamic performance. In order to prove the global asymptotic stability of the RCC inverter with the proposed integral backstepping controller (I-BSC), the Lyapunov function-based theory is used. Finally, the performance of the I-BSC is analyzed on the MATLAB/Simulink environment and compared with a T-BSC. The performance of both I- and T-BSCs is assessed in terms of transient behaviors of the injected current to the neutral, fault current, and line-to-ground voltage of the faulty phase to ensure the standard operational criteria for self-extinguishing powerline bushfires. Simulation results clearly demonstrate that both controllers fulfill operational standards for REFCL-compensated networks though the I-BSC archives better transient behaviors while comparing with the T-BSC. Results from the processor-in-loop (PIL) validations are also included to further justify the applicability of the newly proposed scheme in the real-time environment.

1 | INTRODUCTION

The mitigation of powerline bushfires caused by electric faults is a challenging task for power distribution system operators where 70% of these faults are single-line-to ground (SLG) faults [1]. Arc suppression devices (ASDs) such as rapid earth fault current limiters (REFCLs) or ground fault neutralizers (GFNs) with an adjustable inductor are used to significantly reduce the fault current due to such SLG faults so that the risk of powerline bushfires is minimized. This adjustable inductor in an ASD is usually adjusted for creating resonance with the zero-sequence capacitance of network available at the distribution substation, that is, compensated distribution networks which in turn assists to self-extinguish the fire. Since the inductor is capable to compensate only reactive component of the current, the value of the fault current may be still large enough to ignite fires. Furthermore, the inductor cannot be adjusted to fully compensate the fault current. The residual current compensation (RCC) inverters are used to inject current at the neutral for fully compensating the uncompensated fault current which cannot be tackled by using only the adjustable inductor (i.e. both active and reactive parts). As the severity of the fault and probability of powerline bushfires depend on the magnitude of the fault current which varies with the fault impedance, the RCC inverter needs to properly inject the current to the neutral to fully nullify this current. Hence, the controller used for injecting the current through the RCC inverter should be designed to cope with such variations in the fault current in order to self-extinguish powerline bushfires.

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1.1 | Literature review

The research in the area of resonant grounded distribution networks can be categorized into two directions: (i) fault detection and (ii) control of ASDs. The literature on both directions has started increasing in recent years. A fault detection scheme based on the mathematical morphology approach is presented in [2] to detect faulty phase, feeder, and tentative fault locations. However, it requires higher sampling frequency (i.e. more than 10 kHz) to achieve desired outcomes, while existing field devices have a low sampling frequency (typically 2 kHz). Some advancements have been made in recent years to overcome this problem. For example, a linear optimization technique is proposed in [3] to determine the faulty line along with a robust approach in [4]. A mode decomposition approach with the adaptive noise is used in [5] for ensuring the robust in determining the fault location. However, the fault detection is still a challenging task as the fault current becomes extremely low in a resonant grounded network. Moreover, all these approaches are developed for balanced distribution network though there has been a very recent approach for the unbalanced distribution network [6]. It is worth to mention that the application of ASDs in distribution networks for the powerline bushfire mitigation requires to balance the network to a certain extent. To do this, the network balancing technique as discussed in [7] is used. Another important factor is the fault current compensation through the ASD. Recently, a topology is adopted in [8] for compensating the faulty phase voltage in resonant grounded networks. However, it does not provide effective compensation and it is essential to have controller-based fault current compensation.

Traditionally, RCC inverters uses proportional integral (PI) controllers to reduce the fault current and a closed-loop control scheme is used in [9] for compensating fault currents due to SLG faults in a compensated transmission network. However, the scheme in [9] ensures only the compensation of the active component appearing the fault current. Similarly, advanced topologies with PI controllers are used in [10] for the arc suppression in transmission networks which ensure better performance as compared to the approach discussed in [9]. However, distribution networks are more prone to powerline bushfires as compared to transmission networks. Recently, several controllers have been designed for RCC inverters to reduce the fault current in compensated power distribution networks and these control structures can be broadly categorized as single- and dual-loop controllers while each of these categories also includes compound structure.

A single-loop controller is utilized in [11] for regulating the zero-sequence voltage through a closed-loop controller to suppress the faulty phase voltage. A single-loop compound control structure is presented in [12] for compensated distribution networks using PI controllers where the compound structure is formed using more than one control strategies. In [12], the faulty feeder is identified for an open-loop system and a closed-loop controller is used to reduce the fault current to zero through the neutral voltage displacement. Another PI controller is proposed in [13] for self-extinguishing the arc current due to the SLG fault where its reference value is determined from active and reactive portions of the fault current to achieve the full compensation. The performance of existing PI controllers for compensated distribution networks is improved in [14] using an advanced modulation scheme which is developed based on a distributed commutation scheme. However, all these PI controllers so far discussed in this paper do not have the ability to properly track the sinusoidal reference and ensure adequate damping. A single-loop compound controller is employed in [15] for the RCC inverter where a proportional resonant (PR) controller is used to provide adequate damping while the PI controller enhances the stability margin. However, the tracking problem associate with the sinusoidal reference still exists and the calculation of gain parameters requires to satisfy some constraints.

Dual-loop controllers overcome the problems of single-loop structures used to control RCC inverters where outer and inner loops are used to control the voltage and current, respectively in a similar way to that of controlling traditional voltage source inverters. In [16], the reference current for the RCC inverter is generated through an outer loop by regulating the neutral voltage and then current is then regulated using an inner loop to track the reference current where both loops use PI controllers. Similarly, the dual-loop controller in [17] employs a lag compensator and a PI controller for outer and inner loops, respectively, while functioning exactly in a similar way as discussed in [16]. A similar dual-loop controller is proposed in [18] by designing the outer loop with the combination of PI and PR controllers along with a proportional (P) controller for the inner loop. Though these dual-loop controllers help to effectively self-extinguish powerline bushfires, most of these (except for PR) controllers are designed without considering the dynamic model of ASDs which cannot ensure the complete elimination of the fault current (i.e. significantly reduced chances of igniting powerline bushfires) and hence, it is essential to use model-based approach to design the controller for the RCC inverter.

Model-based approaches, for example, robust H_∞ [19] and model predictive [20] schemes are used to design controllers for the RCC inverter. However, the controller becomes an extremely higher (seventeenth) order one for a first-order system when the robust H_∞ controller as discussed in [19] is used. This makes the implementation more difficult even after reducing the order to seven. On the other hand, the model predictive controller in [20] is applied on an ASD having a three-phase configuration though a single-phase ASD can easily deal with SLG faults. Furthermore, controllers in [19, 20] are designed using the linear model of the ASD whose performance is limited to some specific operating points for which these controllers are designed and the fault current cannot be fully compensated for which there are high chances of powerline bushfires.

Nonlinear backstepping controllers are designed for single-phase [21, 22] and three-phase [23] ASDs where these controllers ensure the global operation in regards to eliminate the fault current. Both controllers are mainly tested only for low impedance faults though compensated distribution networks in bushfire prone areas experience high impedance faults.

Another nonlinear backstepping controller is proposed in [24] for compensated networks with high impedance faults while eliminating some drawbacks (e.g. complex calculation of the reference current) of existing backstepping controllers. However, there still exists the steady-state tracking error with these controllers which can be enough to start powerline bushfires and there are no guarantees that these controllers will ensure the desired the tracking of the sinusoidal reference. Recently, an integral sliding mode controller (SMC) [25], a nonsingular terminal SMC [26], and a nonsingular fast SMC [21, 23–27] are designed for a RCC inverter to mitigate powerline bushfires in REFCL-compensated distribution networks. The controllers in [27] ensures the faster convergence of the fault current to a level that needs to be maintained to ensure the safe operation in bushfire prone areas. However, the desired performance through using these SMCs relies on several arbitrary gains and appropriate sliding surfaces.

1.2 | Research gaps and motivations

Based on the existing literature, the following gaps are identified:

- Existing approaches most consider the connection of the ASD to the distribution buses. However, the effective fault current compensation can only be achieved if the ASD is connected to the neutral.
- Sliding mode controllers are used to control ASDs that are connected to the neutral of the substation but the application of these controllers requires to calculate several gains.
- Existing backstepping approaches do not guarantee the convergence of the fault current to the desired value if the gains are not properly selected.
- Many existing methods are desired based on the three-phase ASDs which are not cost-effective.

These gaps motivate to design a new controller for the effective compensation of the fault current and mitigation of powerline bushfires. Since 70% of total faults are SLG in nature, this work considers only one ASD with a single-phase inverter and it is only capable to work under the SLG faults to solve the problem in a cost-effective way.

1.3 | Contributions

This paper introduces an integral backstepping controller (I-BSC) for the T-type RCC inverter whose main distinct feature over existing backstepping controllers is the inclusion of an integral action for overcoming the tracking problem as mentioned earlier. The main contributions of this work are outlined below:

- The inclusion of an integral action guarantees the desired tracking performance and the proposer compensation of the fault current will be achieved through this proposed I-BSC.
- The use of a T-type inverter that offers several benefits over traditional H-bridge inverters where the lower voltage stresses for switches and improved efficiency are considered as key features.
- The proposed approach is different from all existing sliding mode schemes in terms of the theory and it does not require to calculate so many gains and at the same time, it overcomes the limitation of existing backstepping approaches as it will ensure the convergence through the integral action.

The performance of the proposed I-BSC is compared with a traditional backstepping (T-BSC) in terms of the self-extinguishing capability of powerline bushfires. The main reason for such a comparison is the fairness and features of these both approaches. This paper includes a thorough design process for the proposed I-BSC along with an overview of the T-BSC where the control laws for controlling the switches in T-type RCC inverter is obtained by satisfying a condition that the tracking error will converge to zero. Finally, simulation results are carried out on a compensated distribution networks with variations in fault resistances and these results are benchmarked against standard operational criteria for such networks in bushfire prone areas as indicated in [28]. Simulation results clearly demonstrate the effectiveness of the I-BSC over the T-BSC for self-extinguishing powerline bushfires. The proposed scheme is also validated in the processor-in-loop (PIL) where the performance is compared with I-BSC and nonsingular terminal SMC (NT-SMC) in [26].

1.4 | Organization

The remainder of the paper is organized as follows: Section 2 provides the detailed modeling of the ASD, while the controller design is presented in Section 3. Section 4 shows the simulation results and the PIL validations are presented in Section 5. Finally, concluding remarks are future research directions are provided in Section 6.

2 | MODELING OF ASD WITH RCC INVERTERS

Figure 1 shows a balanced power distribution network which is considered that supplies power to a three-phase load. Each phase in this distribution network includes a zero-sequence impedance network where a zero-sequence resistor and capacitor are connected in parallel. As the network is considered as a balanced one, the values of these zero-sequence resistors for all phases (i.e. R_{0A}, R_{0B}, and R_{0C} for Phases A, B, and C, respectively) will be the same (i.e. R_0) which mean that $R_{0A} = R_{0B} = R_{0C} = R_0$. Similarly, the values of these zero-sequence capacitors for all phases are considered as same, that is, $C_{0A} = C_{0B} = C_{0C} = C_0$ where C_{0A}, C_{0B}, and C_{0C} represent the capacitance for Phases A, B, and C, respectively. The model of the RCC inverter is developed with an SLG fault on Phase A as shown in Figure 1 though the fault can occur on any phases. However,

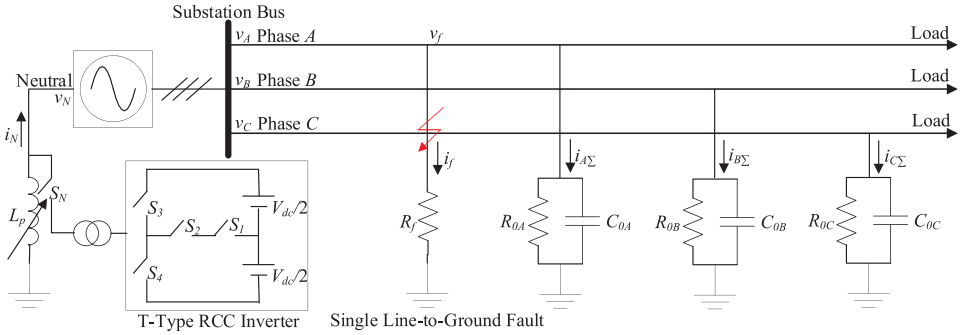

FIGURE 1 A T-type RCC inverter in a REFCL-compensated distribution substation in bushfire prone areas

this will not change the main theme of the modeling and this will be clarified later in this section. An adjustable inductor (L_p) representing the ASD which connects the neutral of the substation with the ground. This inductor has the self-adjusting capability to make resonance with the zero-sequence capacitance looking from the substation. Figure 1 shows that the inverter is connected to the neutral point through a switch (S_N) and a step up transformer where S_N is turned on when there is an SLG fault on the system. The T-type RCC inverter in Figure 1 uses the splitted input DC voltage which indicates the reduction in the voltage stress for switches. The voltage across each phase to ground is basically the sum of the voltages between the phase-to-neutral and neutral-to-ground. For all these phases, these can be written as:

$$\begin{aligned} v_A &= e_A + v_N \\ v_B &= e_B + v_N, \\ v_C &= e_C + v_N \end{aligned} \tag{1}$$

where v_A, v_B, and v_C are phase-to-ground voltages for Phases A, B, and C, respectively; e_A, e_B, and e_C are phase-to-neutral voltages for Phases A, B, and C, respectively; and v_N is the neutral-to-ground voltage. For a balanced network, $e_A + e_B + e_C = 0$ which yields the value of v_N can be written as:

$$v_N = \frac{v_A + v_B + v_C}{3}. \tag{2}$$

Similarly, the current flowing through the impendence network in each phase can be written as the sum of the currents through resistor (i_{R_0}) and capacitor (i_{C_0}). The current flowing through each phase of the impedance network can be expressed as:

$$\begin{aligned} i_{A\Sigma} &= i_{R_{0A}} + i_{C_{0A}} = \frac{v_A}{R_0} + C_0 \frac{dv_A}{dt} \\ i_{B\Sigma} &= i_{R_{0B}} + i_{C_{0B}} = \frac{v_B}{R_0} + C_0 \frac{dv_B}{dt} \\ i_{C\Sigma} &= i_{R_{0C}} + i_{C_{0C}} = \frac{v_C}{R_0} + C_0 \frac{dv_C}{dt} \end{aligned}. \tag{3}$$

Since the fault is applied on Phase A, the fault current (i_f) will be:

$$i_f = \frac{v_f}{R_f} = \frac{v_A}{R_f}, \tag{4}$$

where v_f is the faulty phase voltage which actually represents the line-to-ground voltage for Phase A (i.e. $v_f = v_A$) and R_f is the fault resistance. The neutral current (i_N) can be written as the sum of currents following through each phase of the impedance network and the fault current as indicated below:

$$i_N = i_f + i_{A\Sigma} + i_{B\Sigma} + i_{C\Sigma}. \tag{5}$$

Substituting the values of $i_{A\Sigma}$, $i_{B\Sigma}$, and $i_{C\Sigma}$ from Equation (3) and i_f from Equation (4) into Equation (5), it can be written as:

$$i_N = \frac{v_A}{R_f} + \frac{v_A + v_B + v_C}{R_0} + C_0 \frac{d}{dt}(v_A + v_B + v_C). \tag{6}$$

Using Equation (1), the simplified form of Equation (6) can be written as:

$$i_N = \frac{v_A}{R_f} + \frac{3v_N}{R_0} + 3C_0 \frac{dv_N}{dt}. \tag{7}$$

Since $v_N = e_A + v_A$, that is, $v_A = v_N - e_A$; Equation (7) can be rewritten as:

$$i_N = \left(\frac{3}{R_0} + \frac{1}{R_f}\right) v_A + 3C_0 \frac{dv_A}{dt} - \left(\frac{3}{R_0} e_A + 3C_0 \frac{de_A}{dt}\right). \tag{8}$$

Here, the neutral-to-ground voltage is replaced in terms of the phase-to-neutral and phase-to-ground (or simply phase) voltages of Phase A. However, this phase voltage can also be represented in terms of other phases, that is, Phases A and B which can also be seen from Equation (1). The main reason of replacing the neutral-to-ground voltage in terms of other voltages for Phase A is that the fault is considered on this phase. Hence, the neutral-to-ground voltage can be replaced with other voltages as expressed in Equation (1) depending on which phase the SLG fault occurs.

By considering the RCC inverter, the voltage between the neutral and ground can be expressed as the difference between the output voltage (v_{RCC}) of the RCC inverter and voltage across (v_{L_p}) the adjustable inductor which can be expressed as:

$$v_N = v_{RCC} - v_{L_p}, \tag{9}$$

where $v_{RCC} = mV_{dc}$ with m as the modulation or switching signal for the inverter and V_{dc} as the input DC voltage and $v_{L_p} = L_p \frac{di_N}{dt}$. Hence, Equation (9) can be simplified as:

$$\frac{di_N}{dt} = \frac{mV_{dc} - v_N}{L_p}. \tag{10}$$

In this paper, the main target is to ensure the desired tracking of i_N by regulating m for which the reference value of i_N needs to be determined. This tracking needs to be performed in such a way that i_f in Equation (8) becomes zero which is mandatory for self-extinguishing powerline bushfires. This will be possible if and only if the reference value of i_N, that is, i_{N-ref} is selected as follows [21]:

$$i_{N-ref} = -\left(\frac{3}{R_0} e_A + 3C_0 \frac{de_A}{dt}\right). \tag{11}$$

The proposed integral backstepping controller is designed based on the model in Equation (10) for tracking the reference in Equation (11) which is discussed in the following section.

3 | PROPOSED I-BSC DESIGN AND AN OVERVIEW OF T-BSC FOR RCC INVERTERS

This section presents the detailed design process for the I-BSC while providing an overview of the T-BSC as the performance will be compared with each other, as indicated earlier on this paper. Both controllers will be designed to track i_{N-ref} as indicated in Equation (11). The fundamental difference in designing these controllers is the inclusion of an integral action with the I-BSC. The systematic controller design process for the I-BSC is presented in the subsection below.

3.1 | Design of an I-BSC

If $e_i = i_N - i_{N-ref}$ is used to define the tracking error of i_N, its dynamic can be written as:

$$\dot{e}_i = \frac{mV_{dc} - v_N}{L_p} - \frac{di_{N-ref}}{dt}. \tag{12}$$

For ensuring the fast convergence of the neutral current to its reference value and maintain the zero tracking error, the following integral action (ξ) can be introduced as:

$$\xi = \int_0^t (i_N - i_{N-ref})dt = \int_0^t e_i dt, \tag{13}$$

and dynamic of this integral action represents the error which can be written as follows:

$$\dot{\xi} = e_i. \tag{14}$$

At this instant, the dynamics of both error and integral action of the error need to be analyzed in order to ensure the desired tracking performance, that is, the convergence of the error to zero. For this purpose, it is essential to formulate an energy function or control Lyapunov function (CLF) by considering the effects of both error and integration action of this error. The CLF (W_i) for this can be defined as follows:

$$W_i = \frac{1}{2}\left(e_i^2 + \rho_i \xi^2\right), \tag{15}$$

where ρ_i is a positive constant that is used for controlling the convergence speed of the error with the integral action. Now, the desired tracking can be guaranteed if m is obtained in such a way that $\dot{W}_i < 0$ (i.e. negative-definite) or $\dot{W}_i \leq 0$ (i.e. negative semi-definite). Taking the derivative of $\dot{W}_i$ in Equation (15) and substituting the values of $\dot{e}_i$ and $\dot{\xi}$ from Equations (13) and (14), respectively; it can be written as:

$$\dot{W}_i = e_i\left(\frac{mV_{dc} - v_N}{L_p} - \frac{di_{N-ref}}{dt} + \rho_i \xi\right). \tag{16}$$

The value of $\dot{W}_i$ will be negative semi-definite (i.e. $\dot{W}_i = -k_i e_i^2$) for any value of e_i with k_i is a positive gain parameter. This gain parameter ensures the convergence speed of the error by satisfying the following condition:

$$\frac{mV_{dc} - v_N}{L_p} - \frac{di_{N-ref}}{dt} + \rho_i \xi = -k_i e_i. \tag{17}$$

The switching control input for the RCC inventer can be obtained from Equation (17) as:

$$m_{I-BSC} = \frac{V_{dc}}{L_p}\left(\frac{v_N}{L_p} + \frac{di_{N-ref}}{dt} - \rho_i \xi - k_i e_i\right). \tag{18}$$

Here, m_{I-BSC} is used instead of m to make it different from the T-BSC. This I-BSC is used to control the RCC inverter for completely eliminating the fault current. The control signal in Equation (18) will simplify Equation (16) as follows:

$$\dot{W}_i = -\frac{1}{2} e_i^2, \tag{19}$$

which clearly depicts the negative definiteness (for any values of e_i other than 0) or negative semi-definiteness (for any values of

e_i including 0). Hence, the inclusion of the integral action does not affect the overall stability of the system. This will be further clarified through simulation results later in this paper.

3.2 | An overview of the T-BSC

For the T-BSC, the tracking error is defined as e_T which is exactly similar to that of the error in the previous subsection, that is, $e_T = i_N - i_{N-ref}$. With this tracking error, the CLF (W_T) for the T-BSC (i.e. without considering the integral action) can be written as:

$$W_T = \frac{1}{2}e_T^2. \tag{20}$$

For analyzing the convergence of the error, $\dot{W}_T$ needs to satisfy similar conditions for which it can be written as:

$$\dot{W}_T = e_T\left(\frac{mV_{dc} - v_N}{L_p} - \frac{di_{N-ref}}{dt}\right). \tag{21}$$

The value of $\dot{W}_T$ will be negative semi-definite (i.e. $W_T = -k_T e_T^2$) for any value of e_T if k_T is a positive gain parameter. This gain parameter ensures the convergence speed of the error by satisfying the following condition:

$$\frac{mV_{dc} - v_N}{L_p} - \frac{di_{N-ref}}{dt} = -k_T e_T. \tag{22}$$

The switching control input for the RCC inventer can be obtained from Equation (22) and written as follows:

$$m_{T-BSC} = \frac{V_{dc}}{L_p}\left(\frac{v_N}{L_p} + \frac{di_{N-ref}}{dt} - k_T e_T\right). \tag{23}$$

Here, m_{T-BSC} is used instead of m to make it different from the I-BSC. This T-BSC is compared with an I-BSC and the fundamental difference between these controllers can easily be seen from Equations (18) and (23). Simulation results are carried out in the following section to justify the superiority of the I-BSC over the T-BSC.

4 | SIMULATION RESULTS

The designed I-BSC is simulated for an RCC inverter used in a compensated distribution network as shown in Figure 1 and its performances are compared with a T-BSC under different operating conditions where variations in operating conditions are reflected through changes in fault resistances which in turn change the fault current. Different scenarios are analyzed in terms of achieving the desired fault current compensation, that is, the convergence speed. The adjustable inductor (L_p) is selected as 0.9 H for creating resonance at the substation. Here, the zero-sequence capacitance (C_0) for each phase-to-ground is considered as 4 μF whereas the zero-sequence resistance is 28 kΩ. The rated (line-to-line) voltage for the distribution network is considered as 22 kV (rms) which corresponds the rms value as 12.7 kV for the phase voltage. The T-type inverter has a total input DC voltage (V_{dc}) as 800 V. The internal source resistance is considered as negligible and hence, the rms value of e_A will be similar to that of the phase voltage, that is, 12.7 kV. Equation (18) is used to obtain the control input for the RCC inverter using the I-BSC is formulated based on Equation (18) and its performance is compared with the T-BSC which is quite similar to the backstepping approach as presented in [21]. The control input is converted into switching pulses using the pulse width modulation technique for which the switching frequency is 10 kHz. The control parameters for the I-BSC are selected as: $k_i = 20,000$ and $\rho_i = 500$ while for the T-BSC as: $k_T = 20,000$.

The performances of both controllers are assessed based on the operational criteria used for the mitigation of powerline bushfires as discussed in [28] where these are set following two different conditions of the fault impedance. The first condition is for the low impedance fault having the maximum value of the fault impedance as 1 kΩ for which the faulty phase voltage needs to be observed at three different times (which are at 85 ms, 0.5 s, and 2 s) after activating the RCC inverter with the I-BSC. On the other, this voltage needs to be observed only at 2 s for high impedance faults (i.e. for $R_f > 1$ kΩ). The chances of powerline bushfires will be reduced if the faulty phase voltage is kept at 250 V within 2 s of initiating the RCC inverter for both high and low impedance faults [28]. However, the faulty phase voltages for low impedance faults need to be kept at or below 1900 V at 85 ms and 750 V at 0.5 s of activating the RCC inverter [28]. The fault current needs to be maintained at or below 0.5 A within 2 s after initiating the RCC inverter irrespective of the fault impedance. It should be noted that the RCC inverter generally starts its operation at the instant of detecting faults and the maximum value of R_f is 25.4 kΩ for compensated distribution networks rated at 12.7 kV (rms) as the phase voltage which corresponds the value of the fault current as 0.5 A, up to which the REFCL can detect the fault. However, the simulation studies are carried out in such a manner that the RCC inverter is activated after a specific time delay which is just to demonstrate that the fault current cannot fully be eliminated through the adjustable inductor though its value reduces. The simulation studies are carried out by considering three different fault resistances such as 50 Ω, 10 kΩ, and 26 kΩ to ensure the suitability of the I-BSC with variations in fault impedances. The following operational sequence is considered during the simulation for all three fault resistances:

- Fault occurs on Phase A at t=0.2 s and
- The RCC inverter starts its operation at t=0.4 s.

4.1 | Scenario 1: PIL validation for $R_f = 10\ \Omega$

The simulations are first carried out for an SLG fault with R_f=50 Ω. The distribution system operates under normal

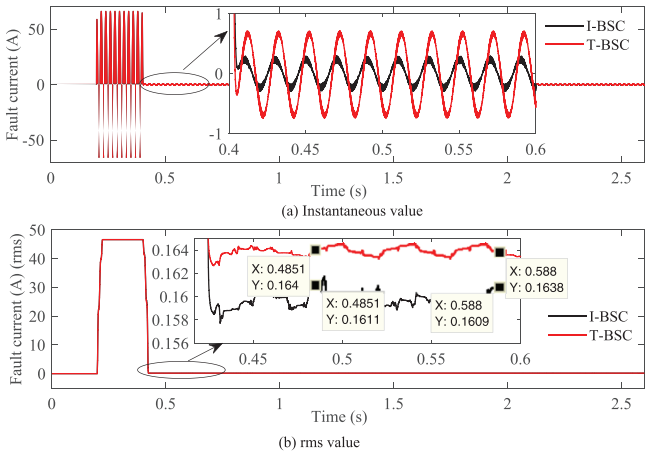

FIGURE 2 Fault current (instantaneous and rms) when the SLG fault occurs on Phase A with R_f=50 Ω

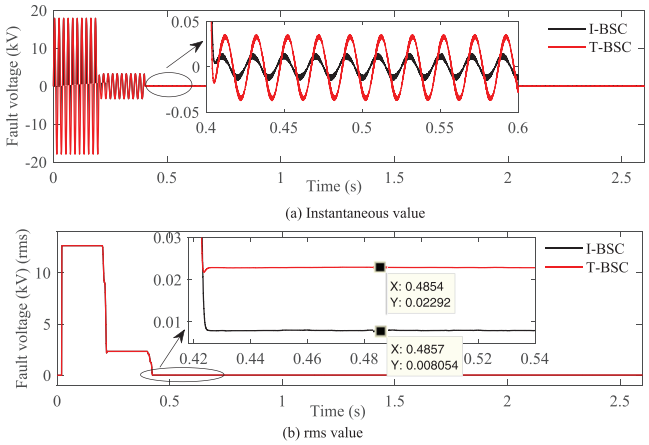

FIGURE 3 Faulty phase voltage (instantaneous and rms) when the SLG fault occurs on Phase A with R_f=50 Ω

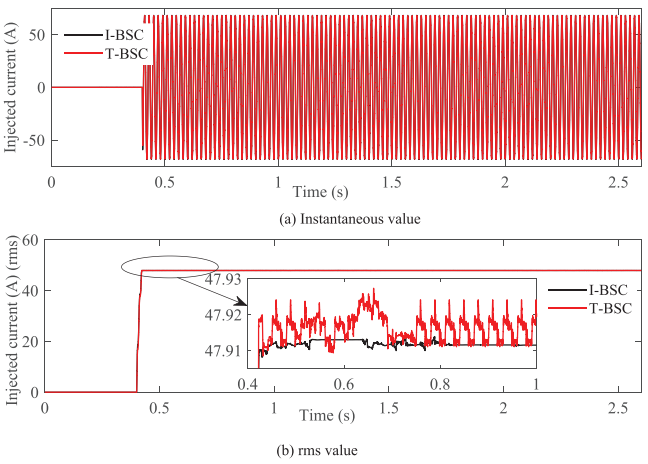

FIGURE 4 Injected current (instantaneous and rms) by the RCC inverter when the SLG fault occurs on Phase A with R_f=50 Ω

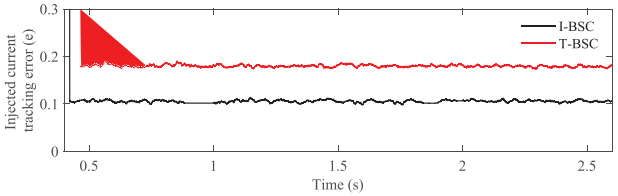

FIGURE 5 Tracking error of the injected current by the RCC inverter when the SLG fault occurs on Phase A with R_f=50 Ω

conditions, that is, there will be no fault current until the fault is applied, that is, up to t=0.2 s. After applying the SLG fault on Phase A, the self-adjusting coil will be in operation and try to make resonance before activating the RCC inverter as the RCC inverter is activated at t=0.4 s rather that at t=0.2 s. Hence, there will be fault current from t=0.2 s and t=0.4 s. The fault current will be reduced when the RCC inverter is activated, that is, at t=0.4 s. All these can be seen from Figure 2 representing the fault current in both instantaneous and rms forms. Figure 2 clearly demonstrates that both controllers (i.e. I-BSC and T-BSC) ensures the value of the fault current below 0.5 A within a timeframe much lower than 2 s after starting the operation of the RCC inverter. The faulty phase voltage will be reduced when an SLG fault occurs on a particular phase. This is due to the short-circuit with the ground through a fault resistance of 50 Ω which can also be seen from Figure 3 where this voltage reduces to around 2 kV. However, the activation of the RCC inverter will further reduce the faulty phase voltage which needs to be maintained as per the standard discussed in [28]. Figure 3 shows that the faulty phase voltage reduces to around 8 V within 85 ms after initiating the operation of the RCC inverter when the designed I-BSC is used while this value is around 22 V with the T-BSC. The faulty phase voltage is much lower with both I- and T-BSCs while comparing the requirement as per the standard in [28] as it needs to be maintained at 1900 V within 85 ms as per this standard. Though both controllers ensure the desired performance, the I-BSC acts in a much better way as compared to the T-BSC due to the inclusion of the integral action. The fault current as well as the faulty phase voltage is being compensated due to the current injection by the RCC inverter as shown in Figure 4 which depicts that the current injection starts at t=0.4 s, that is, at the instant of activating the RCC inverter. Figure 4 also indicates that the RCC inverter with the I-BSC injects more stable current as compared to the T-BSC. The improvement in the tracking performance of the neutral current using the I-BSC over the T-BSC can be observed from the tracking error as shown in Figure 5 which clearly depicts that the designed I-BSC exhibits less tracking error as it uses an integral action. Hence, the I-BSC suppresses the fault current in an effective way as compared to the T-BSC which further enhances the chances of self-extinguishing powerline bushfires due to SLG faults.

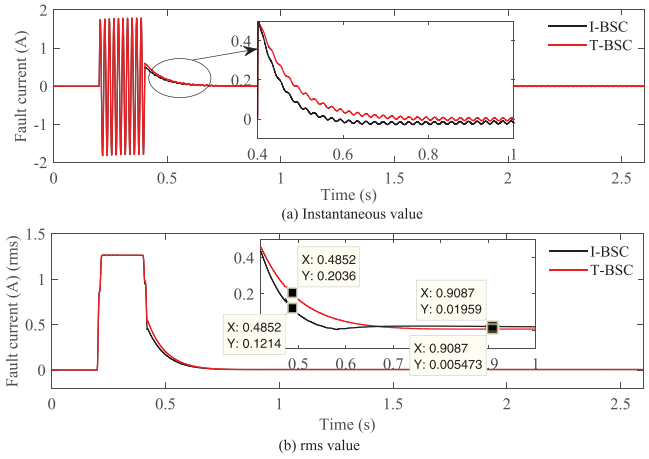

FIGURE 6 Fault current (instantaneous and rms) when the SLG fault occurs on Phase A with R_f=10 kΩ

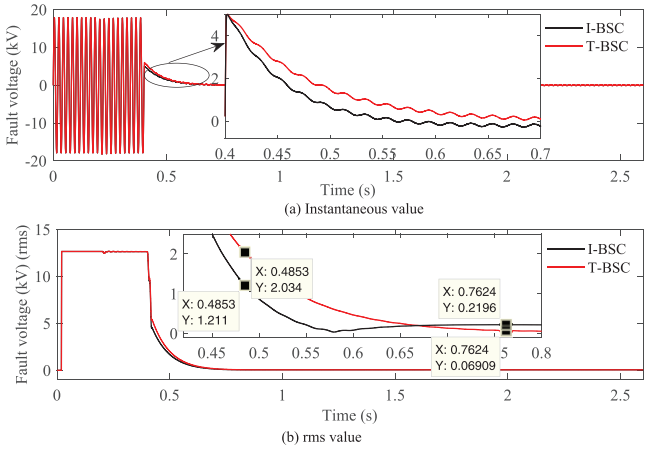

FIGURE 7 Faulty phase voltage (instantaneous and rms) when the SLG fault occurs on Phase A with R_f=10 kΩ

4.2 | Scenario 2: PIL validation for R_f = 10 kΩ

The REFCL-compensated distribution network is then simulated by considering another SLG fault on them same phase, that is, on Phase A but for a different value of R_f where is it is considered as 10 kΩ. Here, a similar operational sequence as indicated earlier on this section is used to demonstrate the performance of the I-BSC over the T-BSC. Since this is a high impedance fault, the fault current will be significantly lower than that of the low impedance fault which can also be clearly observed from Figure 6. From this figure, it can be seen that the value of the fault current from t=0.2 s to t=0.4 s is much lower than that for the low impedance fault as indicated in Figure 2. The fault current is eliminated by activating the RCC inverter as its value is kept below 0.5 A before 2 s. However, the designed I-BSC maintains a much lower value as compared to the T-BSC. The faulty phase voltage at this instant is shown in Figure 7 which clearly shows that the designed I-BSC ensures

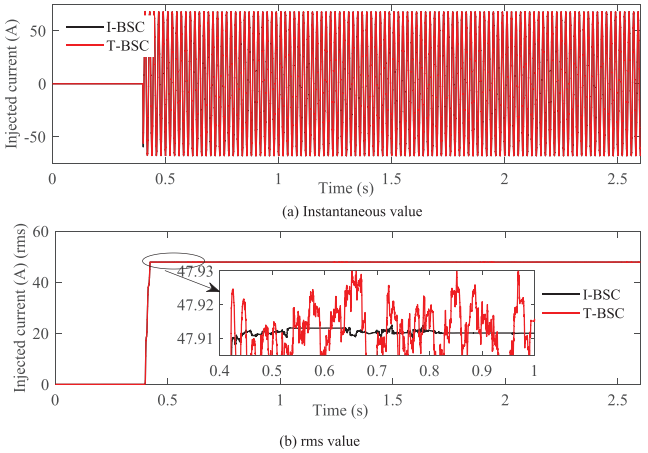

FIGURE 8 Injected current (instantaneous and rms) by the RCC inverter when the SLG fault occurs on Phase A with R_f=10 kΩ

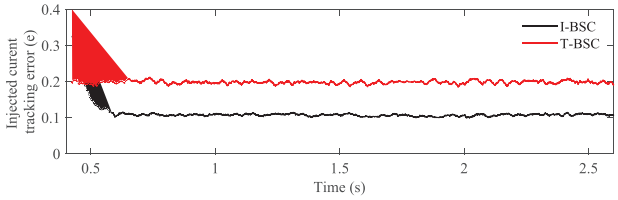

FIGURE 9 Tracking error of the injected current by the RCC inverter when the SLG fault occurs on Phase A with R_f=10 kΩ

the desired operational standard in a faster way than the T-BSC though this standard is ensured by both controllers. The corresponding current injection is shown in Figure 8 which also exhibits less fluctuations as compared to the T-BSC. The tracking errors for the injected current is shown in Figure 9 for both controllers which clearly demonstrate that the RCC inverter with the designed I-BSC injects the current more closer to the reference of the neutral current while comparing with the T-BSC. Therefore, the I-BSC enhances the possibility of self-extinguishing powerline bushfires in a better way.

4.3 | Scenario 3: PIL validation for R_f = 26 kΩ

At this stage, the worst value of the fault impendence for a 22 kV (three-phase) distribution network, that is, the value (R_f = 26 kΩ) for which the fault will be equal to or lower than 0.5 A as the ASD can only detect fault having the fault resistance around this value. Under such a fault condition, the fault current will be significantly lower than two previous fault conditions which can also be evidenced from Figure 10. From Figure 10, it can be observed that the RCC inverter eliminates the fault current and finally, it reduces to almost zero by both I- and T-BSC though the designed I-BSC responds quicker than the T-BSC. At this instant, the faulty phase voltage is shown in Fig 11 which also demonstrates that it reduces to the value aligning with the operational standard as indicated in [28]. The current injected by

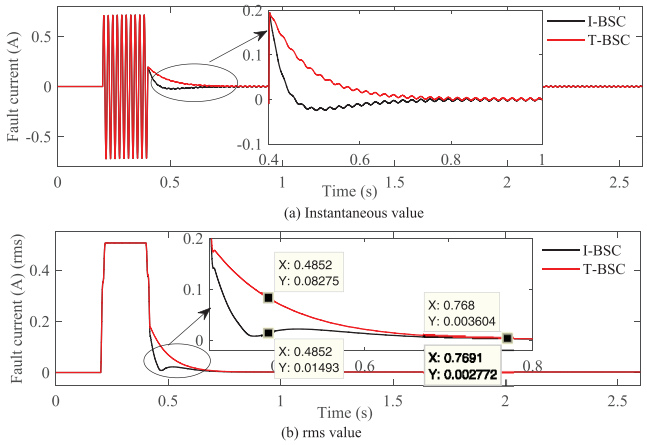

FIGURE 10 Fault current (instantaneous and rms) when the SLG fault occurs on Phase A with R_f=26 kΩ

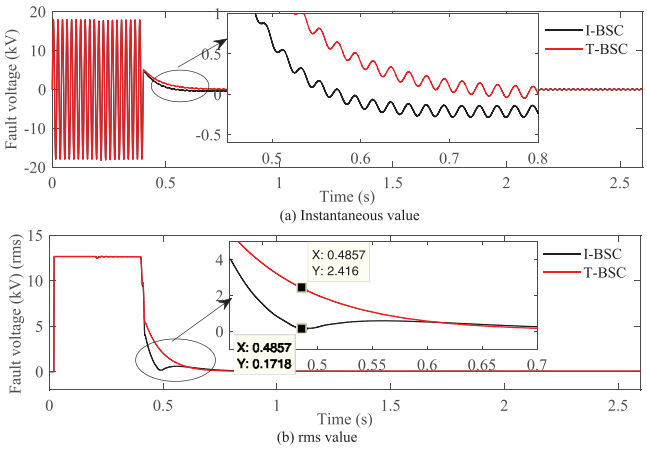

FIGURE 11 Faulty phase voltage (instantaneous and rms) when the SLG fault occurs on Phase A with R_f=26 kΩ

TABLE 1 The rms values of the faulty phase voltage (V) for R_f=50 Ω at different instants

RCC activation time (s)	Simulation time (s)	Voltage (V) with I-BSC	Voltage (V) with T-BSC
0.085	0.485	8.05	22.92
0.5	0.9	8.04	22.88
2	2.4	8.01	22.88

the RCC inverter and the tracking errors for this current with both I- and T-BSCs are shown in Figures 12 and 13, respectively, which clearly demonstrate similar properties to that of other fault conditions where the I-BSC performs better than the T-BSC as it uses an integral action. Hence, it clearly shows the benefit of using an integral action.

The quantitative results highlighting the values of the faulty phase voltage at different time instants are shown in Tables 1, 2, and 3 for the fault impedance of 50 Ω, 10 kΩ, and 26 kΩ, respectively. From Table 1, it can be seen that the faulty phase at

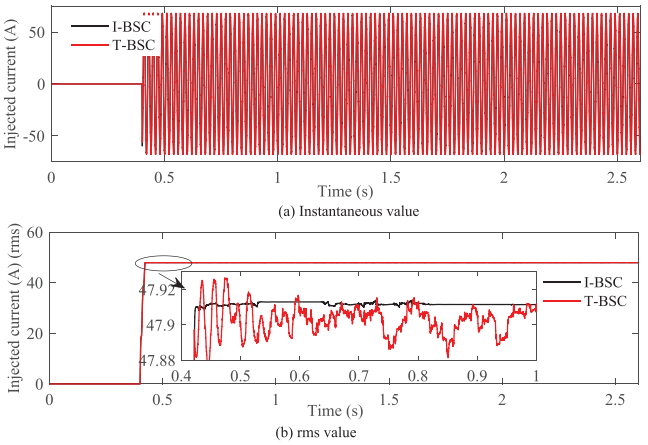

FIGURE 12 Injected current (instantaneous and rms) by the RCC inverter when the SLG fault occurs on Phase A with R_f=26 kΩ

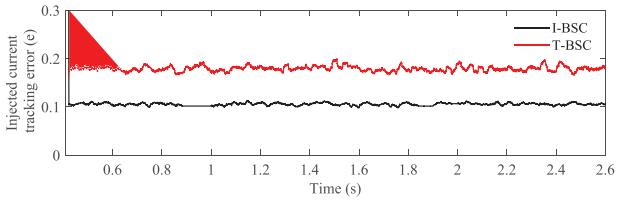

FIGURE 13 Tracking error of the injected current by the RCC inverter when the SLG fault occurs on Phase A with R_f=26 kΩ

TABLE 2 The rms values of the faulty phase voltage (V) for R_f=10 kΩ at different instants

RCC activation time (s)	Simulation time (s)	Voltage (V) with I-BSC	Voltage (V) with T-BSC
0.085	0.485	121.10	203.40
0.5	0.9	54.58	196.50
2	2.4	53.64	57.88

different instatements of simulation is lower with the designed I-BSC when compared with the T-BSC though this value is much lower for both controllers. However, the effectiveness can be clearly distinguished from Tables 2 and 3 from where it can be found that the faulty phase voltage is over 200 V within 85 ms of activating the RCC, while it is much lower for the I-BSC. Hence, it is very clear that the designed controller outperforms

TABLE 3 The rms values of the faulty phase voltage (V) for R_f=26 kΩ at different instants

RCC activation time (s)	Simulation time (s)	Voltage (V) with I-BSC	Voltage (V) with T-BSC
0.085	0.485	171.80	241.60
0.5	0.9	53.80	60.63
2	2.4	50.14	53.88

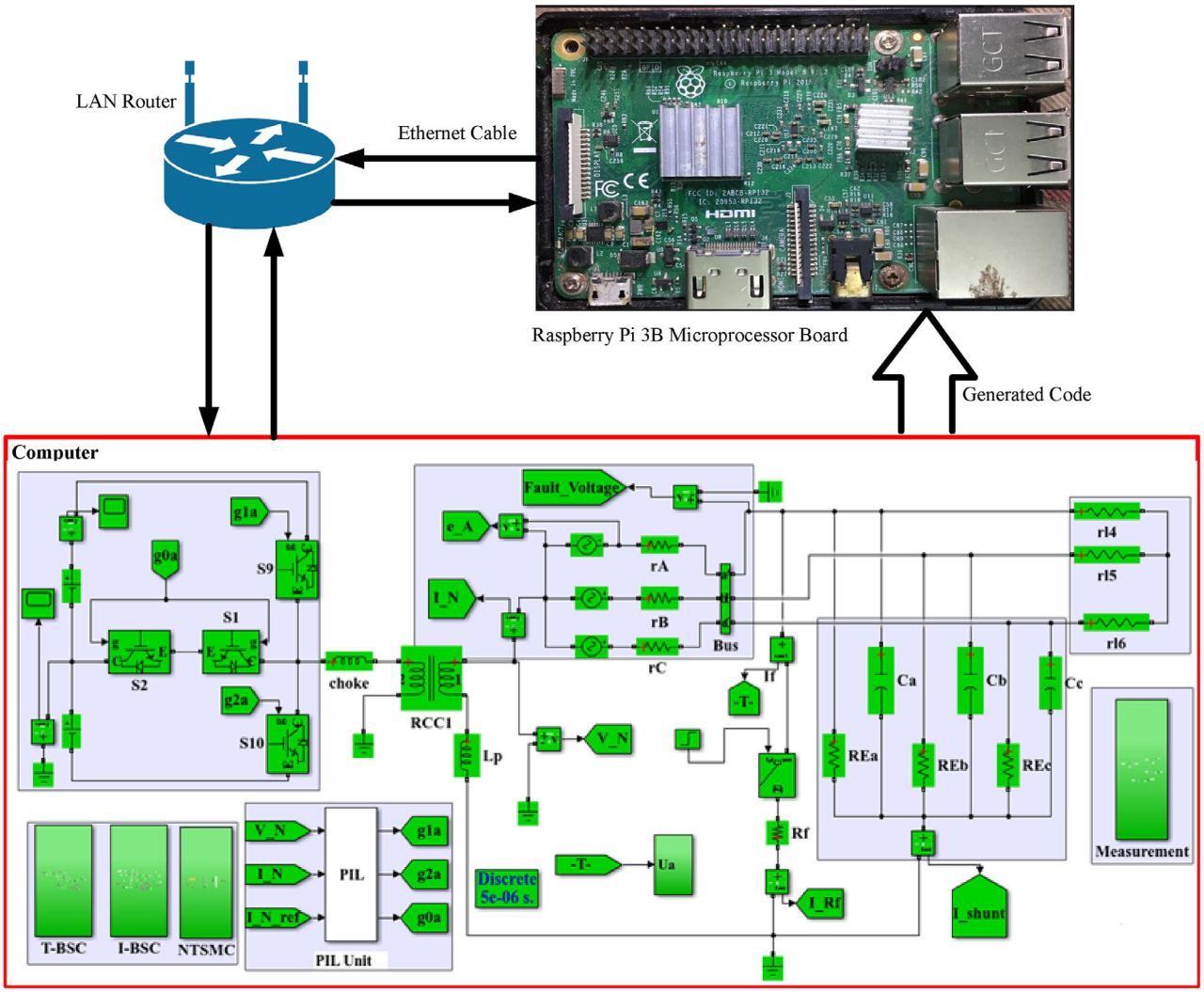

FIGURE 14 PIL platform

that T-BSC. The performance is further analyzed through the PIL validation as discussed below.

5 | PIL VALIDATION

In order to evaluate the viability of the proposed I-BSC, a PIL simulation is performed in this section as it is now widely accepted by the research community to analyze the application of any newly designed controllers. In the PIL framework, the control algorithm is generally deployed in a dedicated processor while the plant operates in an offline simulation platform. In this work, a Rasberry Pi 3B Quad-Core 64-bit Microprocessor Development Board is used to deploy the control signal generated in MATLAB/Simulink environment, while the plant is entirely in the simulation platform as shown in Figure 14. Through the PIL block in Figure 14, the control inputs are routed back to the processor in which the control signals generated from this processor are used to drive the inverter switches in MATLAB/Simulink platform. As shown in Figure 14, the Ethernet line is utilized to send and receive data between the development board and MATLAB/Simulink. It is worth noting that the settings of the experiment are identical to those utilized in previous simulations. However, both low and high impedance faults are simulated to analyze the effectiveness of the proposed controller using the PIL, while considering the similar fault sequence. Here, the performance of the I-BSC is compared with the T-BSC and NT-SMC.

5.1 | Scenario 1: PIL validation for $R_f = 500\ \Omega$

or analyzing the low fault impedance scenario, the value of R_f is considered as 500 Ω where this fault is applied on Phase A to demonstrate the fault-compensation capability of the proposed scheme. The instantaneous and rms values of the faulty phase voltage and current are shown in Figures 15 and 16, respectively. The rms value of the faulty phase voltage and current drop to values lower than 750 V and 0.5 A (at t = 2.4 s)

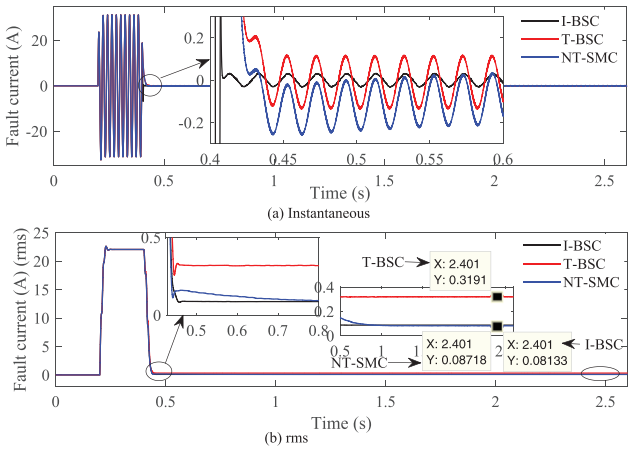

FIGURE 15 Fault current (instantaneous and rms) from the PIL validation when the SLG fault occurs on Phase A with R_f=500 Ω

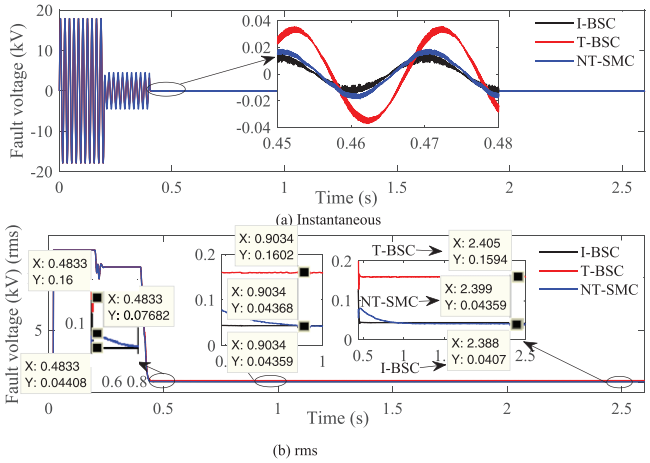

FIGURE 16 Faulty phase voltage (instantaneous and rms) from the PIL validation when the SLG fault occurs on Phase A with R_f=500 Ω

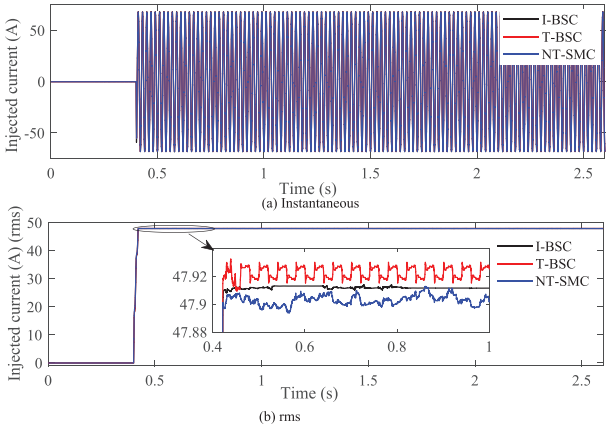

FIGURE 17 Injected current (instantaneous and rms) by the RCC inverter from the PIL validation when the SLG fault occurs on Phase A with R_f=500 Ω

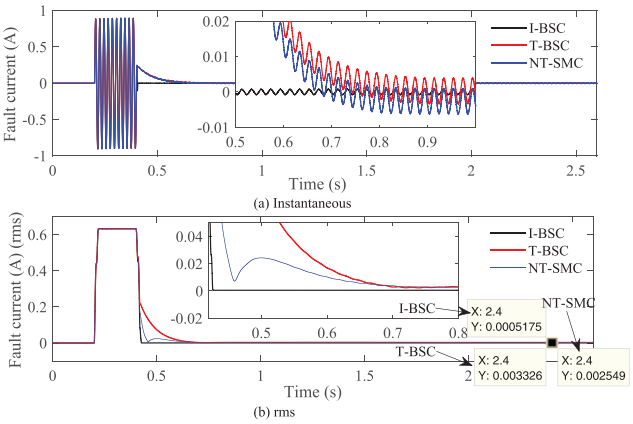

FIGURE 18 Fault current (instantaneous and rms) from the PIL validation when the SLG fault occurs on Phase A with R_f=20 kΩ

TABLE 4 The rms values of the faulty phase voltage (V) for R_f=500 Ω at different instants

RCC activation time (s)	Simulation time (s)	Voltage (V) with I-BSC	Voltage (V) with NT-SMC	Voltage (V) with T-BSC
0.085	0.485	44.08	76.82	160.00
0.5	0.9	43.68	43.68	160.20
2	2.4	40.70	43.59	159.40

or 2 s after the RCC inverter is turned on for all controllers. Figure 17 shows the instantaneous and rms values of the current injected by the RCC inverter. From Figures 15–17, it can be observed that the PIL results are consistent with the simulation results. However, the designed I-BSC can provide superior performance as compared to the T-BSC and NT-SMC. Apart from these, Table 4 shows the rms value of the faulty phase voltage from where it can be seen that the designed I-BSC outperforms both T-BSC and NT-SMC in terms of compensating the faulty phase voltage.

5.2 | Scenario 2: PIL validation for R_f = 20 kΩ

In this scenario, a high fault impedance having a value of R_f = 20 kΩ used while considering the similar fault sequence as discussed in other scenarios throughout the paper. Figures 18–20 show faulty phase voltage, fault current and injected current by the RCC inverter, respectively. From Figure 18, it can be found that there is no noticeable decrease in the faulty phase voltage after the fault is initiated as the fault current is extremely small (i.e. 0.0005175 A for the I-BSC, 0.003326 A for the T-BSC, and 0.002549 A for the NT-SMC) as evidenced from the fault current response in Figure 19. This is quite common due to the behavior of high impedance faults. Table 5 shows the values of the faulty phase voltage for three controllers and it can be

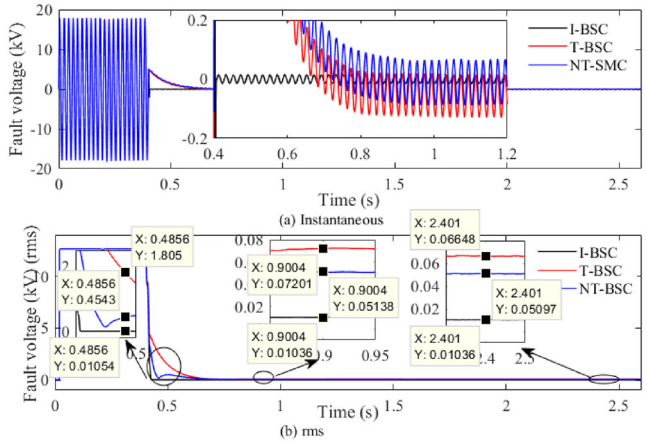

FIGURE 19 Faulty phase voltage (instantaneous and rms) from the PIL validation when the SLG fault occurs on Phase A with R_f=20 kΩ

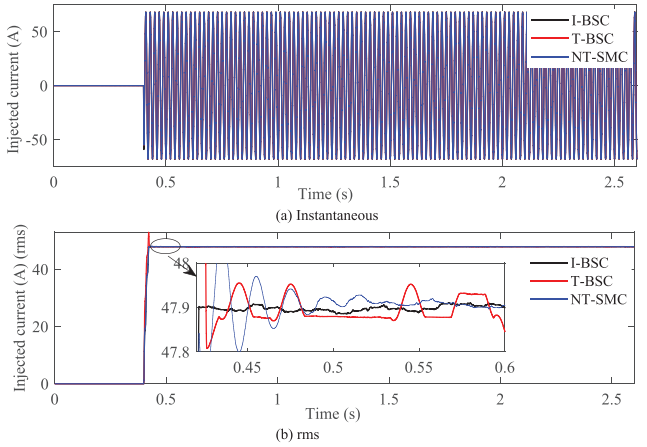

FIGURE 20 Injected current (instantaneous and rms) by the RCC inverter from the PIL validation when the SLG fault occurs on Phase A with R_f=20 kΩ

TABLE 5 The rms values of the faulty phase voltage (V) for R_f=500 Ω at different instants

RCC activation time (s)	Simulation time (s)	Voltage (V) with I-BSC	Voltage (V) with NT-SMC	Voltage (V) with T-BSC
0.085	0.485	44.08	76.82	160.00
0.5	0.9	43.68	43.68	160.20
2	2.4	40.70	43.59	159.40

observed that the designed I-BSC outperforms both T-BSC and the NT-SMC for a high impedance fault.

Hence, both case scenarios demonstrate that the designed I-BSC can be used in a practical scenario. Furthermore, the results under different fault resistances for both simulations and PIL validations clearly indicate that the inclusion of an integral action ensures better dynamic responses due to lower the tracking error for the current injected into the neutral.

6 | CONCLUSION

An integral action is incorporated with the traditional backstepping scheme to design the controller for a residual current compensation inverter in order to guarantee the desired tracking of the neutral current that is essential for the complete elimination of the fault current and thus, improve the self-extinguishing capability of igniting powerline bushfires. The control law for the residual current compensation inverter, within an arc compensation device used for compensated distribution networks in bushfire prone areas, is derived in a way that it theoretically guarantees the convergence of the error to zero. Simulation results are then carried out to further validate theoretical findings for different operating scenarios while benchmarking the results against the standard operational criteria along with providing comparisons with a traditional backstepping controller. Simulation results for all these scenarios clearly depict that the integral backstepping controller performs better than the traditional backstepping controller in terms of injecting the desired current to the neutral and hence, significantly contributing to self-extinguish powerline bushfires by reducing the fault current to almost zero. It is also worth mentioning that the proposed controller always ensures the fault current to a value lower than 0.5 A irrespective of the fault impedance. Furthermore, the proposed controller is used for a single arc suppression device, therefore, it has the ability to compensate only for the single line-to-ground fault. This means that it does not work for the two line-to-ground, two line-to-line, and three-phase short-circuit faults. However, this approach can easily expanded for three-phase arc suppression devices with three-phase inverters and this can be very expensive. Therefore, this has now been planned as a scope for the future work. Moreover, the robustness of the proposed scheme against parametric uncertainties and external disturbances has been overlooked in this work. Future works will consider robustness aspects of the integral backstepping controller by considering the effects of both parametric uncertainties and external disturbances in compensated distribution networks.

CONFLICT OF INTEREST

The authors do not have any conflict of interests.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

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